

# 180nm CMOS process based L-band CML to CMOS converter

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## ABSTRACT

*In this paper, design of a CML to CMOS converter using 180 nm CMOS standard logic process has been presented. In mixed signal design like PLL, logical conversion circuit is needed between differential analog VCO and standard logic digital components. Presented Design is simulated at 1.25 GHz using cadence virtuoso. Proposed design can able to convert differential swing into rail to rail digital output.*

**Keyword:** - Voltage Controlled Oscillator (VCO), Phased locked Loop (PLL), Current Mode Logic (CML)

## 1. INTRODUCTION

Mixed-Signal and RF Chip design can be a challenging aspect of IC development. Presently judging the interplay of transistors, resistors, capacitors and inductor within a semiconductor device depends on precise models, exacting tools and processes, and a solid understanding of the physics behind today's advanced chip process nodes. Mixed-signal ICs are more difficult to design and manufacture than analog only or digital only ICs. For example, an efficient mixed-signal IC would have its digital and analog components share a common power supply [1]. However, analog and digital components have very different power needs and consumption characteristics that make this a non-trivial goal in chip design [1]. In mixed signal PLL, output of analog VCO is fed to CML divider. Rest of the divider section mostly implemented with standard logic digital components. One of the serious concern in these type of mixed signal design is, Output of CML divider is bidirectional and differential but standard logic CMOS digital circuit required rail to rail unidirectional, single input. Proposed design can be used as interface between analog and digital components, which can able to convert analog differential inputs to rail to rail unidirectional output.

## 2. CML TO CMOS DESIGN

Schematic of CML to CMOS converter is designed and simulate using cadence virtuoso. After the Schematic, Layout of CML to CMOS converter is designed. Then Design Rule Check (DRC), Layout Versus Schematic (LVS) and parasitic extraction also performed. To observe the effect of parasitic elements on design Post layout simulation is performed using extracted view. Methodology used for optimum design is as shown in Figure 1. Figure 2 describes the schematic of CML to CMOS converter. Dimensions of each MOSFETs in Figure 2 is chosen carefully to maintain the speed operation as well as to get rail to rail output.

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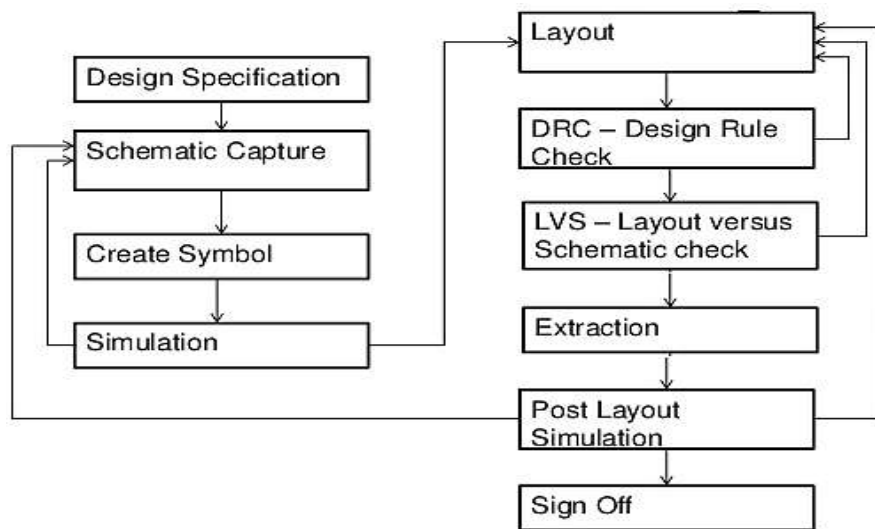


Fig -1: Cadence Design flow

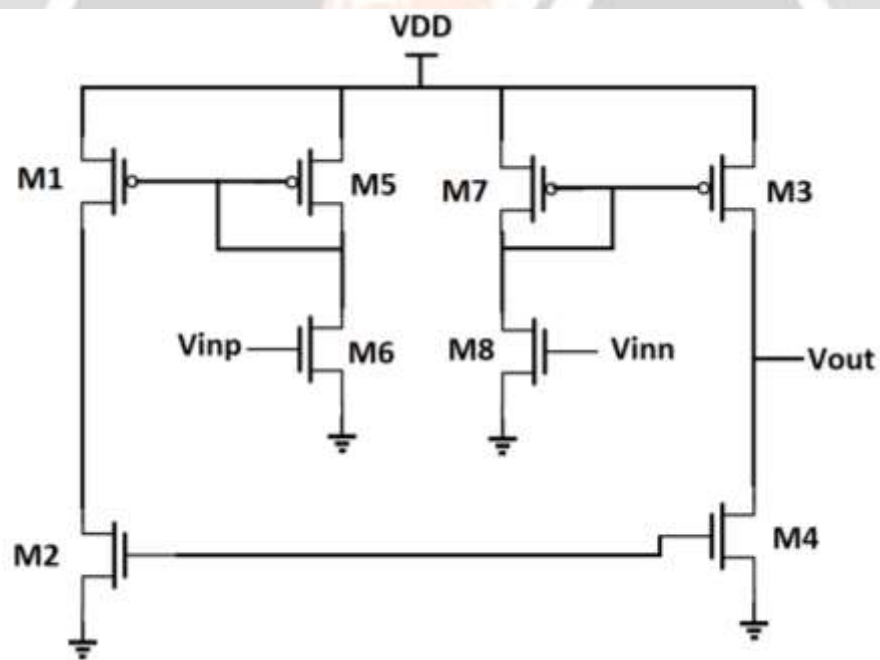


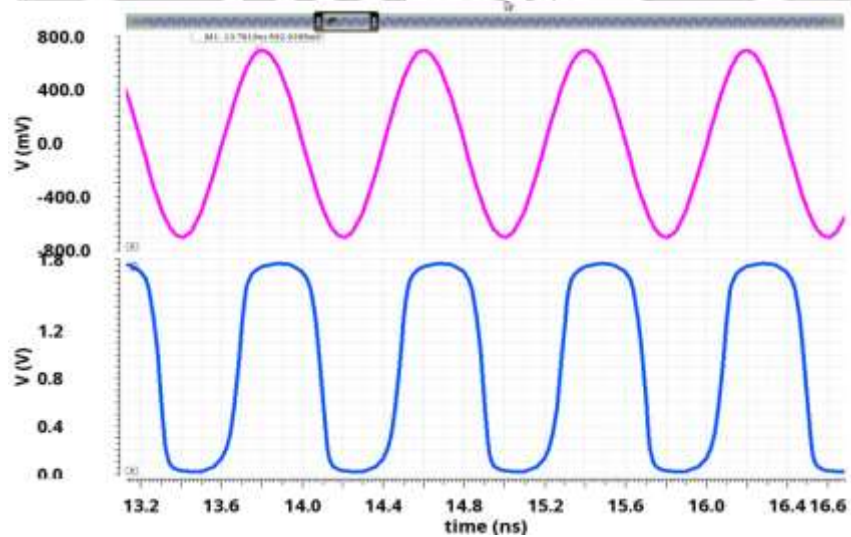
Fig -2: Schematic of CML to CMOS converter



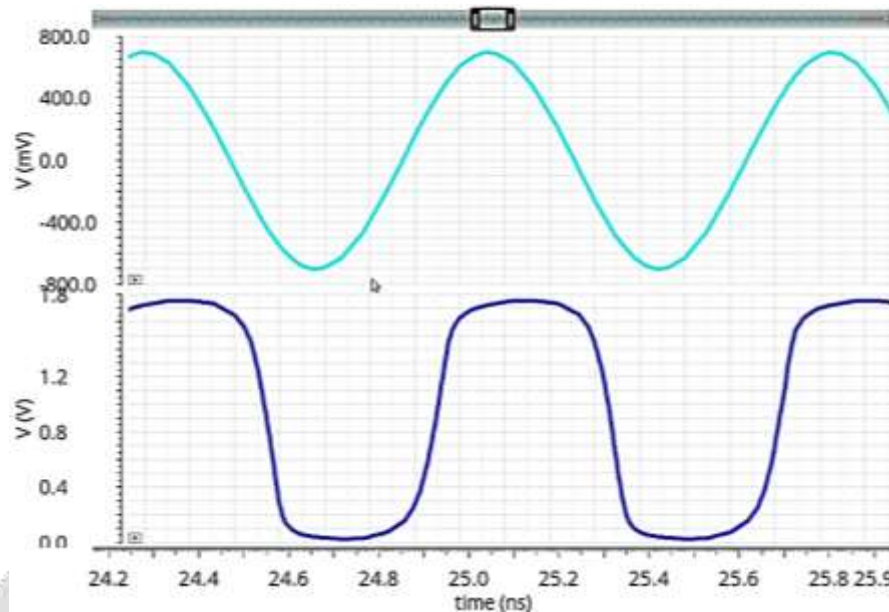
**Fig -3:** Layout of CML to CMOS converter

### 3. RESULTS AND DISCUSSION

Designed schematic and layout is simulated using Analog Design Environment (ADE) in cadence virtuoso. Figure 4 shows the results of schematic of CML to CMOS converter. After extraction, to observe the effects of parasitic elements, post layout simulation is performed. To observe the behavior of proposed design, transient mode simulation is performed with 1.25 GHz input signals.



**Fig -4:** Schematic simulation results of CML to CMOS converter



**Fig -5:** Post layout simulation results of CML to CMOS converter

As shown in Figure 5, Post Layout simulation results follows the schematic results. From the Figure 4 and Figure 5, it is concluded that proposed design can able to produce the full swing even though input signals are not the full scale signals.

#### 4. CONCLUSIONS

In this paper, 180nm CMOS process based CML to CMOS converter is designed and simulated. Proposed design can be very useful to development of mixed signal PLL. Where the CML to CMOS converter can be used as bridge between analog and digital blocks.

#### 5. ACKNOWLEDGEMENT

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#### 6. REFERENCES

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