8-BIT SAR ADC USING COUNTER-BASED DIGITAL CONTROL CIRCUIT IN 90NM CMOS TECHNOLOGY

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ABSTRACT

The conventional 8-bit SAR ADCs that use conventional Control Circuit consume more power, have more delay, and take up more area. In terms of area, power savings, and delay, approximate 8-bit SAR ADCs using CBDCC are far better. Instead of binary search resistive ladder network we used a charge-redistribution capacitor array DAC in this. Traditional SAR based ADC are not suitable for biosensor application, operating at very low frequency due to it is more power requirement in fault tolerant application. To meet low power requirement CBDCC is implemented in Cadence virtuoso environment using 90nm CMOS Technology to evaluate the power consumption, critical path delay. An 8-bit SAR ADC using CBDCC is designed using the D-FFs and 4-i/p clock-gated AND gates. A double-tail latch type comparator has been integrated into the design to reduce power consumption and increase speed. For charge redistribution DAC, area efficiency and for faster operation, synchronous type SAR logic with a counter-based controlled unit is proposed. 90 nm CMOS technology was used to design and simulate the structure. The design is divided into several blocks, which are individually implemented and tested at 10K samples/s and 1V power supply. The SAR-ADC consumed 252.5µW. The results show that the proposed SAR-ADC in 90 nm technology is a good candidate for biomedical medical application.

Keyword: - *Analog-to-digital converter (ADC), digital-to-analog converter (DAC), successive approximation register (SAR) ADC, ultra-low-power sensor etc.*

1. INTRODUCTION

For biosensor applications operating at very low frequency, there is a need for ultra-low-power SAR-based ADC. This uses two ADC techniques viz; 1) a novel DAC switching to suit SAR ADC with single-ended 2) a Counter-based digital control circuit (CBDCC) circuitry. Using half, the reference voltage, the DAC switching approach digitizes the input signal in the range [0, Vr]. It is found to decrease power consumption up to 88% when compared to traditional one. Whereas 30% power reduction is possible in a counter-based controller. Several methods are utilized to lower power requirements in digital circuits by lowering V_{DD} and new CMOS technology.

Adopting low V_{DD} and modern CMOS technology, many ways are designed to improve power consumption in digital circuits. The SAR comparator control algorithm (SAR-CC) and asynchronous binary search using comparators are meant to remove the SAR controller using comparators.

Conversion time can be reduced by using low frequency clock, and the asynchronous approach utilized in the clock power consumption path of high-frequency SAR ADCs. The clock frequency input, it is to give input clock frequency to sampling frequency fs. For the synchronous SAR ADC with N-bits, input clock frequency is

(N+2) fs, (N+2) if a clock cycle is required to digitize a sample. Most of the digital circuits operate at sampling frequencies in the asynchronous SAR ADC. This helps to save power. CBDCC achieve this by reducing the circuit size but need to maintain the switching activity similar to the traditional digital method. Compared with the traditional SBDCC, the counter-based method has many advantages. First, Ten AND or NOR gates, Resettable D-Flip flops, 8 settable/resettable latches, are the requirement of the proposed circuit for as against this the traditional circuit needs 10 resettable DFFs and 8settable /resettable D- flip flops.

D-FF size is double that of the latch. The total size of the proposed method equivalent to 13 D-flip flops with the latch half of that of the D-flip flop. It would be smaller than the traditional one that has 18 Flip-flop. Second, many components in the proposed digital circuits function at a low frequency since, with the exception of the counter, using a high clock frequency, all digital circuitry would use a sampling frequency.

2. LITERATURE REVIEW

Prof. Prashant Avhad, "Design of 8 bit Analog to Digital Converter (ADC)" [1], In today's technologically advanced world, the majority of applications demand that the entire size of the system be reduced in terms of the amount of space that it occupies on any given device. In addition to being extremely power-demanding, the data converter section is typically much more power-demanding than other blocks of any architecture. For this reason, low power has become a strict requirement in the majority of systems, and being maintained at a low figure has practically become a mandatory specification in many applications. Out of all the data converter control logic architectures, we have selected the SAR control logic architecture for our thesis work since it is one of the most effective medium resolution attainable converter systems. When we first encounter the various forms of SAR control logic, our attention is directed toward choosing an appropriate comparator architecture, SAR control logic, and DAC. Based on this analysis, the dynamic two-stage comparator, SAR Control Logic, and BWC Capacitive Array as DAC are chosen because of their energy efficiency, low power consumption, and ability to operate at low supply voltages. The schematic model of the entire system will be attempted to be implemented using the EDA tool Microwind 3.5 and DSCH in order to satisfy the project's technical requirements.

Simon Chaput, David Brooks, and Gu-Yeon Wei, "An Area Efficient 8b Single-Ended ADC with Extended Input Voltage Range" [2], This brief describes an 8-bit successive approximation register (SAR) analog-to-digital converter (ADC) for autonomous flapping wing microrobots that is implemented within a system-on-chip (SoC). The ADC improves capacitor bank energy-are-product (EAP) by 35.72% by utilizing hybrid split-capacitor sub-DAC approaches. Additionally, the device maintains low power consumption by implementing a wide single-ended input voltage range that permits direct connection to sensors. Compared to the state of the art, this approach provides a 51.7% reduction in the energy consumption of digital-to-analog converters (DACs). Four simultaneous 0.001mm^2 1MS/s ADC cores are multiplexed across 13 input ports in the 40nm CMOS SoC. It runs on a 0.9V supply and allows an input range of 0 to 1.8V. The ADC uses 10.4µW and produces a signal-to-noise and distortion ratio (SNDR) of 45.6dB for an input signal that is 1.6Vpp at 1MS/s.

Piotr Otfinowski, "A 2.5MS/s 225 µW 8-bit charge redistribution SAR ADC for multichannel applications" [3], The integrated analog-to-digital converter design for multichannel readout circuits using UMC CMOS 180nm technology is presented in this research. It was suggested to use the successive approximation architecture with charge redistribution. The speed and accuracy of CMOS switches are explained in detail for a capacitive digital-to-analog converter (DAC). Additionally, a resistive auxiliary sub-DAC is offered to minimize the area of the DAC. As a comparator, a synchronous 30 MHz latch with preamplifier is employed. At 225 µW, the designed ADC can achieve conversion rates of 3 MS/s. The presented circuit has modest nonlinearity, with 0.3 LSB, according to the final simulation results.

Minglei Zhang, Xiaohua Fan, "An energy-efficient SAR ADC using a single-phase clocked dynamic comparator with energy and speed enhanced technique" [4], An innovative dynamic comparator-equipped, energy-efficient

500 kS/s 8-bit SAR ADC is presented in this research. An inverter-based pseudo-latch and a cross-coupling cascode-based preamp are used in the suggested dynamic comparator. Compared to a traditional double-tail dynamic comparator, this method achieves a 40% faster speed, a 24% lower power consumption, and a similar input-referred noise level. Furthermore, the suggested comparator just needs a single-phase clock. Using a 0.5 µm CMOS technology, the prototype ADC's active area measured 0.18 mm². With a Nyquist frequency input signal and a 1.8 V supply, the ADC can achieve 47.5 dB and 63.2 dB SNDR and SFDR, respectively, while consuming 18.2 µW at 500 kS/s. It achieves Walden FoM of 188 fJ/conv.-step.

Weibo Hu; Yen-Ting Liu; Tam Nguyen; DonaldY. C. Lie; Brian P. Ginsburg, "An 8-Bit Single-Ended Ultra-Low-Power SAR ADC with a Novel DAC Switching Method and a Counter-Based Digital Control Circuitry" [5], The ultra-low-power successive approximation register (SAR) analog-to-digital converter (ADC) design proposed in this work is specifically tailored for very low frequency biosensor applications. Two innovative strategies are presented: 1) a counter-based digital control circuitry; and 2) a novel digital-to-analog converter (DAC) switching method appropriate for single-ended SAR ADCs. The DAC switching approach lowers the power usage in the DAC during digitization by 87.5% compared to the traditional one. It does this by using VR /2 as the only reference voltage to digitize the input signals inside [0, VR]. The digital circuitry's power consumption can be reduced by 30% using the counter-based controller. Two prototype 8-bit SAR ADCs are constructed, one using a TSMC 0.18-µm CMOS process and the other in a TI 0.35-µm Bipolar-CMOS-DMOS (BCD) technology. At 2 kS/s, the 0.35-µm ADC achieves a figure of merit (FOM) of 227 fJ/conversion-step and a signal to noise and distortion ratio (SNDR) of 48.2 dB while consuming 101 nW. At 2 kS/s, the 0.18-µm ADC can attain a FOM of 79.9 fJ/conversion-step and an SNDR of 46.3 dB with just 27 nW.

3. PROBLEM STATEMENT

We aim is to design, layout, and test a SAR ADC based on an 8-bit CBDCC technique using the CADENCE tool and to improve Energy area product (EAP) by providing a range of analogue input voltages greater than the supply voltage. Besides we would like to carry out the performance analysis in terms of area, power consumed, and leakage.

4. OBJECTIVES

- To design and implement schematic and Layout of a power-efficient high speed 8-bit CBDCC using Virtuoso of Cadence tool.
- To perform DRC and LVS check to extract parasitic using ASSURA.
- To test the performance of the implemented 8-bit CBDCC for different input combinations.
- To analyze the power consumption, time delay, and are using tools like Spectre, ADEL, etc.

5. METHODOLOGY OF IMPLEMENTATION

5.1 CBDCC Block Representation

The system block representation of CBDCC used for building control Logic of SAR ADC is as shown in Figure-1. It is reshown for convenience.

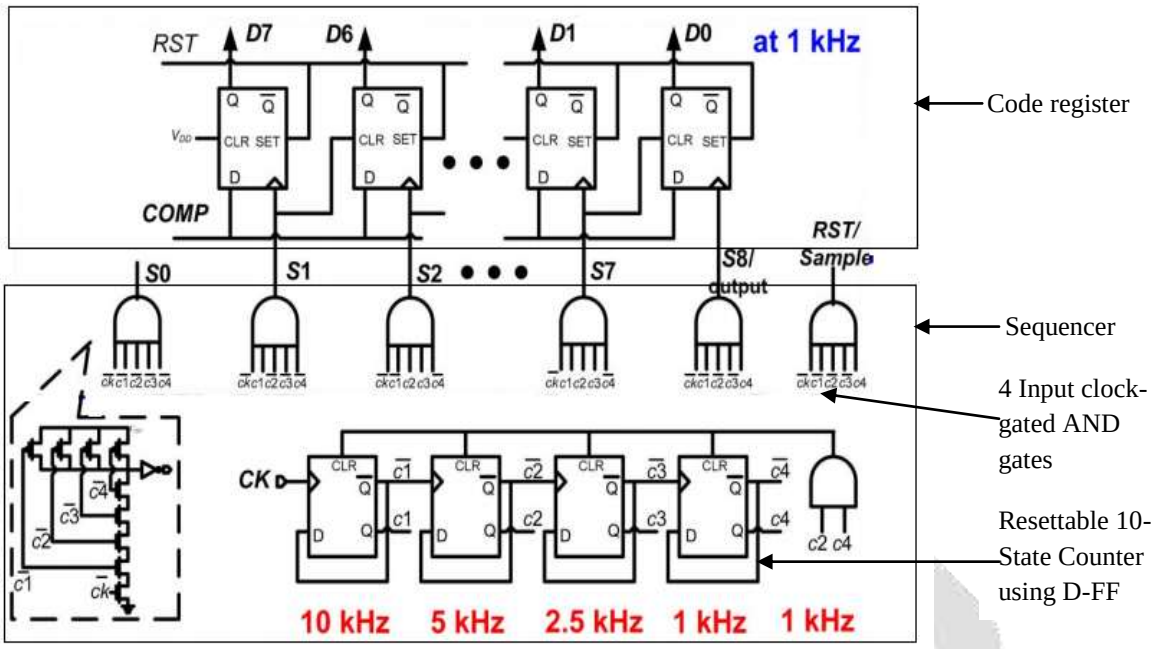

Figure 1: Structure of 8-bit CBDCC for an eight-bit SAR ADC with a sampling frequency 1kHz.

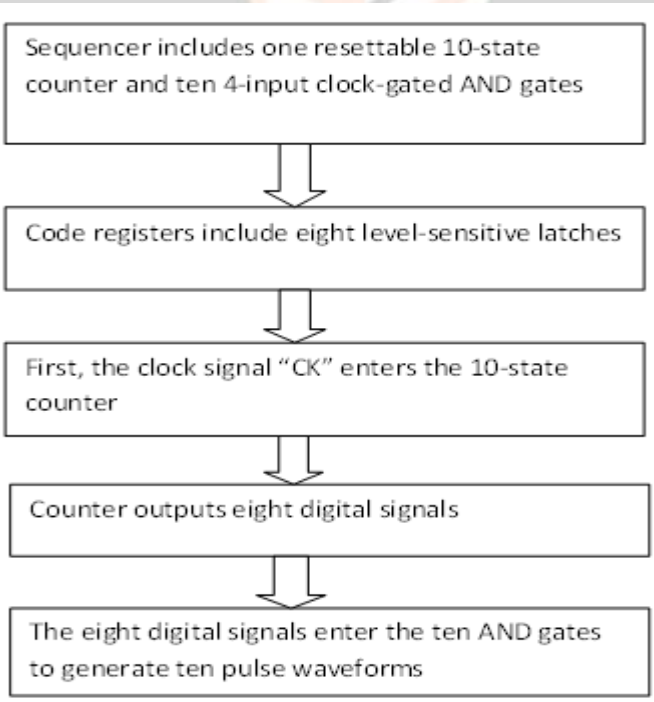

Figure 2: Flowchart of digital control

5.2 STEPS FOR IMPLEMENTATION OF 8-BIT COUNTER-BASED DIGITAL CONTROL CIRCUITS:

A counter-based digital control circuits for an 8-bit SAR ADC will be carried out in CADENCE EDA tool:

i. Design and implement 8-bit counter-based digital control circuits in Cadence using AMS design flow or Verilog ASIC flow and form components.
ii. The D flip-flop is implemented using NAND gates and inverter.
iii. Implement the D-F-F design in cadence Virtuoso schematic editor and simulate in Cadence Virtuoso analog design at 180nm process technology.
iv. Design the layout of the 8-bit counter-based digital control circuit design using cadence virtuoso Layout.
v. Integrate the components in steps 2,3 to build a 8-bit low power high frequency counter-based digital control logic circuits.
vi. Analyze the performance of this 8-bit counter-based digital control logic circuits.
vii. Compute the performance parameters such as Dynamic power consumption, DNL, INL and FOM.
viii. Compare the performance of 8-bit counter-based digital control circuit in traditional one.

6. CONCLUSIONS

The 8-bit SAR ADC using CBDCC is implemented using 90 nm Technology using Cadence Virtuoso tool at 1 V supply voltage and sampling rate of 10 KS/s. Frequency of 1KHz using Cadence Virtuoso tool under 90 nm CMOS technology. At 1 V supply voltage the CBDCC for SAR ADC consumes 252.5µW of power.

7. REFERENCES

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