ANALYSIS OF PWM TECHNIQUES APPLIED TO HALF BRIDGE ANPC INVERTER CONNECTED TO GRID

T. Geetha[1], A. Anil Kumar[2]

[1] Student, Dept of EEE, Vaageswari college of Engineering, Telangana, India
[2] Associate.Prof, Dept of EEE, Vaageswari college of Engineering, Telangana, India

ABSTRACT

This paper presents a PV based Inverter for higher efficiency and safety driven grid connected system. Several Inverter topologies have been proposed and many of them are available commercially today. Among them, the Neutral Point Clamped (NPC) and derived topologies offers high efficiency, low leakage current and low EMI. However one main disadvantage of the NPC inverter is given by an unequal distribution of the losses in the semiconductor devices, which leads to an unequal distribution of temperature that can affect life time. By using the Active NPC topology, where the clamping diodes are replaced by bidirectional switches, the power losses distribution problem is alleviated. The modulation strategy is a key issue for losses distribution in this topology. In this paper two known strategies such as multi-carrier PWM are discussed and a new PWM strategy, namely the Adjustable Losses Distribution is proposed for better losses distribution in the Active NPC topology. A three phase grid connected system is also proposed as an extension work to this. Simulations analysis using MATLAB/SIMULINK software results help in evaluating the modulation strategies.

Keyword: *- Multi-carrier PWM Techniques, PV system, Active-NPC, NPC, Adjustable Losses Distribution ALD*

1. INTRODUCTION

Electricity is becoming a central need of human being. Presently maximum electricity is generated at thermal and hydro power plants. These plants depend upon coal which is limited on earth's crust causing shortage of power supply. To overcome these shortcomings use of non renewable sources is very much useful. In Asian countries solar energy is abundantly available. Applications using solar energy will minimizes energy crisis. As solar energy is clean source of energy, power generation is easy and eco-friendly. Also for energy conversion moving part or heavy machinery is not required. For efficient conversion of solar energy into an electrical power various inverter topologies were proposed. Transformer-less inverter topology is proposed for cost effective PV system, which eliminates leakage current in an inverter system, due to which the overheads over transformer were reduced [1]. To reduce an overall costing on an inverter a new methodology for design of transformer-less photovoltaic (PV) inverters for grid-connected PV systems with less switching is demonstrated [2]

Single-phase photovoltaic (PV) systems (1-10kW) are attractive DPGS (Distributed Power Generation System) in household applications. Hence they have specific needs such as maximum profitability through high efficiency, long life time, low prices, small volume and safety [3], [4]. In order to improve the efficiency of house-hold PV inverters and lower the system prices, isolation transformers used in the past to interface the PV-system with the electric grid in order to provide higher safety and lower leakage current, is typically not present in the new generation of PV-systems. Thereby, many transformer-less applications were proposed [3]-[6], including HERIC topology [7], Full Bridge (FB) with DC Bypass topology [8], H5 topology [9], Neutral Point Clamped (NPC) topology, Conergy NPC topology and Active NPC topology. All these voltage source transformers-less PV inverter topologies can be classified in two groups: one is the topologies derived from conventional full-bridge topology as HERIC, H5 and FB with DC Bypass topology; the other group is the topologies derived from conventional half bridge NPC topology as NPC, Conergy NPC and Active NPC. NPC topology was proposed by Baker in a patent in 1970's, in 1981 for the first time stated in the paper by Nabae, Takahashi and Akagi in [10] and it has been proven to provide high

efficiency and to allow connection to the grid without step-up transformer. [11], [12] Compared with the traditional 2-level full bridge PWM inverters, the NPC topology inverters produce no common mode current which make it appealing for photovoltaic application [13].

Meanwhile one disadvantage of the NPC inverter is given by an unequal distribution of the losses in the semiconductor devices, which leads to an unequal distribution of temperature and limits the output power of the inverter. In order to overcome this drawback, the conventional NPC topology was extended to the Active NPC structure [14]-[15]. Compared with conventional NPC topology, the total efficiency of Active NPC topology is not improved, but this topology has more switching states freedom degrees, which could be used in DC-bus voltage balancing applications [16]-[19] , which is another essential for all NPC topologies. Some of the Active NPC PWM strategies were also used for balancing the losses distribution [20], [21], but all of them were not optimal.
This paper introduced two Active NPC PWM strategies [20], [21] used for balancing the power losses distribution and proposed a novel PWM strategy named Adjustable Losses Distribution (ALD) for better losses distribution balancing. This modulation method could adjust the switching losses distribution depended on different switches conduction loss distribution. By using this method, it could optimal the total switches losses distribution.
Simulation and experimental results are given to validate that the proposed strategy has better losses distribution performance, which could enlarge the components and inverter SOA areas.

2. EQUIVALENT PHOTOVOLTAIC ARRAY

PV array's output current-voltage curve reflects PV array's dependence on environmental conditions such as ambient temperature and illumination level. Typically, the illumination level ranges from 0 to 1100Wb/m2 and the temperature range is between 233 and 353 K. Normally, we select 1100 and 298 as the reference values for illumination level and temperature respectively. The relationship between PV array's output characteristics and environmental conditions could be illustrated from general simulation results of PV array. PV array's output power is increased as illumination level increases, while PV array's output power is improved with the decrease of the ambient temperature. The equivalent circuit of a typical PV-cell is given below.

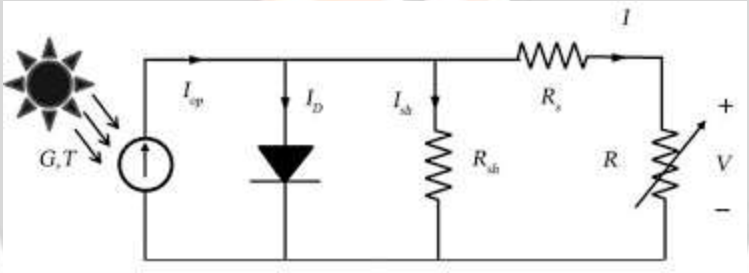


Fig-1: Equivalent circuit of photovoltaic cell

Figure reflects a simple equivalent circuit of a photovoltaic cell. The current source which is driven by sunlight is connected with a real diode in parallel. In this case, PV cell presents a p-n junction characteristic of the real diode. The forward current could flow through the diode from p-side to n-side with little loss. However, if the current flows in reverse direction, only little reverse saturation current could get through. All the equations for modelling the PV array are analysed based on this equivalent circuit.
Boost power converters have been widely used for Power Factor Correction (PFC) in AC-DC conversion and for power management in battery powered DC-DC conversions. Moving beyond low-power applications, such as cellular phones, smart phones and other portable electronic products, boost converters are being used more and more in medium-power applications. For example, in computing and consumer electronics, boost converter-based LED drivers for notebook displays, LCD TVs and monitors have been developed. In communications and industrial products, simple boost converters are used in satellite dish auxiliary power supplies and peripheral card supplies. As boost converters run to CCM (Continuous Conduction Mode), a complex pole pair and a Right-Half Plane (RHP) zero will present in the dynamic characteristic. Some applications of boost converter:

- Programmable soft turn-on for inrush current control
- Hiccup mode for over-current protection
- Complete shutdown with source-load separation
- Simple loop compensation
- Protection for power MOSFET (Q_2) failure

3. TOPOLOGY AND OPERATION PRINCIPLE OF THE PROPOSED CONVERTER

Due to the structure of PV panels, the leakage capacitance between the PV panels' output terminals and ground reaches a significant value. In order to save using isolation transformers, the conventional half bridge NPC topology is a popular topology used in PV inverter applications [22], [23]. In half bridge NPC converters, zero voltage can be achieved by "clamping" the output to the grounded "middle point" of the dc bus using D+ or D depending on the sign of the output current. As presented in Fig. 1, by using this topology, the voltage V_{PE} is clamped to $V_{PV}/2$, the leakage current could not be generated through C_{PE}. All half bridge topologies could be used in this kind of applications to eliminate the leakage current. However NPC half bridge topology has three output voltage levels and better efficient performance.

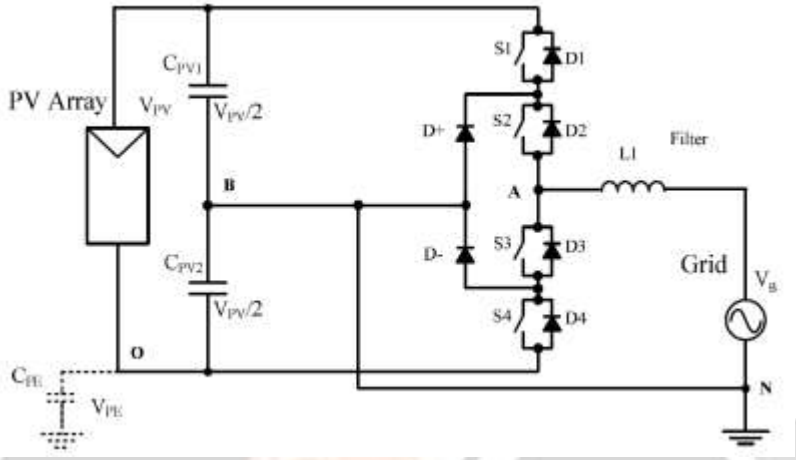


Fig. 2: Neutral Point Clamped Half Bridge

Table I: Switches States of NPC Half Bridge Inverter

Voltage	S1	S2	S3	S4
Positive	1	1	0	0
0^+	0	1	1	0
0^-	0	1	1	0
Negative	0	0	1	1

Since this topology has just one zero state, the PWM method of half bridge NPC has no more options. The commutation states and the switching PWM pattern of the NPC inverter are given by Table I and Fig.2, where "0" stands for "OFF" state of IGBTs while "1" stands for "ON" state of IGBTs. In Fig. 3, *Sr* is the output voltage reference sinusoidal modulation wave which is generated by grid-connected current loop controller [20], [21]. During the positive half cycle of the grid voltage, S2 is ON and only S1 switches at the switching frequency. Therefore, the dead time between S1 and S2 might be set to zero by using this PWM strategy. S3 and S4 work complementarily to S1 and S2, respectively. Fig. 3 shows the switching losses of a 5kW NPC topology inverter at different switching frequencies which presents unbalance losses distribution among the semiconductors. This figure points out that the stresses due to switching losses on the outer switches S1 and S4 is higher than on the inner switches, especially at higher frequency (Fig. 3b). As the switching frequency increases, the uneven losses distribution in the NPC inverter gets even worse. For the grid connected photovoltaic system, the modulation index (M) is often fixed when DC bus voltage and grid voltage are given, e.g. by using the traditional full-bridge topology connected with 230 V RMS grid, usually using 400 V DC bus, the modulation index is set to M=0.9.

In the case of half bridge NPC topologies, the other obvious drawback is that these topologies need double DC bus voltage compared with traditional full-bridge topology which is the common drawback of all the half bridge PV panels in series or using an additional DC/DC boost converter, but more PV panels in series would influent the maximum power point tracking while using an additional DC/DC boost converter would decrease the efficiency of PV systems [24], [25]. Although by using DC/DC boost converter [26], cascade technique [27] or some other methods [28] could solve this problem ideally, it usually introduces more facilities.

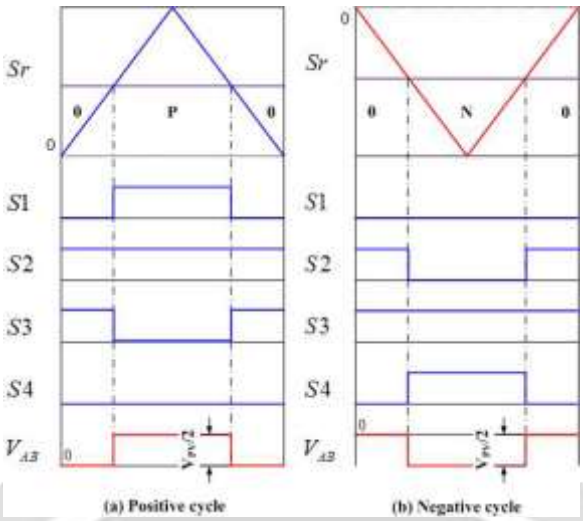


Fig. 3: Sinusoidal PWM for conventional NPC half bridge inverter

3. ACTIVE NPC CONVERTER

The ANPC topology inverter [14] is derived from the conventional NPC topology as presented in Fig. 4. Two active switches with anti-parallel diodes are used for clamping. In contrast to the conventional NPC converter, it has more than one way to clamp the midpoint. The upper clamping path results from turning on S2 and S5 and the lower clamping path from turning on S3 and S6.

The current can be conducted through both clamping ways in both directions. The distribution of the conduction losses during the zero states can be controlled by the selection of the different NPC paths. The switching losses could be controlled by the selection of different commutation states. There are many different PWM strategies for Active NPC control by using different zero states and conduction paths [19]. In this section, two PWM strategies are introduced, and a new PWM strategy named Adjustable Losses Distribution (ALD) is proposed in the next section.

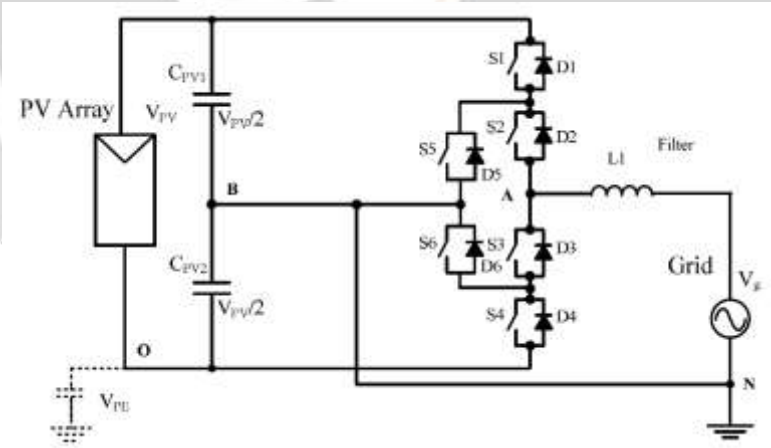


Fig. 4: Active Neutral Point Clamped Half Bridge

- **Classical Active PWM Strategy**

In [20], two PWM strategies, named PWM-1 and PWM-2, for Active NPC are discussed. In the case of the PWM-1 strategy, the inner switches have only conduction losses and the switching losses mainly stress the outer IGBTs. In the case of PWM-2 the strategy, the mainly switching losses only stress the inner switches.

The power losses distribution situation is not improved in the PWM-1 strategy and gets even worse in the PWM-2 strategy compared with conventional NPC topology.

- **DF-ANPC Strategy**

Papers [20] show a PWM strategy named Double-Frequency ANPC control which naturally doubles the apparent switching frequency. In comparison with the other ANPC PWM strategies, the DF-ANPC strategy has four zero states: 0+1, 0+2, 0-1 and 0-2 (Table III). The modulation wave *Sr* is compared with two different carrier waves phase-shifted by TS/2 to generate the pulse as shown in Fig.5. As there are two active states during one switching period, the output voltage has an apparent switching frequency equal to 2fS. The work mode during positive half cycle is analyzed as below: As shown in Fig.5 (a), there are two active state periods with VAO=VPV/2 during one switching cycle. In the case of the first period, when S1 turns on, S2 keeps on state from zero state to active state, the switching on losses totally stresses on S1. When S2 turns off, S1 keeps on state from active state to zero state, all the switching off losses stresses on S2. In the case of second period, the situation is opposite, S2 takes the turn on losses and S1 takes the turn off losses.

By using this PWM method, the switching losses are distributed more uniformly among inner and outer IGBTs as presented in Fig. 6. Compared with the conventional NPC topology, although the efficiency was not improved, the power losses distribution problem is improved.

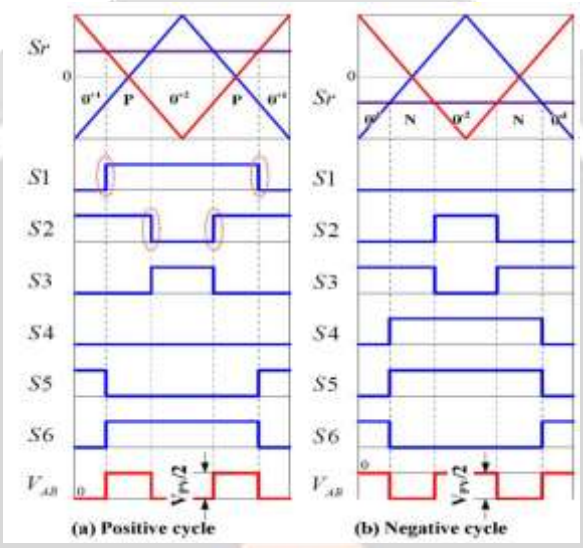


Fig. 5: Sinusoidal PWM for ANPC-DF strategy: (a) Sr>0, (b) Sr<0

Table-III: Switches States of DF-ANPC Half Bridge Inverter

Voltage	S1	S2	S3	S4	S5	S6
Positive	1	1	0	0	0	1
$\mathbf{0^{+1}}$	0	1	0	0	1	0
$\mathbf{0^{+2}}$	1	0	1	0	0	1
$\mathbf{0^{-2}}$	0	1	0	1	1	0
$\mathbf{0^{-1}}$	0	0	1	0	0	1
Negative	0	0	1	1	1	0

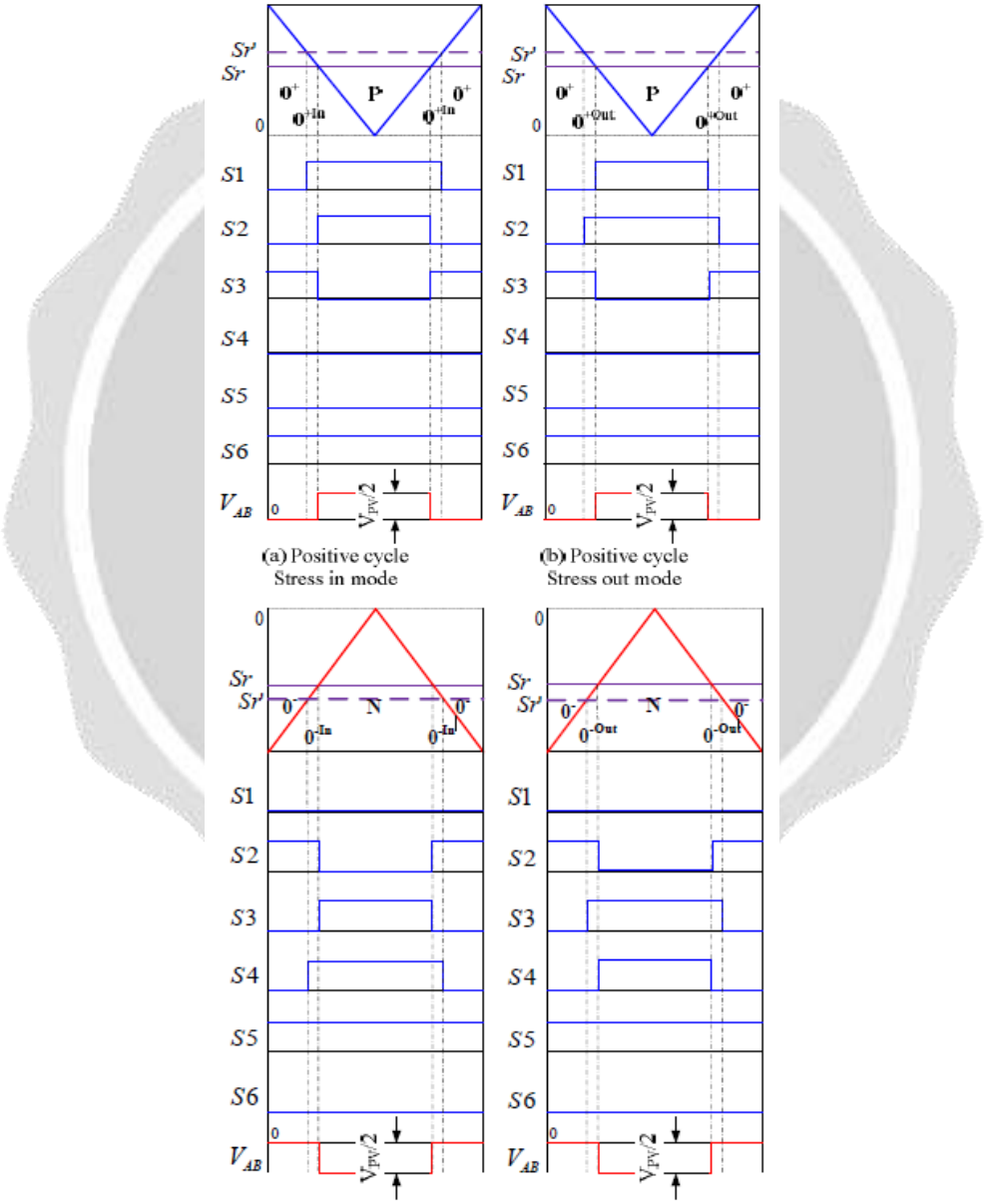
- **ADJUSTABLE LOSSES DISTRIBUTION (ALD) ANPC STRATEGY ALD Strategy**

In the case of previously described classical strategies, the switching losses are concentrated on the outer or inner switches, which lead the power losses distribution unbalanced. The DF strategy could distribute the switching losses between inner switches and outer switches equally, however which still cannot optimize the total losses distribution. In this part, a new PWM strategy (named ALD strategy) is proposed, which combines the classical and DF PWM strategies' advantages.

This strategy uses 6 different zero states and a total of 8 switches states as shown in Table IV and Fig. 7: By distributing switching losses between inner and outer switches, ALD PWM could optimize the IGBT total losses distribution, and simplify the heat sink design.

Table-IV: Switches States of ALD-ANPC Half Bridge Inverter

Voltage	S1	S2	S3	S4	S5	S6
Positive	1	1	0	0	0	1
0^{+In}	**1**	**0**	**1**	**0**	**0**	**1**
0^{+Out}	**0**	**1**	**1**	**0**	**0**	**1**
0^{+}	**0**	**0**	**1**	**0**	**0**	**1**
0^{-}	**0**	**1**	**0**	**0**	**1**	**0**
0^{-Out}	**0**	**1**	**1**	**0**	**1**	**0**
0^{-In}	**0**	**1**	**0**	**1**	**1**	**0**
Negative	**0**	**0**	**1**	**1**	**1**	**0**



(a) Positive cycle Stress in mode (d) Positive cycle Stress out mode (c) Negative cycle Stress in mode (d) Negative cycle Stress out mode

Fig. 6: The switches states and output voltage of ALD strategy (a) Sr>0 Stress-in mode, (b) Sr>0 Stress-out mode, (c) Sr<0 Stress-in mode, (d) Sr<0 Stress-out mode

S5 and S6 switches with grid frequency, half cycle on, half cycle off. (Fig.6). When Stress-in mode is selected, during the positive half cycle, S1 uses signal *Sr'* instead modulation signal *Sr* whereas during the negative half cycle, S4 uses *Sr'* instead *Sr*. When Stress-out mode is used, during the positive half cycle, S2 uses *Sr'* whereas during the negative half cycle, S3 uses *Sr'* instead *Sr*, which is illustrated by Fig. 6.

4. RESULTS AND ANALYSIS

The proposed system is designed in MATLAB/SIMULINK software. The figures 7 to 19 are results of the proposed circuit. The fig-14, 15 & 16 show the input voltage verses output voltage, voltage across and current through the elements of the proposed circuit.

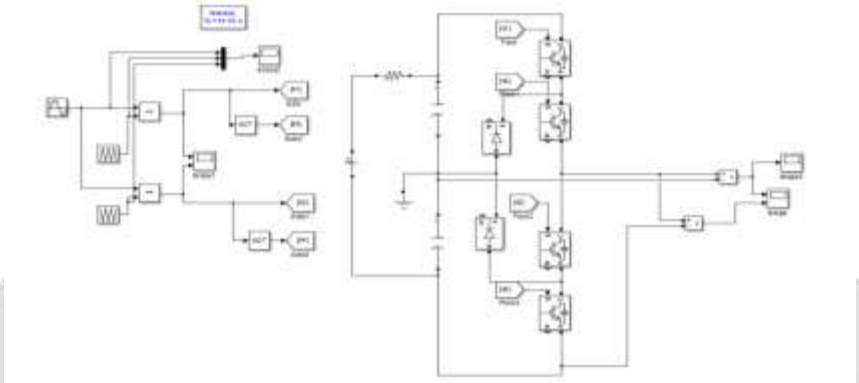


Fig-7: Block diagram of proposed circuit using MATLAB

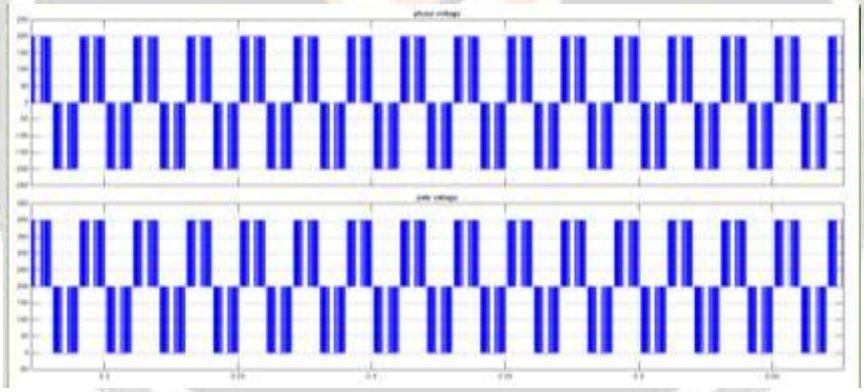


Fig-8: Line Voltage of the Proposed ANPC circuit

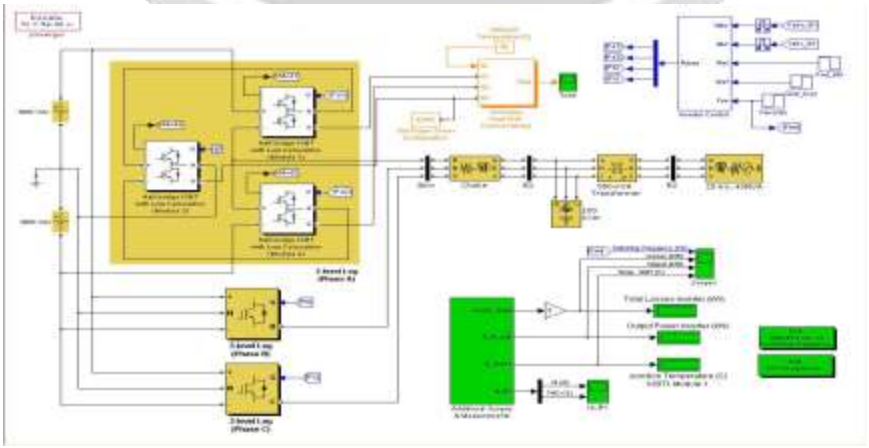


Fig-9: Three phase Circuit diagram of proposed circuit using MATLAB (Extension Work)

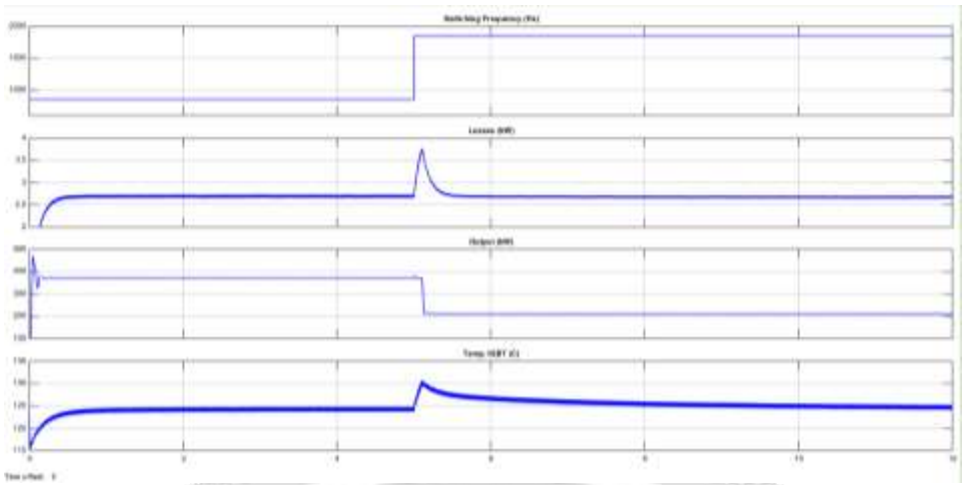


Fig-10: Switching frequency, its corresponding losses, output and Temperature of the switch

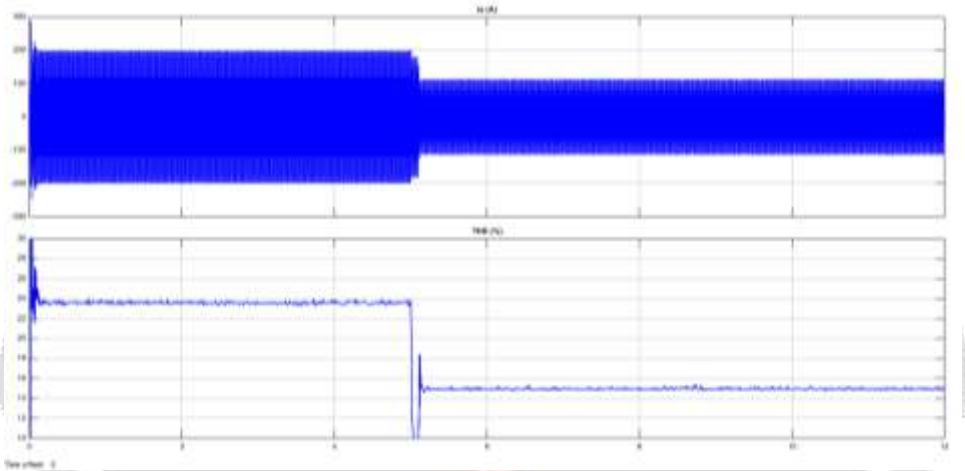


Fig-11: Line current and THD of the modified system

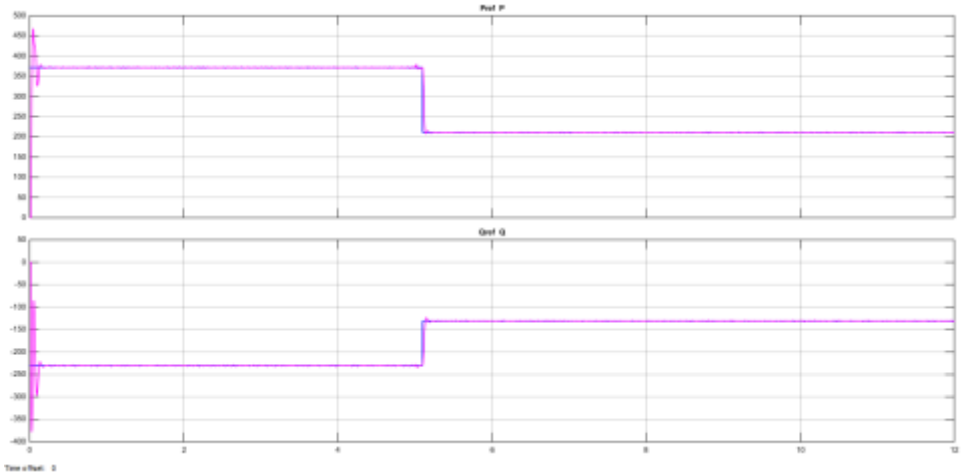


Fig-12: active and reactive power of the system

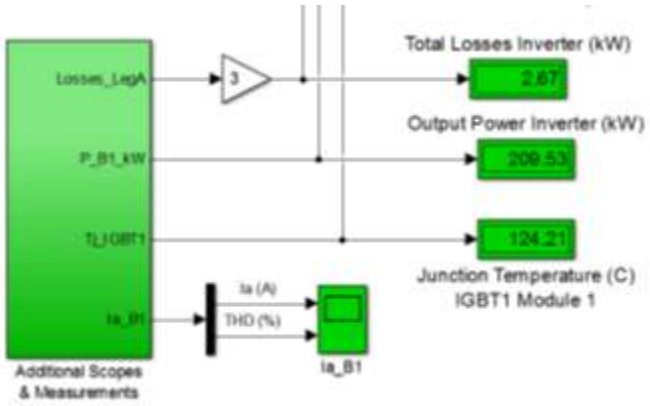


Fig-13: Overall system results

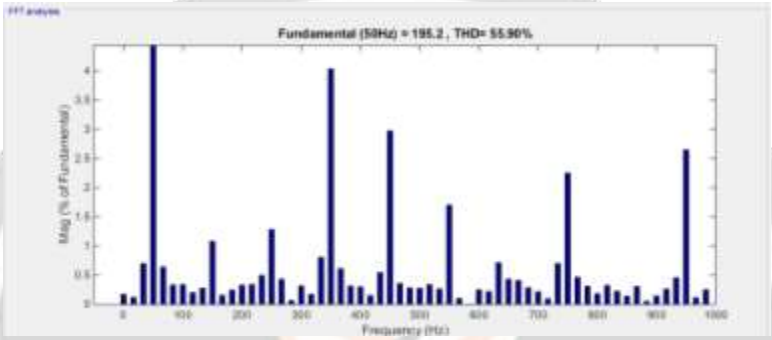


Fig-14: FFT analysis of NPC inverter using proposed control strategy

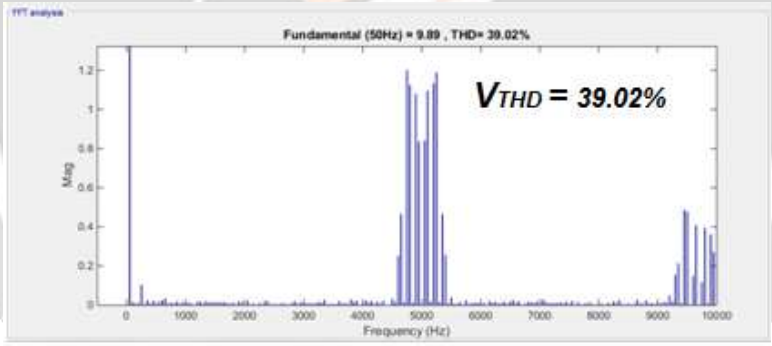


Fig-15: FFT analysis of ANPC inverter using proposed control strategy

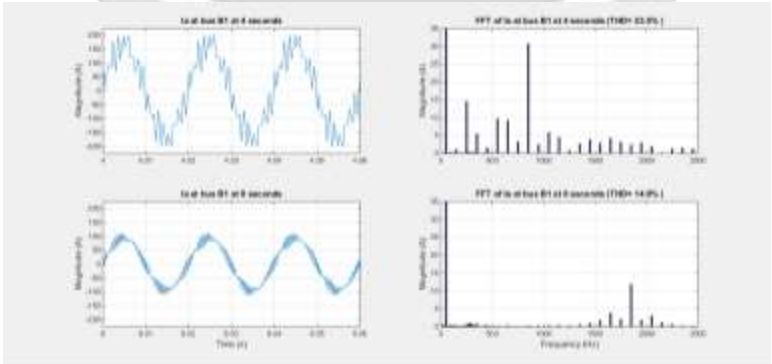


Fig-16: FFT analysis of three phase Neutral point inverter system

5. CONCLUSION

In this paper various NPC topologies have been proposed among those the modified ANPC with multi-carrier PWM has proven to be very suitable for transformer-less PV systems due to their high efficiency, low leakage current and low EMI. The main disadvantage of the NPC inverter is given by an unequal distribution of the losses in the semiconductor devices, which leads to an unequal distribution of temperature and limits the output power of the inverter. The Active NPC structure has been developed in order to overcome this drawback. For the ANPC topology, due to the presence of switches instead of clamping diodes, it is possible to use different modulation strategies aiming at obtaining a better power losses distribution. Thus, the ANPC topology is suitable for the high power transformer-less PV system applications. The modulation strategy is a key issue in this topology. In this paper, a new ANPC modulation strategy named Adjustable Losses Distribution (ALD) is proposed. This PWM method combines the losses distribution advantages of classical and DF-ANPC strategies. Depending on the different modulation index and power factor (which means different conduction losses distribution between inner and outer switches), it is able to choose the most suitable Stress-in/Stress-out mode rate to balance the total losses distribution between inner and outer switches, where the switching losses distribution is controlled by the Stress-in/Stress-out mode rate. The simulation and experimental results show that the losses distribution could be balanced without adding any new components in all the modulation index and power factor conditions.

6. REFERENCES

[1] Saridakis, S. ; Koutroulis, E. ; Blaabjerg, F. "Optimal Design of Modern Transformerless PV Inverter Topologies", *IEEE Transactions on Energy Conversion*, vol. 28 , no. 2, pp. 394-404, June 2013.

[2] Koutroulis, E. ; Blaabjerg, F. "Design Optimization of Transformerless Grid-Connected PV Inverters Including Reliability", *IEEE Transactions on Power Electronics*, vol 28 , no. 1, pp. 325-335, Jan 2013.

[3] Alajmi, B.N. ; Ahmed, K.H. ; Adam, G.P. ; Williams, B.W. "Single-Phase Single-Stage Transformer less Grid-Connected PV System", *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2664-2676, June 2013.

[4] Breazeale, L.C. ; Ayyanar, R. "A Photovoltaic Array Transformer-Less Inverter With Film Capacitors and Silicon Carbide Transistors", *IEEE Transactions on Power Electronics*, vol. 30 , no. 3, pp. 1297-1305, March 2015 .

[5] Anand, S. ; Gundlapalli, S.K. ; Fernandes, B.G. "Transformer-Less Grid Feeding Current Source Inverter for Solar Photovoltaic System", *IEEE Transactions on Industrial Electronics*, vol. 61 , no. 10, pp.5334-5344, Oct 2014.

[6] Gonzalez, R.; Gubia, E.; Lopez, J.; Marroyo, L.; "Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter", *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp.2694-2702, July 2008.

[7] Schmidt, Heribert – European Patent Application, Pub No.03009882.6, Pub. Date: 15.05.2003

[8] Gonzalez, R.; Lopez, J.; Sanchis, P.; Marroyo, L, "Transformer-less Inverter for Single-Phase Photovoltaic Systems", *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp.693-697, March 2007.

[9] Matthias Victor – United States Patent Application, Pub No.US2005/0286281 A1, Pub. Date: 29 Dec 2005.

[10] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter", *IEEE Trans. Ind. Applicat.*, vol. 17, pp. 518–523, Sep./Oct. 1981,.

[11] Matsui, K. ; Kawata, Y. ; Ueda, F. "Application of parallel connected NPC-PWM inverters with multilevel modulation for AC motor drive ", *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp.901-907, Sep 2000.

[12] Barros, J.D. ; Silva, J.F.A. ; Jesus, E.G.A. "Fast-Predictive Optimal Control of NPC Multilevel Converters", *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp.619-627, Feb 2013.

[13] Li Zhang ; Kai Sun ; Lanlan Feng ; Hongfei Wu ; Yan Xing, "A Family of Neutral Point Clamped Full-Bridge Topologies for Transformerless Photovoltaic Grid-Tied Inverters", *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 730-739, Feb 2013.

[15] Jun Li ; Huang, A.Q. ; Zhigang Liang ; Bhattacharya, S. "Analysis and Design of Active NPC (ANPC) Inverters for Fault-Tolerant Operation of High-Power Electrical Drives", *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp.519-533, Feb 2012.

[16] Zaragoza, J.; Pou, J.; Ceballos, S.; Robles, E.; Jaen, C.; Corbalan, M.; "Voltage-Balance Compensator for a Carrier-Based Modulation in the Neutral-Point-Clamped Converter", *IEEE Transactions on Industrial Electronics*, vol. 56, no.2, pp.305-314, Feb. 2009.

[17] Wang, K. ; Xu, L. ; Zheng, Z. ; Li, Y. "Capacitor Voltage Balancing of a Five-Level ANPC Converter Using Phase-Shifted PWM", *IEEE Transactions on Power Electronics*, vol. 30 , no. 3, pp.1147-1156, March 2015.

[18] Wensheng Song ; Xiaoyun Feng ; Smedley, K.M. "A Carrier-Based PWM Strategy With the Offset Voltage Injection for Single-Phase Three-Level Neutral-Point-Clamped Converters", *IEEE Transactions on Power Electronics*, vol. 28 , no. 3, pp. 1083-1095, March 2013.

[19] Cobreces, S.; Bordonau, J.; Salaet, J.; Bueno, E.J.; Rodriguez, F.J.; "Exact Linearization Nonlinear Neutral-Point Voltage Control for Single-Phase Three-Level NPC Converters", *IEEE Transactions on Power Electronics*, vol. 24, no. 10, pp. 2357-2362, Oct 2009.

[20] Floricau, D. ; Floricau, E. ; Dumitrescu, M. "Natural doubling of the apparent switching frequency using three-level ANPC converter", *Non-sinusoidal Currents and Compensation, 2008. International School on ISNCC 2008.* , pp. 1-6.