ANALYSIS OF SOLAR POWER GENERATION WITH A MULTILEVEL INVERTER

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ABSTRACT

Abstract— In this paper a solar power generation system with a multilevel inverter, which is consist of a DC/DC power converter and a new grid connected solar seven-level pulse-width modulated (PWM) inverter. The DC/DC boost converter and a transformer to convert the output voltage of the solar cell into two self-determining voltage sources with numerous relationships integrate by DC/DC power converter. This new seven-level inverter is configured using a capacitor selection circuit and a full-bridge power converter, connected in cascaded. The capacitor selection circuit converts the two output voltage sources of DC/DC power converter into a three-level dc voltage, and the full-bridge power converter which further converts this three-level DC voltage into a seven-level AC voltage.

In this way, the proposed solar power generation system generates a sinusoidal output. This inverter consist of only six power electronics switch, and using only one power electronic switch is switched at high frequency at any time this is salient features of a project. A model is developed and tested to verify the performance of proposed solar power generation.

***Keywords— Grid-connected, multilevel inverter, pulse-width modulated (PWM)* inverter.**

1. INTRODUCTION

Now a day's many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power.

The energy of solar array is proving to be more essential as it creates less contamination and the cost of fossil energy increases, while the expense of solar panel exposures is diminished. The power conversion interface is important for grid-connected solar power systems because it converts DC power generated by a solar cell array into AC power and feeds AC power into the utility grid [1]. An inverter is required in the power conversion interface to convert DC power to AC power [2]. The power conversion efficiency of the power conversion interface is very important to ensure that there is no misuse of the energy produced by the solar cell array. In the inverter there is a loss due to the active device and the passive device. Power losses due to active devices include both conduction losses and switching losses. The loss of conduction results from the use of active devices, while the switching loss is proportional to the voltage and current changes for each switching and switching frequency. The voltage change in each switching operation for a multi-level inverter is reduced in order to improve its energy conversion efficiency. The rival of the switching harmonics is further attenuated, so that the loss of art caused by all the filter inductance is further reduced. Multi-level inverter must be designed at the highest voltage levels in order to recover conversion efficiency and reduce harmonic content [2].
The multilevel inverter normally has three types:

1) Cascaded H-Bridge Multilevel Inverter [3].
2) Flying Capacitor Multilevel Inverter [4].
3) Diode Clamped Multilevel Inverter [5].

In this type inverters are still used as capacitors to accumulate the different voltage levels [5]. However, it is difficult to control the voltage of these capacitors. Since it is difficult to generate voltage levels in both the diode and flying capacitor topologies [6]. The power circuit is difficult because of the increase in voltage levels that is essential for a multilevel inverter. For a seven-level inverter that uses twelve IGBT switches in both the diode clamped and flying capacitor network topologies [6]. The PWM cascade bridge must allow for many output voltage steps, so that the H-Bridge inverter in cascade the stages of tension. While in the circuit topology two H-bridge inverters among the multiple connection DC bus voltage and is connected in cascade mode to produce a seven-stage single phase inverter and also used an eight IGBT switches. However, in recent years different types of topologies are proposed for the seven-stage inverter [7]. For example, a single-phase seven-level inverter was developed for the solar power generation system. And this generation system is connected to the grid through a filter circuit

2. MULTILEVEL INVERTER

The power in the battery is in DC mode and the motor that drives the wheels usually uses AC power, therefore there should be a conversion from DC to AC by a power converter. Inverters can do this conversion; the simplest topology that can be used for this conversion is the two-level inverter that consists of four switches. Each switch needs an anti-parallel diode, so there should be also four anti parallel diodes. There are also other topologies for the inverters. A two-level Inverter creates two different voltage level for the load i.e. suppose we are providing V_{dc} as an input to a two level inverter then it will provide + $V_{dc}/2$ and – $V_{dc}/2$ on output. In order to build an AC voltage, these two newly generated voltages are usually switching by PWM.

Although this method of creating AC is effective but it has few drawbacks as it creates harmonic distortions in the output voltage, and also has a high dv/dt as compared to that of a multilevel inverter. Normally this method works, but in few applications it creates problems particularly those where low distortion in the output voltage is required.

The concept of multilevel Inverter (MLI) is kind of modification of two-level inverter. In multilevel inverters we don't deal with the two level voltage instead in order to create a smoother stepped output waveform, more than two voltage levels are combined together and the output waveform obtained in this case has lower dv/dt and also lower harmonic distortions [8]. Smoothness of the waveform is proportional to the voltage levels, as we increase the voltage level the waveform becomes smoother but the complexity of controller circuit is increase and components also increases along with the increased levels.

Figure 1: Block diagram of the proposed solar power generation system is composed of a solar cell array, a DC–DC power converter and a new seven-level inverter. The solar cell array is connected to the DC–DC power converter, through a proper solar tracking system, in this paper the perturb and observe maximum power point tracking method are used for extraction of the maximum power [9].The DC–DC power converter is a boost converter, The DC–DC power converter converts the output power of the solar cell array into two independent voltage sources with multiple relationships, which are supplied to the seven-level inverter [10]. This new seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, connected in a cascade. The output voltage of power inverter is to be a pure sinusoidal waveform with minimum total harmonic distortion. Energy dump are providing for this new seven level inverter for interfacing costumer to regulatory authority for selling and buying power, through NET Metering. The major issues for the control of the power inverters are to get suitable modulation methods to control the output rectangular waveforms to synthesize the desired waveforms. Therefore, a modulation control method is required to get a desired fundamental frequency voltage and to eliminate higher order harmonics as much as possible.

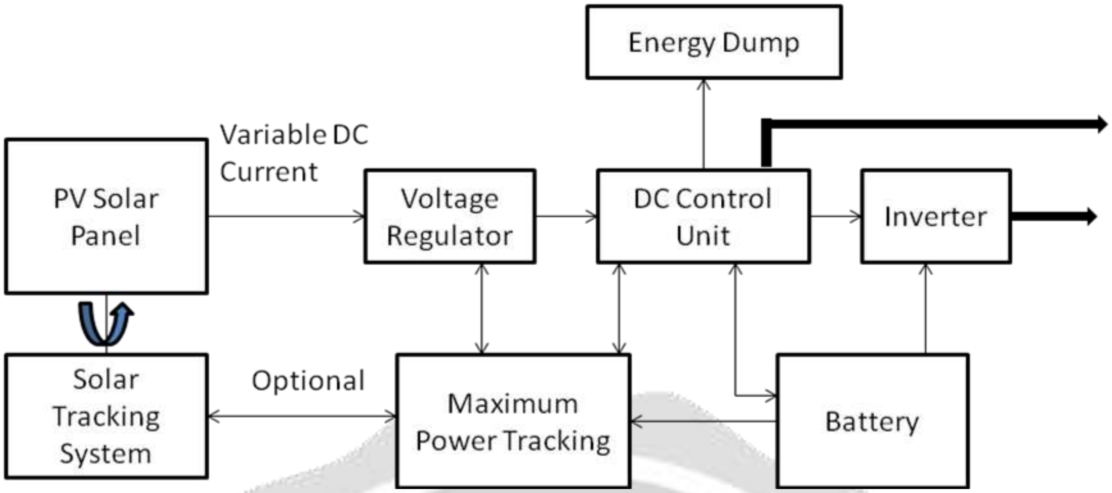


Fig-1: Block diagram of the system

3. CIRCUIT CONFIGURATION

Figure 2: shows the circuit diagram consist of solar cell array, DC-DC Boost converter and new seven level inverter. Solar cell array and the DC–DC power converter is a boost converter that incorporates a transformer with a turn ratio of 2:1. Capacitor C1 and C2 are connected across the H bridge inverter with a multiple relationship power electronic switches of capacitor selection circuit determine the discharge of the two capacitors, while the two capacitors are being discharged individually or in series. Because of the multiple relationships between the voltages of the DC capacitors, the capacitor selection circuit outputs a three-level DC voltage. The full-bridge power converter further converts this three-level DC voltage to a seven-level AC voltage that is synchronized with the utility voltage. In this way, the proposed solar power generation system generates a sinusoidal output current that is in phase with the utility voltage and is fed into the utility.

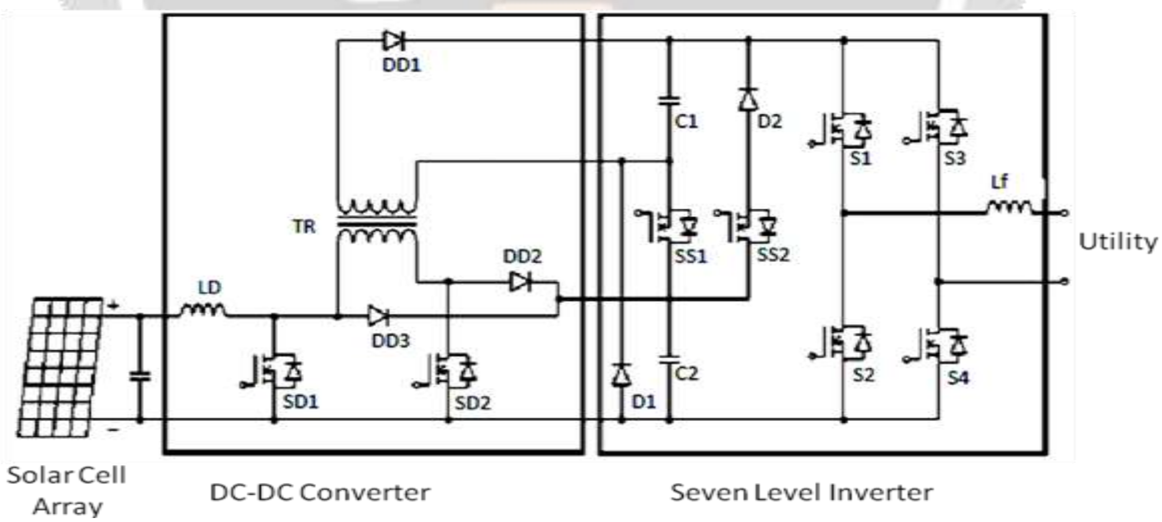


Fig- 2: Circuit diagram of the new seven level inverter [11].

The DC–DC power converter incorporates a boost converter and a current-fed forward converter. The boost converter is composed of an inductor LD, a power electronic Switch SD1, and a diode DD3. The boost converter charges capacitor C2 of the seven-level inverter. The current-fed forward converter is composed of an inductor LD, Power electronic switches SD1 and SD2, a transformer, and diodes DD1 and DD2. The current-fed forward converter charges capacitor C1of the seven-level inverter. The inductor LD and the power electronic switch SD1 of the current-fed forward converter are also used in the boost converter.

The operating circuit of the DC–DC power converter, when SD1 is turned ON, The solar cell array supplies energy to the inductor LD. When SD1 is turned OFF and SD2 is turned ON, capacitor C1 is connected to capacitor C2 in parallel through the transformer, so the energy of inductor LD and the solar cell array charge capacitor C2 through DD3 and charge capacitor C1 through the transformer and DD1 during the off state of SD1. Since capacitors C1 and C2 are charged in parallel by using the transformer, the voltage ratio of capacitors C1 andC2 is the same as the turn ratio (2:1) of the transformer. Therefore the voltages of C1 and C2 have multiple relationships. The boost converter is operated in the continuous conduction mode (CCM).

The voltage of C2 can be represented as,

$$V_{C2} = \frac{Vs}{1-D} \tag{1}$$

Where Vs the output voltage of solar cell array and D is the duty ratio of SD1, The voltage of capacitor C1 can be represented as,

$$V_{C1} = \frac{Vs}{2(1-D)} \tag{2}$$

It should be noted that the current of the magnetizing inductance of the transformer increases when SD2 is in the ON state. Conventionally, the forward converter needs a third demagnetizing winding in order to release the energy stored in the magnetizing inductance back to the power source. However, in the proposed DC–DC power converter, the energy stored in the magnetizing inductance is delivered to capacitor C2 through DD2 and SD1 when SD2 is turned OFF. Since the energy stored in the magnetizing inductance is transferred forward to the output capacitor C2 and not back to the DC source. The power efficiency is improved; in addition the power circuit is simplified because the charging circuits for capacitors C1 and C2 are integrated. Capacitors C1 and C2 are charged in parallel by using the transformer so their voltages automatically have multiple relationships, the control circuit are also simplified.

4. SEVEN LEVEL INVERTER.

Figure 2: the circuit configuration of seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, which are connected in cascade. The operation of the seven level inverter can be divided into the positive half cycle and the negative half cycle of the utility. For ease of analysis, the power electronic switches and diodes are assumed to be ideal, while the voltages of both capacitors C1 and C2 in the capacitor selection circuit are constant and equal to $V_{dc}/3$ and $2V_{dc}/3$ respectively. Since the output current of the solar power generation system will be controlled to be sinusoidal and in phase with the utility, the output current of the seven-level inverter is also positive in the positive half cycle of the utility. The operation of the seven-level inverter in the positive half cycle of the utility can be further divided into four modes:

Mode 1: Both SS1 and SS2 of the capacitor selection circuit are OFF, so C1 is discharged through D1 and the output voltage of the capacitor selection circuit is $V_{dc}/3$. S1 and S4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is directly equal to the output voltage of the capacitor selection circuit, which means the output voltage of the seven-level inverter is $V_{dc}/3$.

Mode 2: In the capacitor selection circuit, SS1 is OFF and SS2 is ON, so C2 is discharged through SS2 and D2 and the output voltage of the capacitor selection circuit is $2V_{dc}/3$, S1 and S4 of the full-bridge power converter are ON. At this point the output voltage of the seven-level inverter is $2V_{dc}/3$.

Mode 3: In the capacitor selection circuit SS1 is ON, Since D2 has a reverse bias when SS1 is ON, the state of SS2 cannot affect the current flow. Therefore, SS2 may be ON or OFF, to avoiding switching of SS2. Both C1 and C2 are discharged in series and the output voltage of the capacitor selection circuit is V_{dc} . S1 and S4 of the full-bridge power converter are ON. At this point the output voltage of the seven-level inverter is V_{dc} .

Mode 4: Both SS1 and SS2 of the capacitor selection circuit are OFF. The output voltage of the capacitor selection circuit is $V_{dc}/3$. Only S4 of the full-bridge power converter is ON, since the output current of the seven-level inverter is positive and passes through the filter inductor, it forces the anti parallel diode of S2 to be switched ON for continuous conduction of the filter inductor current. At this point the output voltage of the seven level inverter is zero. Therefore, in the positive half cycle, the output voltage of the seven-level inverter has four levels: V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, and 0,.In the negative half cycle the output current of the seven-level inverter is negative.

The operation of the seven-level inverter can also be further divided into four modes. Operation of the capacitor selection circuit in the negative half cycle is the same as that in the positive half cycle. The difference is that S2 and S3 of the full-bridge power converter are ON during modes 5, 6,and 7, and S2 is also ON during mode 8 of the negative half circuit is inverted by the full-bridge power converter, so the output voltage of the seven-level inverter also has four levels: $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$ and 0.In summary, the output voltage of the seven-level inverter has the voltage levels: V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}/3$, $-2V_{dc}/3$, and $-V_{dc}$.

5. CONTROL CIRCUIT

The proposed solar power generation system includes a DC-DC converter and a seven-level inverter. The seven-level inverter converts the DC power to high quality AC power and supplies it to the utility and regulates the voltages of capacitors C1 and C2. The DC-DC converter provides two independent voltage sources with multiple relationships and tracks a maximum power point (MPPT) to extract the maximum output power from the solar cell array.

Following figures Shows the model of the seven-level inverter under different range of utility voltage in the operating voltage range of smaller than V_{dc} /3 in the range of V_{dc} /3, to $2V_{dc}/3$ and the range of higher than $2V_{dc}$ /3.The seven-level inverter is controlled by the current-mode control, and pulse-width modulation (PWM) is use to generate the control signals for the power electronic switches. The output voltage of the seven-level inverter must be switched in two levels, according to the utility voltage. One level of the output voltage is higher than the utility voltage in order to increase the filter inductor current, and the other level of the output voltage is lower than the utility voltage, in order to decrease the filter inductor current. In this way, the output current of the seven-level inverter can be controlled to trace a reference current. Accordingly, the output voltage of the seven-level inverter must be changed in accordance with the utility voltage.

In the positive half cycle, when the utility voltage is smaller than $V_{dc}/3$, the seven-level inverter must be switched between modes 1 and 4 to output a voltage of $V_{dc}/3$ or 0. Within this voltage range, S1 is switched in PWM. The duty ratio d of S1 can be represented as the output voltage of first level is in between $V_{dc}/3$ and 0. Within this voltage range, S1 is switched in PWM. The duty ratio d of S1 can be represented as,

$$d = \frac{V_m}{V_{tri}} \qquad (3)$$

Where V_m and V_{tri} are the modulation signal and the amplitude of carrier signal in the PWM circuit respectively. The output voltage of the seven-level inverter can be written as,

$$V_0 = d \times \frac{V_{dc}}{3} = K_{pwm} \times V_m \qquad (4)$$

Where K_{pwm} is the gain of inverter which can be written as,

$$K_{pwm} = \frac{V_{dc}}{3V_{tri}} \tag{5}$$

Fig- 3 shows the simplified model of the seven-level inverter of utility voltage range smaller than V_{dc} /3.Theclosed loop transfer function can be derived as,

$$I_0 = \frac{K_{pwm} G_c / L_f}{s + K_i \times K_{pwm} G_c / L_f} I_0 - \frac{\frac{1}{L_f}}{s + \frac{K_i \times K_{pwm} G_c}{L_f}} V_u \tag{6}$$

Where G_c is the current controller and K_i is the gain of the current detector. The seven-level inverter is switched between modes 2 and 1, in order to output a voltage of $2V_{dc}/3$ or $V_{dc}/3$ when the utility voltage is in the range $V_{dc}/3$, $2V_{dc}/3$.Within this voltage range, SS2 is switched in PWM. The duty ratio of SS2 is the same as equation 3. However, the output voltage of seven-level inverter can be written as,

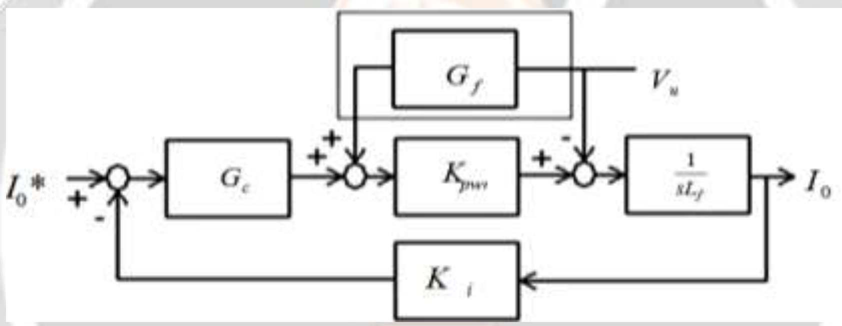


Fig- 3: Model of the seven-level inverter under different range of utility voltage in the range of smaller than $V_{dc}/3$.

Figure 4 shows the simplified model for the seven-level inverter when the utility voltage is within the voltage range of $V_{dc}/3$ **to** $2V_{dc}/3$. The closed-loop transfer function can be derived as

$$V_0 = d \times \frac{V_{dc}}{3} + \frac{V_{dc}}{3} = K_{pwm} \times \mathrm{V_m} + \frac{V_{dc}}{3} \tag{7}$$

$$I_0 = \frac{K_{pwm} G_c / L_f}{s + K_i \times K_{pwm} G_c / L_f} I_0 - \frac{\frac{1}{L_f}}{s + \frac{K_i \times K_{pwm} G_c}{L_f}} \left(V_u - \frac{V_{dc}}{3} \right) \tag{8}$$

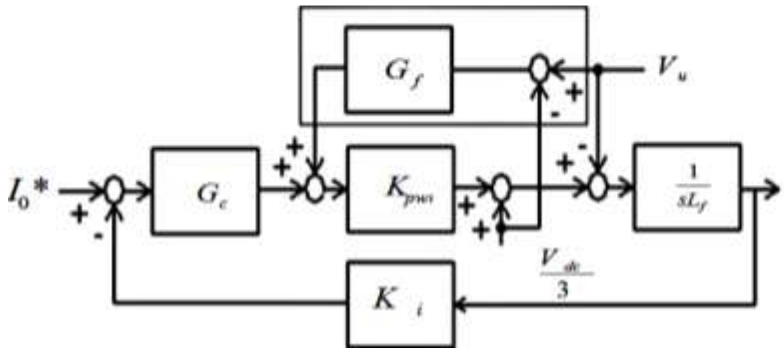


Fig 4: Model of the seven-level inverter under different range of utility voltage in the range of $V_{dc}/3$ to $2V_{dc}/3$.

The seven-level inverter is switched between modes 3 and 2 in order to output a voltage of V_{dc} or $2V_{dc}/3$, when the utility voltage is in the range $2V_{dc}/3$, V_{dc} Within this voltage range, SS1 is switched in PWM and SS2 remains in the ON state to avoid switching of SS2. The duty ratio of SS1 is the same as equation 3 However, the output voltage of seven-level inverter can be written as

Figure 5shows the simplified model for the seven-level inverter when the utility voltage is within the voltage range of $2V_{dc}/3$. The closed-loop transfer function can be derived as

$$V_0 = d \times \frac{V_{dc}}{3} + \frac{2V_{dc}}{3} = K_{pwm} \times V_m + \frac{2V_{dc}}{3} \tag{9}$$

$$I_0 = \frac{K_{pwm}G_c / L_f}{s + K_i \times K_{pwm}G_c / L_f} I_0 - \frac{\frac{1}{L_f}}{s + \frac{K_i \times K_{pwm}G_c}{L_f}} \left(V_u - \frac{2V_{dc}}{3} \right) \tag{10}$$

Equation 9 and equation 10 shows the output voltage and current respectively in a third level.

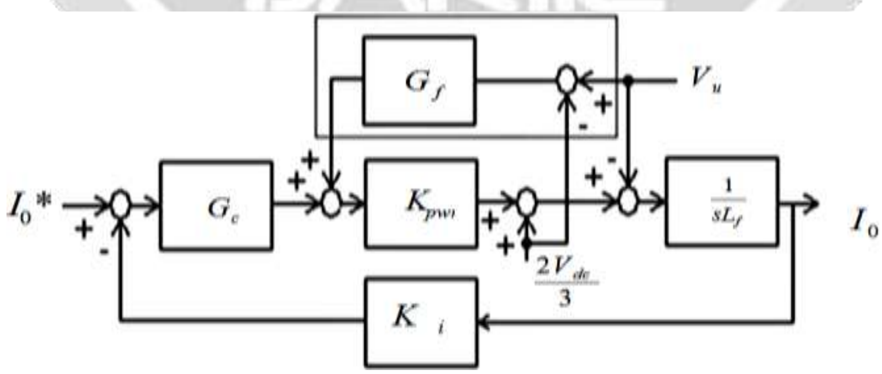
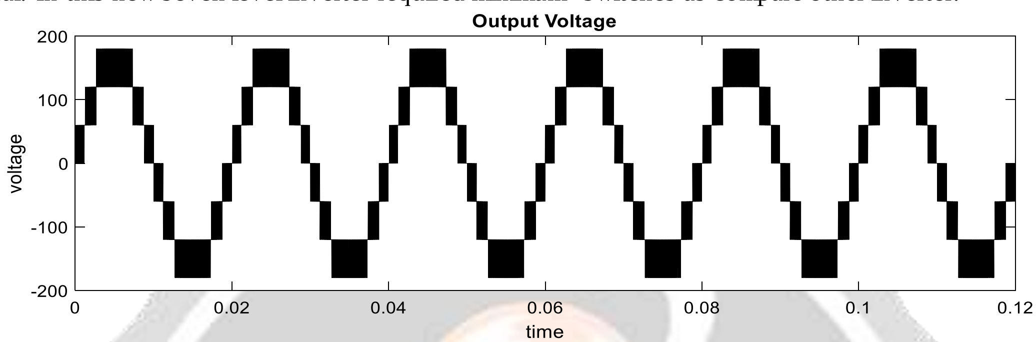


Fig- 5: Model of the seven-level inverter under different range of utility voltage in the range of higher than $2V_{dc}/3$.

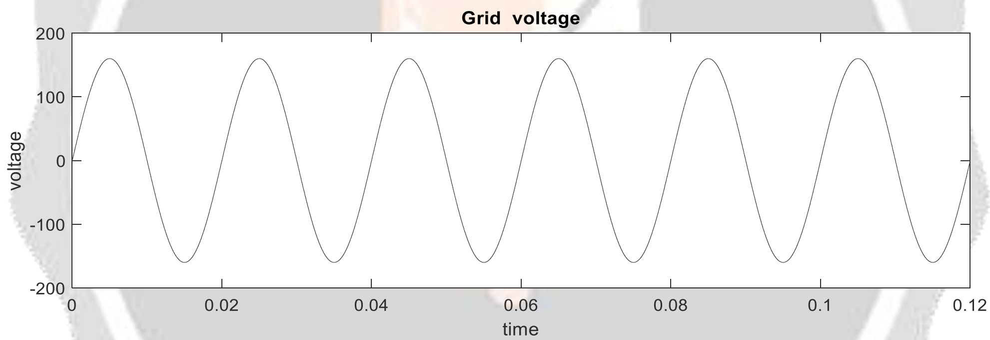
6. RESULT

To verify the performance of the proposed solar power generation system, a simulation model is developed and simulation result show's as follows.

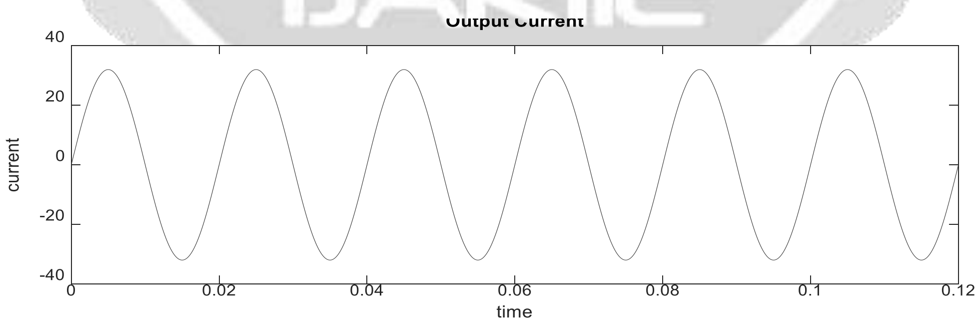
Figure 6: shows the seven level output voltage of inverter it is clearly seen that first wave shows the seven level voltage of inverter second and third wave indicate the grid voltage and output current waveforms respectively. From these waveforms it is clearly observed that at a time of conversion of DC to AC the output voltage waveforms is smooth as compare to the conventional two level inverter, due to step voltage this inverter have less losses. But if we increase the voltage level the number of requirement of switches are increase so up to seven levels it is economical. In this new seven level inverter required minimum switches as compare other inverter.



(a)



(b)

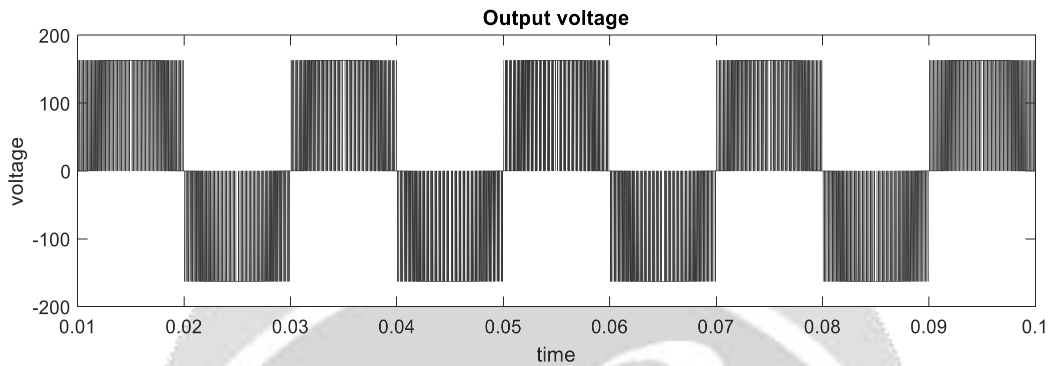


(C)

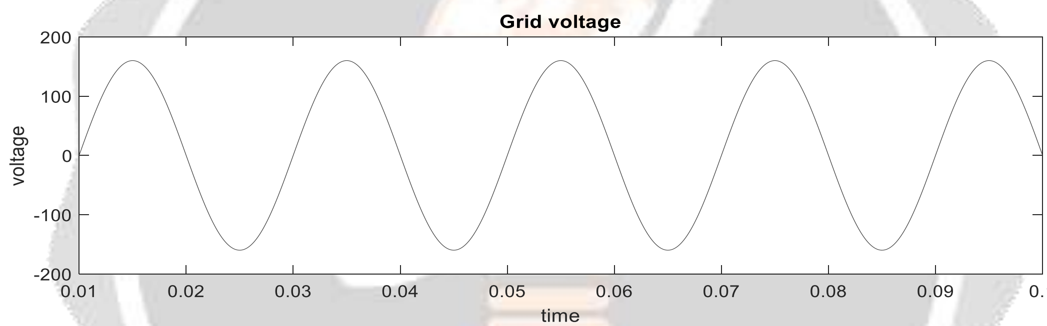
Fig- 6: the waveforms of new seven level inverter with closed loop control: (a) inverter output voltage, (b) grid voltage after filter, (c) output current.

Figure 7: shows the waveforms of conventional two level output voltage of the inverter with grid connected system, first wave of two stage voltage and second and third wave indicates the grid voltage and output current across the load. In a conventional two level inverter having only two output voltage levels due to that, at a

time of DC to AC conversion the inverter have some losses take place, due to that this inverter having less efficient than the new seven level inverter. When we comparing the efficiency of the both the inverter circuit then we observed that the efficiency of the new seven level inverter is above 94.16% and efficiency of the conventional two level inverter is of 91.23%.



(a)



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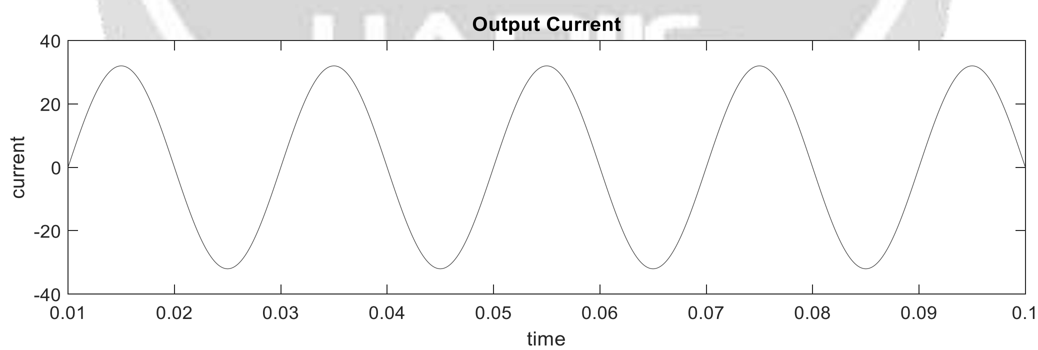

(c)

Fig- 7: The waveforms of conventional inverter with closed loop control :(a) inverter output voltage, (b) grid voltage after filter, (c) output current.

7. CONCLUSIONS

This seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. By using only one power electronic switch is operated at high frequency at any time to generate the seven-level output voltage. This may reduce the switching power loss and improves the power efficiency; it reduces the harmonic distortion of voltage and current. The voltages of the two capacitors in the proposed seven-level inverter will balance automatically due to grid connected system. And it is observed that the this solar power generation system seven level output voltage which is sinusoidal current and that is in phase with utility voltage, yield a power factor of unity. In addition, the proposed solar power generation system can effectively trace the maximum power of solar cell.

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9. REFERENCES

[1] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system,"IEEE Trans. Ind. Electron, Jun. 2011vol. 58, no. 6, pp. 2435–2443.

[2] R. A. Mastromauro, M. Liserre, and A. Dell'Aquila, "Control issues in single-stage photovoltaic systems: MPPT, current and voltage control,"IEEE Trans. Ind. Informat, May. 2012, vol. 8, no. 2, pp. 241–254,

[3] E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Control scheme of three-level NPC inverter for integration of renewable energy resources into AC grid," IEEE Syst. J, Jun. 2012 vol. 6, no. 2, pp. 242–253.

[4] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multi cell converter based on modified phase-shifted pulse width modulation," IEEE Trans. Power Electron, Jun. 2010,vol 25, no. 6, pp. 1517–1526.

[5] K. Hasegawa and H. Akagi, "Low-modulation-index operation of a five level diode-clamped pwm inverter with a dc-voltage-balancing circuit for a motor drive, IEEE Trans. Power Electron" Aug. 2012, vol.27, no.8, pp.3495–3505.

[6] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application.

[7] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics Converters, Applications and Design, Media Enhanced 2003, 3rd Ed, New York, NY, USA: Wiley.

[8] Manuj Rai, Dr. Ramesh Kumar Tripathi "A Novel Multilevel Inverter Topology with Selective Harmonic Elimination Technique", IEEETrans.978-1-4799-5912-9/2014

[9] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturband observe maximum power point tracking method,"IEEE Trans. Power Electronics. Jul. 2005, vol. 20, no. 4, pp. 963–973.

[10] Z. Zhao, M. Xu, Q. Chen, J. S. Jason Lai, and Y. H. Cho, "Derivation, analysis, and implementation of a boost–buck converter-based high-efficiency pv inverter," IEEE Trans. Power Electronics, Mar. 2012vol. 27, no. 3, pp. 1304–1313.

[11]Jinn-Chang Wu and Chia-Wei Chou "A Solar Power Generation System With a Seven-Level Inverter'', IEEE transactions on power electronics, JULY 2014,VOL. 29, NO. 7,