ANALYSIS OF VARIABLE FREQUENCY PWM TECHNIQUES FOR UNEQUAL VOLTAGE SOURCE MULTILEVEL INVERTER

V. Arun[1], R. Selvarasu[2], G.S. Arunkumar[3]

[1] *Associate Professor, Electrical and Electronics Engineering, Sree Vidyanikethan Engineering College, Andhra pradesh,India*

[2] *Professor, Electrical and Electronics Engineering, Sree Vidyanikethan Engineering College, Andhra pradesh,India*

[3] *Assistant Professor, Electrical and Electronics Engineering, Sree Vidyanikethan Engineering College, Andhra pradesh,India*

ABSTRACT

This paper represents a new topology of asymmetrical variable frequency multilevel inverters using trapezoidal reference. Seven level output are achieved by the Binary DC sources. The asymmetric inverter is triggered by Variable Frequency Unipolar Pulse Width Modulation (VFUPWM) methods using Phase Disposition (PD) strategy, Alternate Phase Opposition Disposition (APOD) strategy, and Carrier Overlapping (CO) strategy. The Performances measure like Total Harmonic Distortion (THD), Fundamental VRMS, Crest Factor (CF), Distortion Factor (DF) and Form Factor (FF) are estimated for different modulation indices. Simulation is performed by using MATLAB-SIMUINK. It is observed that VFUPDPWM method provides lower THD, VFUCOPWM method provides higher fundamental VRMS output voltage and Form Factor, and VFUAPODPWM method provides lower Distortion Factor

Keyword : - *Inverter, PWM, VFUPWM, THD.*

1. INTRODUCTION

Multilevel Inverter is developed to reduce the switching stress and to obtain the estimated output voltage with multiple steps without using a transformer and it achieved the lower Total Harmonic Distortion (THD) and increased fundamental VRMS. Multilevel inverters can operate at both fundamental switching frequency and high frequency switching PWM. Taghizadeh and Tarafdar Hagh [1] analyzed harmonic elimination of cascade multilevel inverters with non equal DC sources using particle swarm optimization. Fei et al [2] introduced a generalized half-wave symmetry SHE-pwm formulation for multilevel voltage inverters. Dixon et al [3] developed asymmetrical multilevel inverter for traction drives using only one DC supply. Khoucha et al [4] made a comparison of symmetrical and asymmetrical three-phase h-bridge multilevel inverter for DTC induction motor drives. Nguyen et al [5] introduced an optimized discontinuous pwm method to minimize switching loss for multilevel inverters. Li et al [6] analyzed a novel single-phase five-level inverter with coupled inductors. Roshankumar et al [7] developed a five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and a h-bridge. Hinago et al [8] introduced a switched-capacitor inverter using series / parallel conversion with inductive load. Zhang and Spencer [9] developed study of multisampled multilevel inverters to improve control performance. Batschauer et al [10] developed hybrid multilevel inverter based on half bridge modules. Cage et al [11] developed a phase disposition technique for parallel multilevel inverters. Hamzeh [12] et al integrating hybrid power source into an islanded mv microgrid using cascaded H- bridge multilevel inverter under unbalanced and nonlinear load conditions.

Mekhilef et al [13] developed digital control for three stage multilevel inverters. Rathore et al [14] developed optimal pulse width modulation of multilevel inverters for low-switching-frequency control of medium-voltage high-power industrial ac drives. Sepahvand et al [15] made capacitor voltage regulation in single-dc-source cascaded h-bridge multilevel converters using phase-shift modulation techniques. Babaei et al [16] developed multilevel inverter with series connection of novel H- bridge units. Mokhberdoran and Ajami [17] developed symmetric and asymmetric voltage source cascaded multilevel inverter. Kaliamoorthy et al [18] proposed hybrid switching topology for single-phase modular multilevel inverter. Farakhor et al [19] developed Symmetric and asymmetric transformer based cascaded multilevel inverter with minimum number of components. PrakashGautam et al [20] developed symmetrical multilevel inverter using less number of power electronic devices. Taghvaie et al [21] developed step up multilevel inverter with single DC source. Cheng-Han et al [22] designed and implemented a novel multilevel DC–AC inverter. Sandeep et al [23] designed and implemented a sensorless multilevel inverter with reduced parts.This paper proposed a single phase asymmetrical 7 level inverter with various VFUPWM switching methods. Simulations were developed using MATLAB - SIMULINK.

2. VARIABLE FREQUENCY ASYMENTRIC MULTILEVEL INVERTER

Fig. 1 shows proposed seven level asymmetrical multilevel inverter. The two half of the H-bridges are connected in series with different voltage ratings, in order to get the seven level output. The voltage levels are 0Vdc, Vdc, 2Vdc, 3Vdc, -Vdc, -2Vdc, -3Vdc. The switches S1, S2, S3 and S4 have the higher frequencies to get the positive polarity output levels. The switches A1, A2 and B1, B2 operate at the main fundamental frequency. The excepted output voltage levels become sum of the voltage in two half of the H-bridges. Here IGBT switches are used for simulation.

Excepted Output Voltage is calculated by the following formula:

$Vn = 2^{n+1}-1$, n = 1, 2, 4... n=number of dc sources.

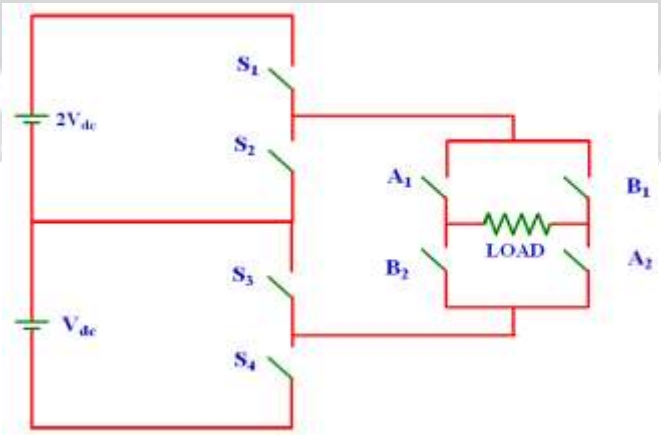

Fig -1: Proposed 7 level Asymmetrical Multilevel Inverter

3. VARIABLE FREQUENCY UNIPOLAR PWM METHODS

In this proposed work a unipolar trapezoidal reference with triangle carrier is used to generate firing pulses for a 7 level asymmetrical multilevel inverter. For that 7-level inverter, 3 carriers with the different frequencies (fc1, f c2) and same peak to peak amplitude Ac are used. The reference waveform has amplitude Am and frequency fm

and it is placed at the zero reference. The reference wave is sequentially compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are turned on. Otherwise, the device turned off.

There are many alternative strategies are available, some of them are worked in this paper and they are:

- Variable Frequency Unipolar Phase Disposition PWM method (VFUPDPWM).
- Variable Frequency Unipolar Alternative Phase Opposition Disposition PWM strategy (VFUAPODPWM).
- . Variable Frequency Unipolar Carrier Overlapping PWM strategy (VFUCOPWM).

The frequency ratio mf is as follows:

$$mf = fc / fm$$

The formula to be finds the amplitude modulation indices for UVFPD and UVFAPOD as follows:

$$ma= 2Am/ (m-1)Ac$$

3.1 Variable Frequency Unipolar Phase Disposition PWM (VFUPDPWM)

In VFUPDPWM strategy for a 7 level inverter, 3 carriers with the different frequency (2000Hz and 1000Hz) and same amplitude are arranged contiguous. The carrier arrangement for trapezoidal reference is shown in figures 2.

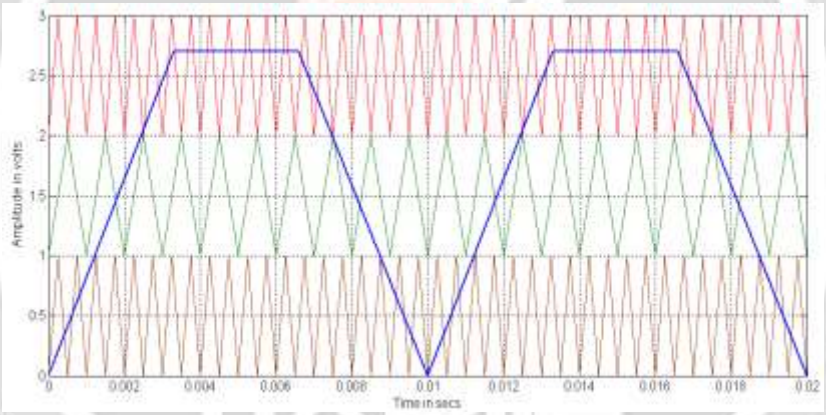

Fig 2: Carrier arrangement for VFUPDPWM method (ma = 0.9 and mf1=40, mf2=20)

3.2. Variable Frequency Unipolar Alternative Phase Opposition Disposition PWM (VFUAPODPWM)

In VFUAPODPWM method, the carriers of same amplitude are arranging in such a manner that each carriers is in out of phase with its neighbor by 180 degree. The carrier arrangement for trapezoidal reference which is shown in figures 3.

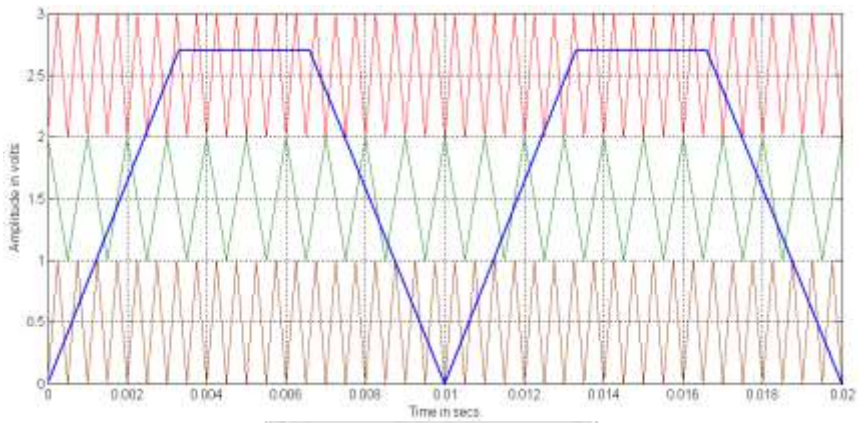

Fig 3: Carrier arrangement for VFUAPODPWM method (ma = 0.9 and mf1=40, mf2=20)

3.3. Variable Frequency Unipolar Carrier Overlapping PWM (VFUCOPWM)

The carriers are disposed such that the bands they occupy overlap each other, the overlapping vertical distance between each carrier is half of the peak to peak amplitude (AC/2). The carrier arrangement for trapezoidal reference which is shown in figures 4. The formula to find the amplitude modulation indices as follow:
ma= Am/ (2*Ac)

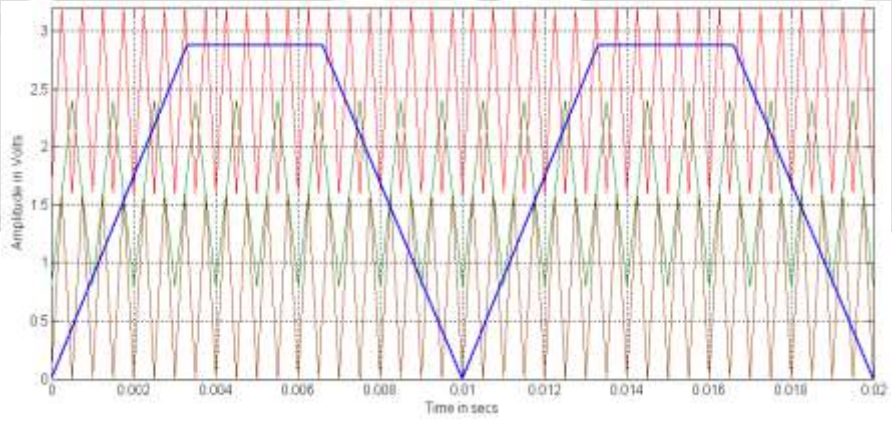

Fig 4: Carrier Arrangement for VFUCOPWM method (ma=0.9 and mf1=40, mf2=20)

4. SIMULATION RESULT

A single phase asymmetrical seven level inverter is simulated in SIMULINK using MATLAB software. Switching signals for asymmetrical multilevel inverter Variable Frequency Unipolar Pulse Width Modulation methods are simulated. Fig. 5 and 6 respectively represents the seven level output voltage generated by VFUPD method and its FFT plot. Fig. 7 and 8 respectively shows the 7 level output generated by VFUAPOD method and its FFT Plot. Fig. 9 and 10 deals the seven level output voltage generated by COUPWM method and its FFT plot. Simulations were carried out for different values of ma ranging from 0.8 to 1 and the corresponding %THD is measured using the FFT block and their values are shown in the Table 1. In that the VFUPDPWM method provides lower %THD. Next Table 2 represents the VRMS of the asymmetric inverter output for same modulation indices. In that VFUCOPWM method is found to perform better since it provides relatively higher fundamental RMS output voltage. Table 3 and Table 4 shows respectively the corresponding Crest Factor (CF) and Form Factor (FF) of the asymmetric inverter output voltage CF should be same for all PWM methods with different modulation indices and

VFUCOPWM method is found to higher Form Factor. Table 5 shows the Distortion Factor (DF) of the asymmetric inverter output voltage. In that VFUAPODPWM method provides less DF.

The following parameters values are used for simulation: VDC=100, R (load) = 100, fc1=2000 Hz, fc2 =1000 Hz and fm=50 Hz.

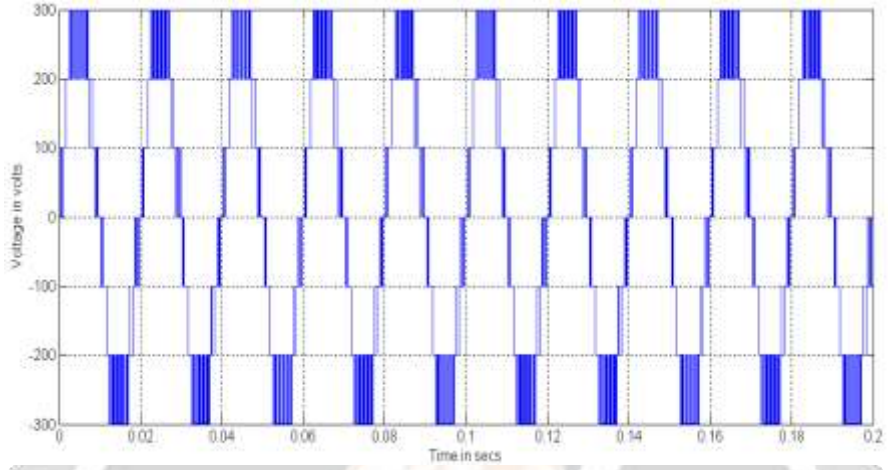

Fig 5: Output voltage generated by VFUPDPWM method

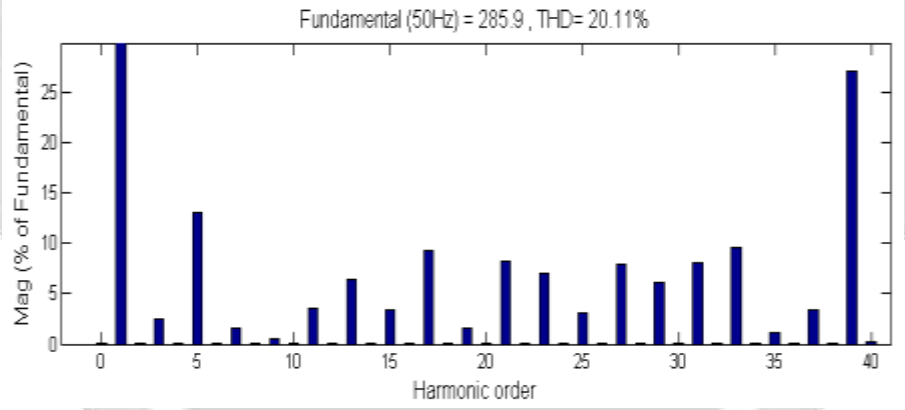

Fig 6: FFT plot for output voltage of VFUPDPWM method

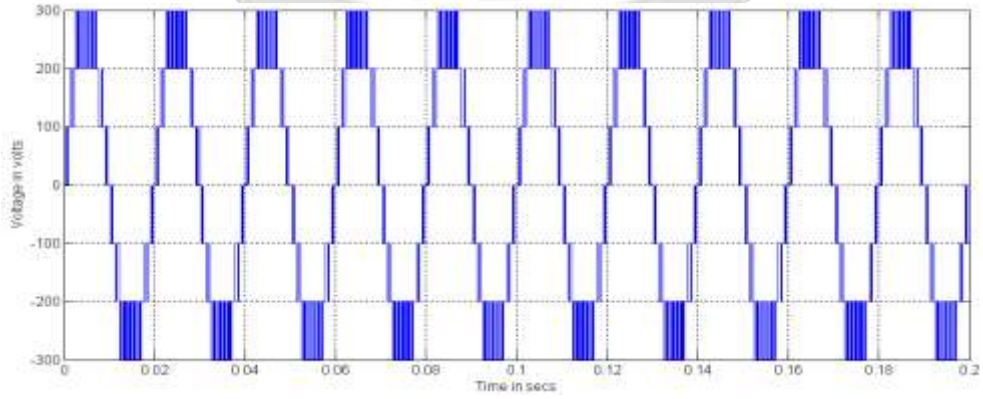

Fig 7: Output voltage generated by VFUAPODPWM method

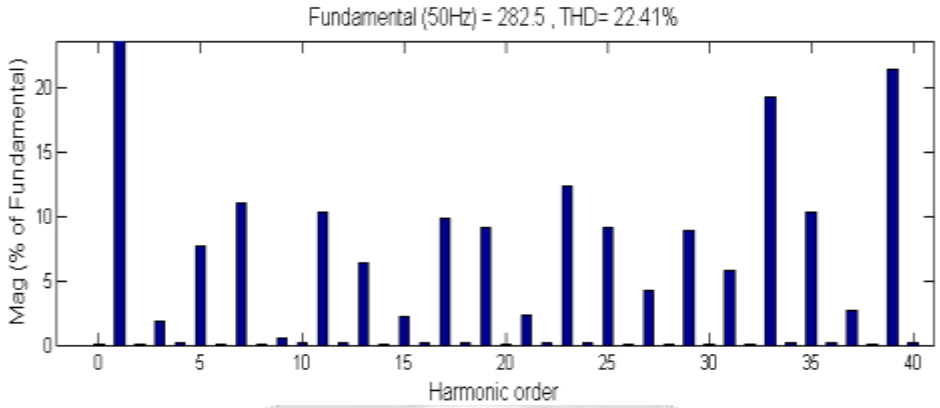

Fig 8: FFT plot for output voltage of VFUAPODPWM method

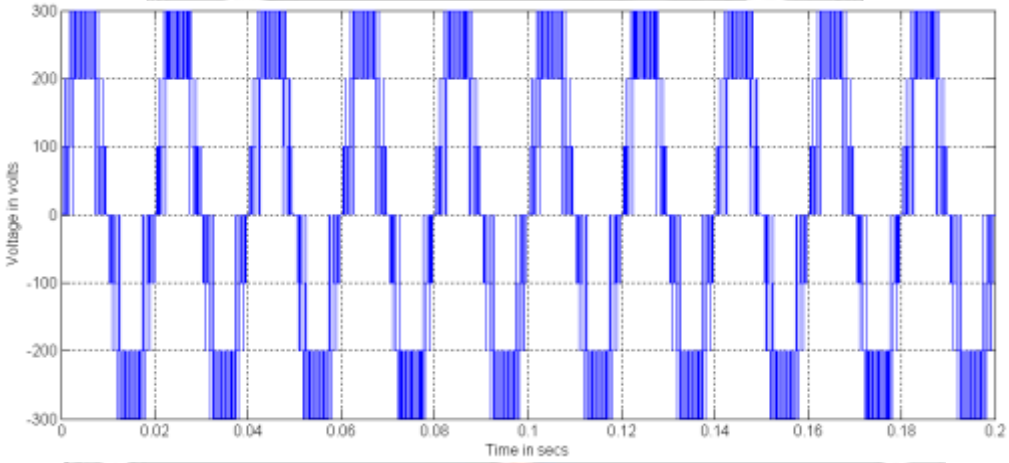

Fig 9: Output voltage generated by VFUCOPWM method

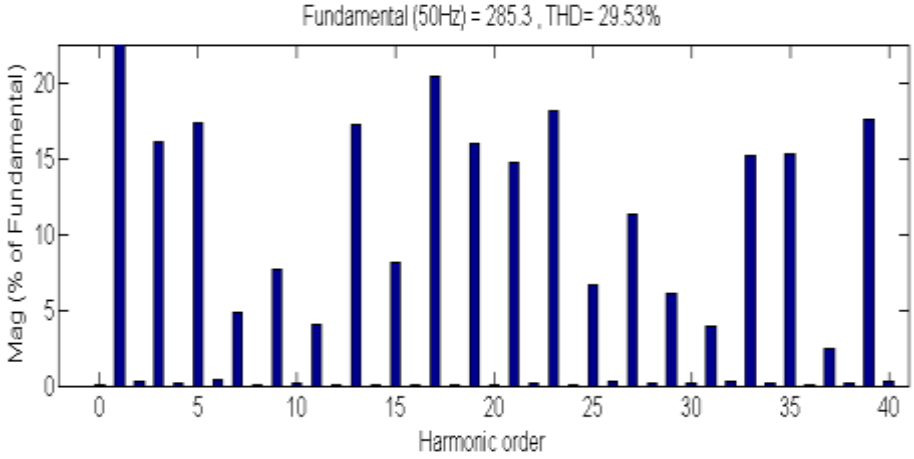

Fig 10: FFT plot for output voltage of VFUCOPWM method

Table 1. %THD for different modulation indices

ma	VFUPDPWM	VFUAPODPWM	VFUCOPWM
1	14.51	16.71	20.89
0.95	17.96	20.34	25.83
0.9	20.16	22.41	29.55
0.85	23.18	23.99	31.32
0.8	25.26	24.45	32.29

Table 2. VRMS for different modulation indices

ma	VFUPDPWM	VFUAPODPWM	VFUCOPWM
1	222.8	223.2	225.7
0.95	212.4	211.1	213.3
0.9	202	199.8	201.6
0.85	190.5	188.8	192.1
0.8	178.5	178.2	184.4

Table 3. Crest factor for different modulation indices

ma	VFUPDPWM	VFUAPODPWM	VFUCOPWM
1	1.414273	1.415247	1.414267
0.95	1.414313	1.414495	1.413971
0.9	1.414356	1.413914	1.414187
0.85	1.414173	1.414195	1.414368
0.8	1.414566	1.414141	1.414317

Table 4. Form factor for different modulation indices

ma	VFUPDPWM	VFUAPODPWM	VFUCOPWM
1	1.381E+09	9.184E+03	1.397E+09
0.95	1.364E+09	1.365E+09	1.416E+09
0.9	1.364E+09	8.307E+03	1.455E+09
0.85	1.361E+09	1.362E+09	5.198E+05
0.8	1.367E+09	1.366E+09	1.411E+09

Table 5. Distortion factor for different modulation indices

ma	VFUPDPWM	VFUAPODPWM	VFUCOPWM
1	0.002333229	0.00152	0.003391
0.95	0.002118568	0.001462	0.004295
0.9	0.002091908	0.00157	0.006623
0.85	0.001891779	0.001791	0.008771
0.8	0.001540165	0.002295	0.009445

For ma=0.9 it is observed from the figures [6, 8 and 10] the harmonic energy is dominant in: (a) 5th, 7th, 17th, 21st, 27th, 31st, 33rd and 39th orders in VFUPD method. (b) 5th, 7th, 11th, 17th, 19th, 23rd, 25th, 29th, 33rd, 35th and 39th orders in VFUAPOD method. (c) 3rd, 5th, 13th, 17th, 19th, 21st, 23rd, 27th, 33rd, 35th and 39th orders in VFUCO method.

5. CONCLUSIONS

In this paper, VFUPWM methods for asymmetrical seven level inverter have been presented. This multilevel inverter gives higher output voltage with reduced switch count and low harmonics. Performance factors like VRMS, %THD, DF, FF and CF have been estimated presented and analyzed. It is found that the VFUPDPWM method provides lower %THD. VFUCOPWM method is found to perform better since it provides relatively higher fundamental RMS output voltage and higher Form Factor. VFUAPODPWM method provides less DF.

6. REFERENCES

[1]. H.Taghizadeh and M. Tarafdar Hagh, "Harmonic Elimination of Cascade Multilevel Inverters with Nonequal DC Sources Using Particle Swarm Optimization," IEEE Transactions on Industrial Electronics, vol. 57, no. 11, pp. 3678–3684, 2010.

[2]. W. Fei, X. Du, and B. Wu, "A Generalized Half-Wave Symmetry SHE-PWM Formulation for Multilevel Voltage Inverters IEEE Transactions on Industrial Electronics,, vol. 57, no. 9, pp. 3030–3038, 2010.

[3]. J. Dixon, J. Pereda, C. Castillo, and S. Bosch, "Asymmetrical Multilevel Inverter for Traction Drives Using Only One DC Supply," IEEE Transactions On Vehicular Technology, vol. 59, no. 8, pp. 3736–3743, 2010.

[4]. F. Khoucha, M. S. Lagoun, A. Kheloui, and M. E. H. Benbouzid, "A Comparison of Symmetrical and Asymmetrical Three-Phase H-Bridge Multilevel Inverter for DTC InductionMotor Drives," IEEE Transactions On Energy Conversion, vol. 26, no. 1, pp. 64–72, 2011.

[5]. N. Nguyen, B. Nguyen, and H. Lee, "An Optimized Discontinuous PWM Method to Minimize Switching Loss for Multilevel Inverters," IEEE Transactions on Industrial Electronics, vol. 58, no. 9, pp. 3958–3966, 2011.

[6]. Z. Li, P. Wang, Y. Li, and F. Gao, "A Novel Single-Phase Five-Level Inverter With Coupled Inductors," IEEE Transactions on Power Electronics, vol. 27, no. 6, pp. 2716–2725, 2012.

[7]. P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A Five-Level Inverter Topology with Single-DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge," IEEE Transactions on Power Electronics,vol. 27, no. 8, pp. 3505–3512, 2012.

[8]. Y. Hinago and H. Koizumi, "A Switched-Capacitor Inverter Using Series / Parallel Conversion With Inductive Load," IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 878–887, 2012.

[9]. X. Zhang and J. W. Spencer, "Study of Multisampled Multilevel Inverters to Improve Control Performance," IEEE Transactions on Power Electronics, vol. 27, no. 11, pp. 4409–4416, 2012.

[10]. A.L. Batschauer, S. A. Mussa, and M. L. Heldwein, "Three-Phase Hybrid Multilevel Inverter Based on Half Bridge Modules," IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 668–678, 2012.

[11]. B.Cougo, G. Gateau, T. Meynard, M. Bobrowska-rafal, and M. Cousineau, "PD Modulation Scheme for Three-Phase Parallel Multilevel Inverters," IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 690–700, 2012.

[12]. M. Hamzeh, A. Ghazanfari, H. Mokhtari, and H. Karimi, "Integrating Hybrid Power Source Into an Islanded MV Microgrid Using CHB Multilevel Inverter Under Unbalanced and Nonlinear Load Conditions," IEEE Transactions On Energy Conversion, vol. 28, no. 3, pp. 643–651, 2013.

[13]. S. Mekhilef, M. N. A. Kadir, and Z. Salam, "Digital Control of Three Phase Three-Stage Hybrid Multilevel Inverter," IEEE Transactions on Industrial Electronics, vol. 9, no. 2, pp. 719–727, 2013.

[14]. A.K. Rathore, J. Holtz, and T. Boller, "Generalized Optimal Pulse Width Modulation of Multilevel Inverters for Low-Switching-Frequency Control of Medium-Voltage High-Power Industrial AC Drives," IEEE Transactions on Industrial Electronics, vol. 60, no. 10, pp. 4215–4224, 2013.

[15]. H. Sepahvand, J. Liao, M. Ferdowsi, and K. A. Corzine, "Capacitor Voltage Regulation in Single-DC-Source Cascaded H-Bridge Multilevel Converters Using Phase-Shift Modulation," IEEE Transactions on Industrial Electronics, vol. 60, no. 9, pp. 3619–3626, 2013.

[16]. E. Babaei, S. Laali, S. Alilu," Cascaded Multilevel Inverter With Series Connection of Novel H-Bridge Basic Units,"IEEE Transactions on Industrial Electronics, vol. 61, no. 12, pp. 6664 - 6671, 2014.

[17]. A.Mokhberdoran, A. Ajami," Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology," IEEE Transactions on Power Electronics, vol. 29, no. 12, pp. 6712 – 6724, 2014.

[18]. M. Kaliamoorthy, V. Rajasekaran, Irudayaraj Gerald Christopher Raj, and Lawrence Hubert Tony Raj, " Generalised hybrid switching topology for a single-phase modular multilevel inverter,"IET Power Electronics, vol. 7, no. 10, pp. 2472 - 2485, 2014.

[19]. A.Farakhor, Rouzbeh Reza Ahrabi, HosseinArdi, and S.N. Ravadanegh," Symmetric and asymmetric transformer based cascaded multilevel inverter with minimum number of components," IET Power Electronics, vol. 8, no. 6, pp. 1052 - 1060, 2015.

[20]. S. PrakashGautam, L. Kumar, S. Gupta," Hybrid topology of symmetrical multilevel inverter using less number of devices," IET Power Electronics, vol. 8, no. 11, pp. 2125 - 2135, 2015.

[21]. A. Taghvaie, J. Adabi, M. Rezanejad," Circuit Topology and Operation of a Step Up Multilevel Inverter With a Single DC Source," IEEE Transactions on Industrial Electronics, vol. 63, no. 11, pp. 6643 - 6652, 2016,

[22]. Cheng-Han Hsieh, Tsorng-Juu Liang, Shih-Ming Chen, Shih-Wen Tsai," Design and Implementation of a Novel Multilevel DC–AC Inverter," IEEE Transactions on Industry Applications, vol. 52, no., pp. 2436 - 2443, 2016.

[23]. N. Sandeep, R. Udaykumar, Yaragatti, "Design and Implementation of a Sensorless Multilevel Inverter With Reduced Part Count," IEEE Transactions on Power Electronics, vol. 32, no.9, pp. 6677 - 6683, 2017.