AN EFFICIENT VLSI ARCHITECTURE FOR IMAGE COMPRESSION USING DWT TECHNIQUE

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ABSTRACT

The modern real time applications related to image processing demand high performance discrete wavelet transform (DWT). The proposed architecture includes Line Buffers, PIPO and Lifting Block. This architecture works in non-separable fashion using a lifting scheme computes 1D, 2D and 3D-DWT at different resolution levels. The lifting scheme represents the fastest implementation of the DWT than the existing convolution based DWT. The proposed 3D-DWT achieves reduction in total area and net power respectively as compared with existing convolution DWT. The major objective of this work is to improve the performance of the DWT for DSP applications. The experimental results shows the proposed design requires less delay, area, and power dissipation than existing systems.

1. INTRODUCTION

1.1 Image Compression And Its Techniques

In these days, starting from family photos, satellite images to medical diagnosis images are stored on our computers. To get these images on the computer they must be transmitted over phone lines or other cables. When the images are larger it takes longer compression time and higher storage space. A common characteristic of most images is that the neighbouring pixels are correlated and therefore contain redundant information. Hence in order to remove that redundant information we have to detect less correlated pixels representation of the image. The main two components involved in compression are redundancy and irrelevancy reduction. In order to decrease the redundant information we go for the option of eliminating duplication from an image or a video. The reductions in irrelevancy eliminate the part of the image or video that will not be noticed by the signal receiver, namely the Human Visual System (HVS).

Thus the compression is obtained after removing one or more of three basic data redundancies: Coding redundancy, that are present only when code words used are less than optimal; Inter pixel redundancy, that occurs as a result due to the correlations between the pixels of an image; psycho visual redundancy which is due to data that is ignored by the human visual system. For many years, artificial neural networks (ANNs) have been studied and used to model information processing systems based on or inspired by biological neural structures. The artificial neural network results with solutions whose performance is better than that of traditional problem-solving methods, and also provides a clear understanding of human cognitive abilities.

1.2 Self Organisation Map

When comparing to several existing neural network architectures and learning algorithms, Kohonen's self-organizing map (SOM) is one of the most popular neural network models. This is mainly introduced for an associative memory model; it is one of the unsupervised learning algorithms with a simple structure and computational form. Self-organization is a fundamental pattern recognition process.

In turn SOM is also applicable to various other applications, like reducing dimensionality, data visualization, clustering and classification. Wavelet transform is the only method that provides both spatial and frequency domain information. The properties of wavelet transform gently helps in identification and selection

of significant and non-significant coefficients from among the wavelet coefficients. Image compression based on wavelet transform result in an improved compressed ratio as well as image quality and thus both the significant coefficients and their positions within an image are encoded and transmitted. In this paper a wavelet based image compression is applied to the result of the SOM based vector quantization.

1.3 VLSI Technology

With the rapid progress of VLSI design technologies, many processors based on audio and image signal processing have been developed recently. The discrete wavelet transform plays a major role in the JPEG-2000 image compression standard The Discrete Wavelet Transform (DWT) has become a very versatile signal processing tool. The advantage of DWT over other traditional transformations is that it performs multi resolution analysis of signals with localization both in time and frequency. Presently, research on the DWT is attracting a great deal of attention. In addition to audio and image compression the DWT has important applications in many areas, such as computer graphics, numerical analysis, radar target distinguishing and so forth. Discrete wavelet transform (DWT) has been widely used in many multimedia applications including video coding and various signal processing applications.

2. PROPOSED SYSTEM

In image processing, DWT can be used in image compression, image reconstruction, image coding, and Image fusion. In general, VLSI architecture for DWT is classified into two categories, they are

- Convolution based and
- Lifting based

2.1 DWT (Discrete Wavelet Transform) Convolution Based

DWT for image processing The DWT represents the signal in dynamic sub-band decomposition. Generation of the DWT in a wavelet packet allows sub-band analysis without the constraint of dynamic decomposition. The discrete wavelet packet transform (DWPT) performs an adaptive decomposition of frequency axis.

The Discrete Wavelet Transform (DWT), based on time-scale representation, provides efficient multi-resolution sub-band decomposition of signals. It has become a powerful tool for signal processing and finds numerous applications in various fields such as audio compression, pattern recognition, texture discrimination, computer graphics etc. Specifically the 2-D DWT and its counterpart 2- D Inverse DWT (IDWT) play a significant role in many image/video coding applications.

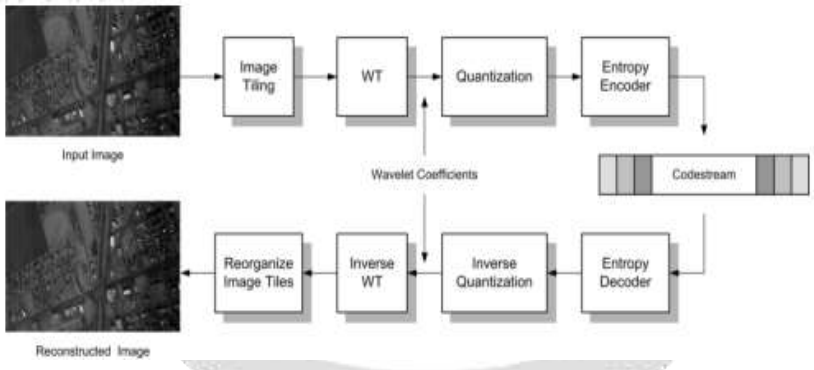

Fig -1 Block diagram of image processing

The Discrete Wavelet Transform (DWT), based on time-scale representation, provides efficient multi-resolution sub-band decomposition of signals that shown in fig 1. It has become a powerful tool for signal processing and finds numerous applications in various fields such as audio compression, pattern recognition, texture discrimination, computer graphichnhnhs etc.

2.2 Block Diagram

The low pass and high pass filters are represented as *H* and *G* respectively. Each filter output samples are decomposed down by the factor of 2. So, at each stage, the number of samples is equal to the half of the previous stage. Here, the input samples are *a*0, *a*1, *a7* and the number of input samples is 8. The coefficients of filter *G* are named as *g*0, *g*1, *g*2, and *g*3. The coefficients of filter *H* are *h*0, *h*1, *h*2, and *h*3.

So, the transfer functions of *G* and *H* can be written as

$$G(z)=g0+g1z-1+g2z-2+g3z-3 \quad (4.1)$$

$$H(z)=h0+h1z-1+h2z-2+h3z-3 \quad (4.2)$$

respectively. The equations (4.1) and (4.2) show the high pass and low pass filter outputs in *N*-point convolution based DWT respectively, where *P* is the length of the filter and *x* is input sample. The high pass and low pass

filter co-efficient are represented as *g* and *h* respectively. In Fig. 4.3, the first stage outputs b and c have 4 samples. The second stage outputs d and e have 2 samples. The last stage outputs f and f_ have one sample. The high pass outputs are given below.

2.3 Convolution based 2D-DWT

Here, the input signal sample values are represented as a N × N matrix. During the row process, each row of the input signal matrix is 1D transformed and the results are stored in N × N2 buffer. After completing all the N rows of input signal matrix, transpose matrix of the buffer is taken for column process.

In column process, each row of transposed buffer matrix is 1D transformed and results are the required 2D-transformed values. Fig. 3 shows the example for 2D-DWT with 3 levels of decomposition. Fig. 3 shows the 1D and 2D folded convolution based DWTs respectively.

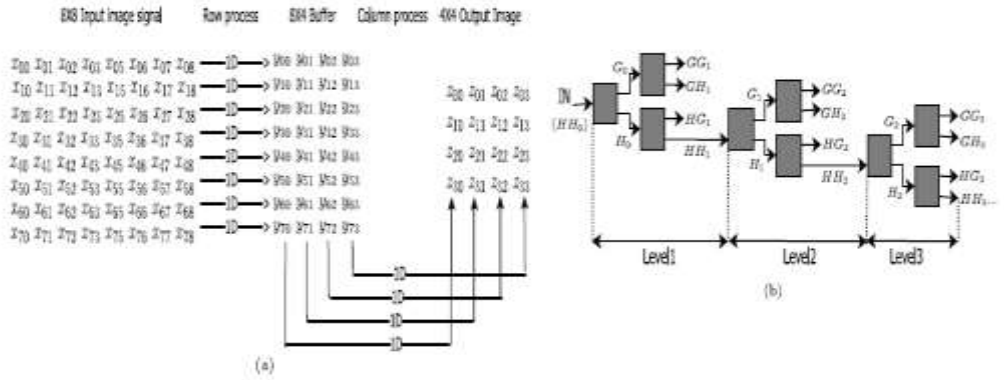

Fig -2 Convolution based 2D-DWT (a)8x8 image signal with 1 level decomposition and (b) Example: decomposition with 3 levels

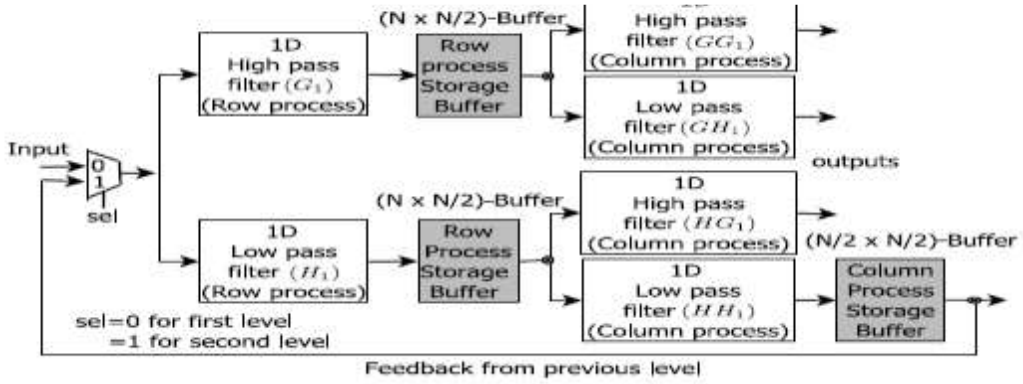

Fig -3 Convolution based folded 2D-DWT architecture

2.4 The Proposed Convolution Based Floating Point 2D-DWT Architecture

In this section, convolution based floating point 2D-discrete wavelet transform architecture is proposed, which is designed with floating point multiply accumulate circuit (MAC). The MAC operation can be defined as multiplication and repeated addition. Figure 5 shows proposed 8-point floating point high pass filter (*G*1) for convolution based 2D-DWT. Fig. 5 shows proposed 8-point floating point high pass filter (*G*1) for convolution based 2D-DWT. Here, one stage pipelined floating point MAC is used. If *in* = 0 then, MAC operations will be performed otherwise multiplication will be performed. The select lines *s*0 and *s*1 are used to select the proper inputs.

In general, the appropriate select lines of multiplexers are used to perform the required 1D-DWT using proposed architecture. Fig 5 shows the overall architecture of proposed 1D-DWT, where the select lines of multiplexers are stored in a lookup table with corresponding address. The *Addr* will be increased by one in every clock cycle and initially it is 0. The appropriate select lines *Sel*[*Addr*] are obtained from memory during each clock cycle to perform 1D-DWT.

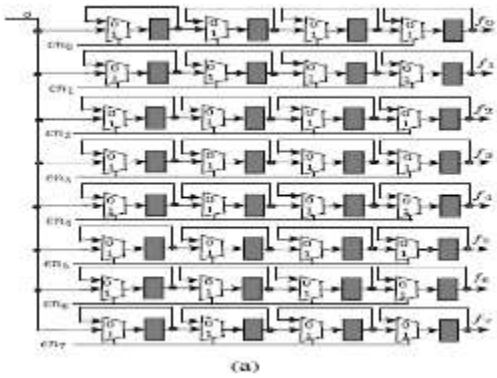

Fig -4 8 × 4-Buffer used for the row process in proposed floating point convolution based 8 × 8 2D-DWT with 2 levels

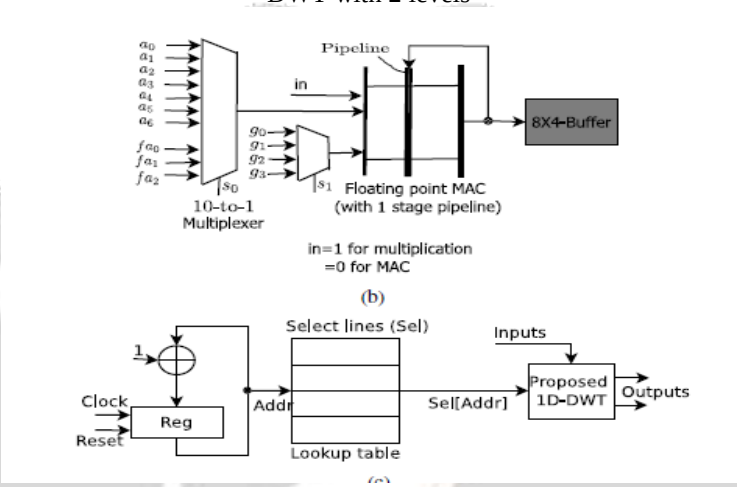

Fig -5 Proposed 8-point floating point high pass filter (*G*1) for convolution based 2D-DWT, and (c) Overall architecture of proposed 1D-DWT for 2D implementation.

In computing, especially digital signal processing, the multiply–accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known as a multiplier–accumulator (MAC, or MAC unit); the operation itself is also often called a MAC or a MAC operation. The MAC operation modifies an accumulator *a*: When done with floating point numbers, it might be performed with two rounding's (typical in many DSPs), or with a single rounding. When performed with a single rounding, it is called a fused multiply–add (FMA) or fused multiply–accumulate (FMAC). Modern computers may contain a dedicated MAC, consisting of a multiplier implemented in combinational logic followed by an adder and an accumulator register that stores the result. The output of the register is fed back to one input of the adder, so that on each clock cycle, the output of the multiplier is added to the register. Combinational multipliers require a large amount of logic, but can compute a product much more quickly than the method of shifting and adding typical of earlier computers. The first processors to be equipped with MAC units were digital signal processors, but the technique is now also common in general-purpose processors.

2.5 Proposed System (DWT –Lifting)

- This paper proposes the 3D- DWT using lifting scheme.
- The lifting scheme entirely relies on the spatial domain, has many advantages compared to filter bank structure, such as lower area, power consumption and computational complexity.
- The lifting scheme can be easily implemented by hardware due to its significantly reduced computations.
- Lifting has other advantages, such as "in-place" computation of the DWT, integer-to-integer wavelet transforms which are useful for lossless coding.

2.6 Backward Lifting Scheme

Wim Sweldens developed a lifting scheme for the construction of bi-orthogonal wavelets. The main feature of the lifting scheme is that all constructions are derived in the spatial domain. Lifting scheme is a

simple and an efficient algorithm to calculate wavelet transforms as a sequence of lifting steps as shown in the figure 6.

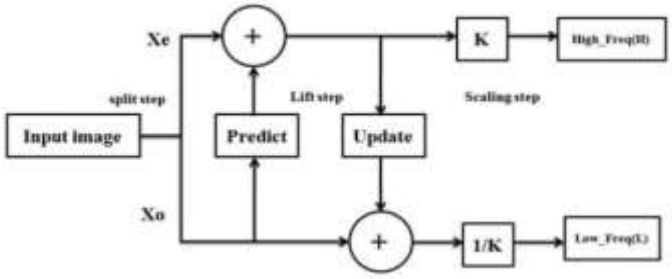

Fig -6 Backward lifting scheme using 5/3 wavelets transform

Constructing wavelets using lifting scheme comprises three steps:

1. Split step: The original signal, input image X (n), is split into odd and even samples.

2. Lifting step: This step is executed as N sub steps depending on the type of the filter, where the odd and even samples are filtered by the prediction and update filters, p(z) and u(z).

3. Normalization or Scaling step: After N lifting steps, scaling coefficients K and 1/K are applied respectively to the odd and even samples in order to obtain the low pass sub band i.e. significance coefficient YL (i) and the high-pass sub band i.e. detailed coefficient YH (i).

The proposed work is specialized for the DWT 5/3 wavelet in lifting scheme implementation. „X" be the input image, which has predefined pixels.

Let, $X = [X(1), X(2) \ldots X(2n)]$ be an array of length 2n (4.8)

In this work we begin with the "poly-phase decomposition," splitting X into two sub-bands, each of length N. the original signal

$$Xo = [X(1), X(3), X(5) \ldots X(2n-1)] \quad (4.9)$$

$$Xe = [X(2), X(4), X(6) \ldots X(2n)] \quad (4.10)$$

There are four stages in the lifting scheme architecture which is summarized by the equations as follows:

$$P1(n) = Xo(n) + a\,(Xe(n) + Xe(n+1)) \quad (4.11)$$

$$U1(n) = Xe(n) + b\,(P1(n) + Xe(n+1)) \quad (4.12)$$

$$dc(n) = k * P1(n) \quad (4.13)$$

sc(n) = 1/k * U1(n) P1(n) and U1(n) are scaled by the constant K and K-1 respectively, for normalizing their magnitude. Filter coefficients are described in table 1. The inverse transform is done by performing the lifting steps in the reverseorder and with a, b and k negated.

3. RESULTS

3.1 Input of DWT Blocks in Binary Form

Inputs of DWT blocks x of values 256 as shown in the figure 7

Fig -7 Input of DWT blocks

3.2 DWT-Convolutional Output:

DWT Convolutional outputs c is gets by compression of input x as shown in the figure 8.

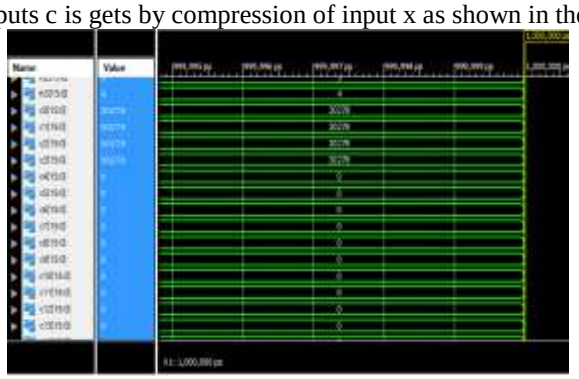

Fig -8 DWT Convolutional output

3.3 Design Summary And Timing Analysis

Number of Slices LUTs - 682 out of 5720 11%
Number of fully used LUT-FF pairs - 2 out of 682 0%
Number of bended IOBs - 68 out of 102 66%

The timing analysis of the DWT compression technique using the Lifting algorithm is 8.020 ns obtained in the DWT techniques.

3.4 Output Of MAC (Multiplier Accumulate Unit):

The output of the DWT convolutional using MAC is shown in the figure 9

Fig -9 Output of MAC

3.5 Design Summary And Timing Analysis

Number of Slices LUTs - 169 out of 5720 2%
Number of fully used LUT-FF pairs - 0 out of 169 0%
Number of bended IOBs – 48 out of 102 47%

The timing analysis of the DWT compression technique using the Convolutinal using MAC algorithm is 66.245 ns obtained in the DWT techniques.

3.6 DWT-Lifting Output

DWT lifting output c is shown in the figure 10.

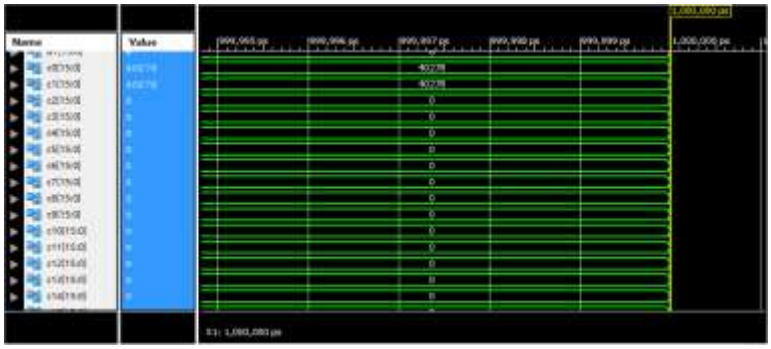

Fig -10 DWT-Lifting output

3.7 Design Summary And Timing Analysis

Number of Slices LUTs - 643 out of 2400 26%

Number of fully used LUT-FF pairs - 0 out of 643 0%

Number of bended IOBs – 881 out of 102 79%

The timing analysis of the DWT compression technique using the Lifting algorithm is 3.318 ns obtained in the DWT techniques.

3.8 Comparisons

The below table 1 shows the number of the components, LUT'S and slices, bounded IOB'S used in DCT and DWT techniques. It is clear that the proposed system uses less area than the previous system. This increases the speed and reduces the power consumption which is the major requirement in the processor applications. The comparison between area and delay clearly explains that area, power, delay is reduced.

Table -1 Comparison of DCT and DWT compression

PARAMETER	AREA ANALYSIS	TIMING ANALYSIS
DWT(CONVOLUTIONAL)	682 LUT's (decrease)	8.092 ns (decrease)
DWT(LIFTING)	643 LUT's (decrease)	3.381 ns (decrease)

4. CONCLUSION

From the above results, it is proved that from the DCT method of image compression, DWT techniques is efficient compression technique. And also the area consumption in DWT is smaller than the existing DCT technique. Comparing with the DWT techniques of lifting and convolutional method, lifting proves to be more efficient in terms of image compression, lesser area and less timing analysis.

5. REFERENCES

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