A High Performance CMOS Active Inductor

Disha M Kacha

[1] *Communication system engineer, Name of the Department, L.D.College of Engineering, Gujarat, India.*

ABSTRACT

A novel approach of CMOS active inductor, which can improve the quality factor and tuning range, was presented in this paper. A cascode grounded active inductor circuit topology and current mirror technique was presented, which can substantially improve its equivalent inductance, quality factor and tuning range. Further improvement in quality factor and inductance can be achieved by use of negative feedback network with cascode active inductor. These two active inductors were implemented by using 0.18-µm CMOS technology in cadence virtuoso IC6.1.6.Cascode active inductor design demonstrates a maximum quality factor 2.5k ,inductance 11.1nH at 4.9GHz and wide tuning range (6MHz-8GHz). The dc power consumption of this active inductor is 3.2mW. And negative feedback network-cascode active inductor design demonstrates a maximum quality factor 10k, inductance 18.29nH and wide tuning range (6.68 MHz-6.31 GHz). The dc power consumption of this active inductor is 4.1mW.

Keyword: - *CMOS active inductor, active inductor application, inductor, CMOS, cascoding topology.*

1. INTRODUCTION

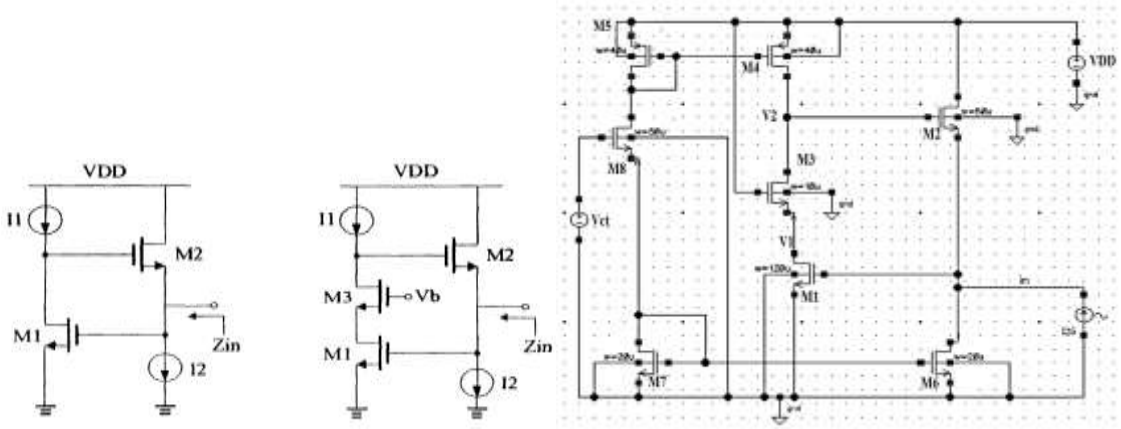
Traditionally, passive inductors are off-chip discrete component. The need for off-chip communication with these passive components severely limits the bandwidth, reduces the reliability, and increases the cost of systems. Since early 1990s, a significant effort has been made to fabricate inductors on a silicon substrate such that an entire wireless transceiver can be integrated on a single substrate monolithically. In the mean-time , the need for a large silicon area to fabricate spiral inductors has also sparked a great interest in and an intensive research on the synthesis of inductor using active devices , aiming at minimizing the silicon consumption subsequently the fabrication cost and improving the performance. The evolution of CMOS technology has allowed the integration of communication systems on a single chip. It deals with replacing the area consuming, lossy spiral inductors by gyrator based CMOS active inductors. Active inductor (AI) have found increasing application in high speed analog signal processing and data communications.

This includes implementation of cascode active inductor. This paper is organized as follow: Section II includes basic implementation of CMOS active inductor. Section III simulation results. Conclusion is shown in section IV.

2. IMPLEMENTATION OF ACTIVE INDUCTOR

The widely known one-port active inductor topology is the grounded active inductor which is based on "Gyrator theory" is shown in the figure 1(a). This architecture of active inductor generates several nH of inductance operating at a few GHz region.

As shown in figure 1(b) ,it is so called cascode grounded active inductor by adding a transistor M_3 on top of the M_1 .By minimizing g_{ds} (or g_0) in transistor M_3 ,the zero frequency of the active inductor can be decrease for the wider bandwidth application. Apart from this, cascode topology also offers attractive characteristics like quality factor improvement, no reduction in the inductance and upper bound of the frequency range.



(a) (b) (c)

Fig- 1: (a) grounded active inductor (b) cascode grounded active inductor (c) Schematic of cascode active inductor in cadence virtuoso

2.1 Cascode active inductor

Fig-1(c) shows schematic of proposed active inductor. As the input input voltage applies to the M_1 transistor, the transconductance g_{m1} converts the voltage to a drain current charging the capacitance C_{gs2} of transistor M_2. The voltage across C_{gs2} is then converted to the input current by the transconductance of M_2. Transistor M_3 is used as the gain boosting stage to improve Q factor of the active inductor, while the required bias currents for M_1 and M_2 are provided by the current mirrors M_4-M_7. Transistor M_8 generates the required bias current in saturation mode. Transistor $M_4 – M_7$ which are the current mirrors copy the current generated by transistor M_8. The key advantage of the current mirror is to generate multiple current branches with different amplitudes to different part of the circuits and eliminates the use of external supply for that part.From the small-signal analysis the node voltages V_1 and V_2 can be expressed as

$$V_1 = \frac{- g_{m1} V_{in}}{sC_{gs3} + g_{m3}} \quad (1)$$

$$V_2 = \frac{s^2C_{gs2} C_{gs3} + sC_{gs2}g_{m3} - g_{m1}g_{m3}}{S^2C_{gs2}C_{gs3} + sC_{gs2}g_{m3}+sC_{gs3}g_{ds4}+g_{m3}g_{ds4}} \quad (2)$$

and the input admittance of the active inductor at node in is given by

$$Y_{in}=1/Z_{in} \approx \frac{g_{m1}g_{m2}g_{m3}}{sC_{gs2}(g_{m3}+sC_{gs3})} + \frac{g_{m1}g_{m3}}{g_{m3}+sC_{gs3}} + sC_{gs1} \quad (3)$$

Assuming that the operating frequency of the active inductor is much lower than the cut-off frequency of M_3. The input admittance of can be written as

$$L \approx C_{gs2} / (g_{m1}g_{m2}) \quad (4)$$

$$R_s \approx -\omega^2C_{gs2}C_{gs3} / (g_{m1}g_{m2}g_{m3}) \quad (5)$$

$$G_p \approx g_{m1} \quad (6)$$

$$C_p \approx C_{gs1} \quad (7)$$

The value of the inductance L is determined by the small signal circuit parameters of M_1 and M_2, while the Q factor is strongly influenced by the values of G_p and R_s. G_p represents the shunt conductance,accounting for the loss of the active inductor. R_s is a negative resistance with frequency dependent characteristics. The resonant frequency of the active inductor is given by

$$f_{res} \approx 1/2\pi\sqrt{LC_p} \approx 1/2\pi\sqrt{\omega_{t1}\omega_{t2}} \quad (8)$$

note that the ω_{t1} and ω_{t2} are the cut-off frequencies of M_1 and M_2 respectively, which impose fundamental limitation on the operating frequencies of the active inductors. Generally, the active inductors are operated at frequencies lower than the resonant frequency to ensure the desirable circuit characteristics. The Quality factor of an active inductor can be approximated by

$$Q \approx \frac{\omega^2 C_{gs2} g_{m1} g_{m2} g^2_{m3}}{g_{m1} g_{m2} g^2_{m3} g_{ds4} + \omega^2 C_{gs2} g_{m1} g_{m3} (C_{gs2} g_{m3} - C_{gs3} g_{m2})} \quad (9)$$

Other than the reduced chip area and the enhanced Q factor, another advantage of using active inductor is the tuning capability of the inductance values. The value of the L is changed by the transconductance g_{m1} and g_{m2}. Hence, the inductance can be adjusted by the bias currents. However this is not very accurate for the active inductors operating in the large signal mode. The excess voltage swing leads to decrease in the transconductance of the transistors. Due to nonlinear characteristics inductance L deviates from its small signal value, resulting in undesirable signal distortion. Therefore, the impact of the linearity issues on the circuit performance should be carefully examined. For a CMOS active inductor using the cascode topology, the deviation in the transconductance due to large signal operation can be minimized by increasing the overdrive voltage and by reducing the transistor size at the expense of an elevated supply voltage.

2.2 Negative feedback network cascode active inductor

In cascode active inductor, we can improve quality factor by increasing the width of the transistor but it also introduce the high gate capacitance. The another way to improve quality factor is to use feedback resistance or negative feedback network which substantially improve quality factor without increasing width of transistors.

As shown in fig-2, It is a cascode active inductor with a negative feedback network consisting of R_1, R_2 and C_2. The parameter of this active inductor are given by

$$L = (C_3 + C_{gs2}) / g_{m1}\, g_{m2} \quad (10)$$

$$\omega_o = \sqrt{(g_{m1}\, g_{m2})} / (C_{gs1}\, (C_3 + C_{gs2}) \quad (11)$$

$$Q(\omega_o) = \sqrt{(g_{m1} g_{m2} (C_3 + C_{gs2}) / C_{gs1}\, g^2_{o1}} \quad (12)$$

It is seen from eq. that C3 is used to boost the inductance. It is also increases the quality factor and decreases the self-resonant frequency of the active inductor. The RC network consisting of R1,R2-C2 is negative feedback network that reduces the parasitic resistance of the active inductor.

A standard 0.18-µm CMOS process was employed for the circuit implementation, in order to characterize the small and large signal performance of the active inductors for RF applications.

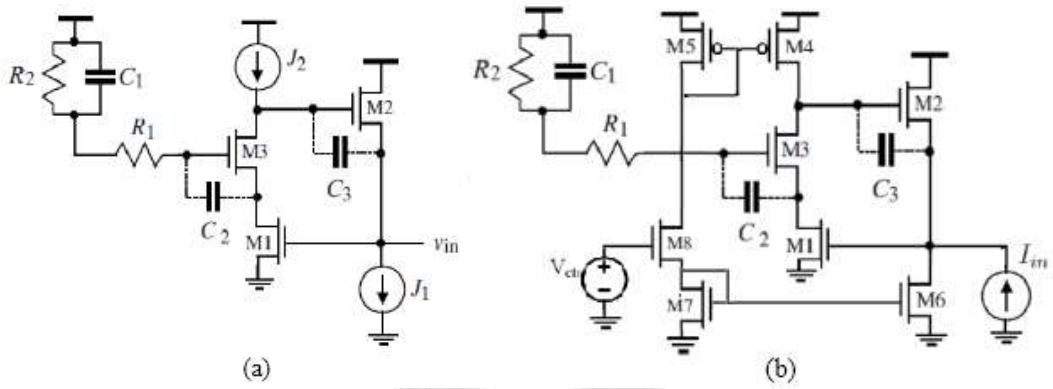


Fig-2 (a) schematic of negative feedback network cascode active inductor (b) schematic of negative feedback network cascode active inductor with current mirror

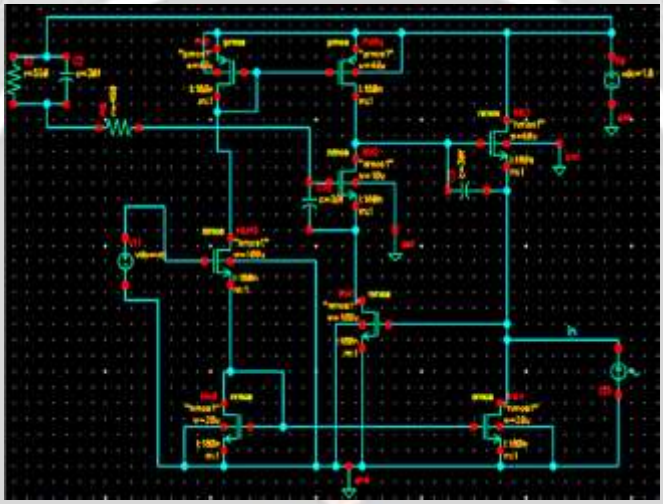


Fig -3 schematic of negative feedback network cascode active inductor in cadence virtuoso

3. SIMULATION RESULTS

3.1 Cascode active inductor

The equivalent inductance Leq is defined here as

$L_{eq} = I_m(Z_{in}) / \omega$ (10)

The experimental results are as follow

Table 1: Parameter of circuit

Transistors	W / L (μm /μm)
M_1	120/0.18
M_2	50/0.18
M_3	10/0.18
M_4	40/0.18
M_5	40/0.18
M_6	20/0.18
M_7	20/0.18
M_8	50/0.18

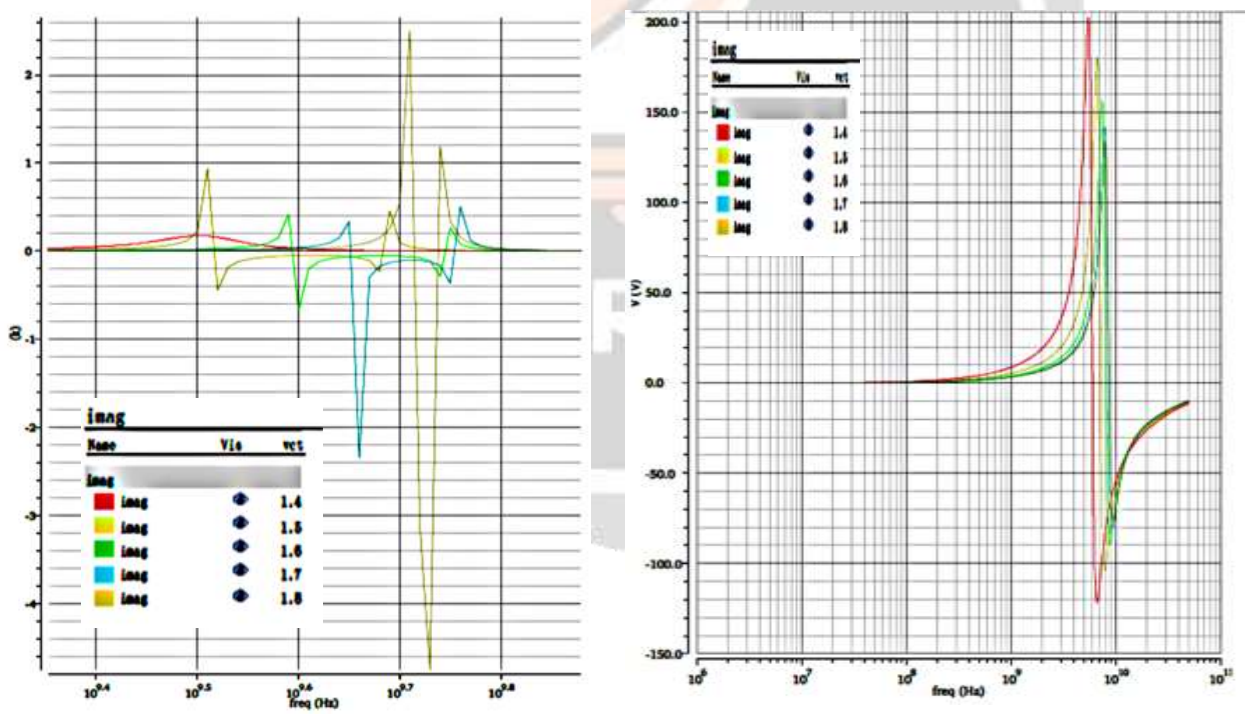
The circuit was simulated by using 0.18-µm CMOS process. The supply voltage of the tunable active inductor is 1.8 V and the power consumption is 3.2mW. With 1.8V bias voltage Vct, the maximum Quality factor is 2.5K,inductance is 11.1nH at 4.9GHz and the self-resonant frequency at 8.5GHz. By varying the bias voltage Vct of tunable active inductor, the inductance can be tuned from 5.9nH to 11.5nH.

3.2 Negative feedback network cascode active inductor

Design parameter and simulated results are as follow.

Table 2 : Parameter of circuit

Transistors	W / L (µm /µm)
M_1	50/0.18
M_2	60/0.18
M_3	10/0.18
M_4	40/0.18
M_5	40/0.18
M_6	40/0.18
M_7	40/0.18
M_8	100/0.18
R1 = R2 = 450 Ω , C1 = C2 = C3 = 30 f F	



(a) (b)

Fig -4 (a) Quality factor of cascode active inductor for different control voltage Vct (range 1.4 ~ 1.8 V) (b) simulated inductance value of cascode active inductor for different control voltage Vct (range 1.4 ~ 1.8 V)

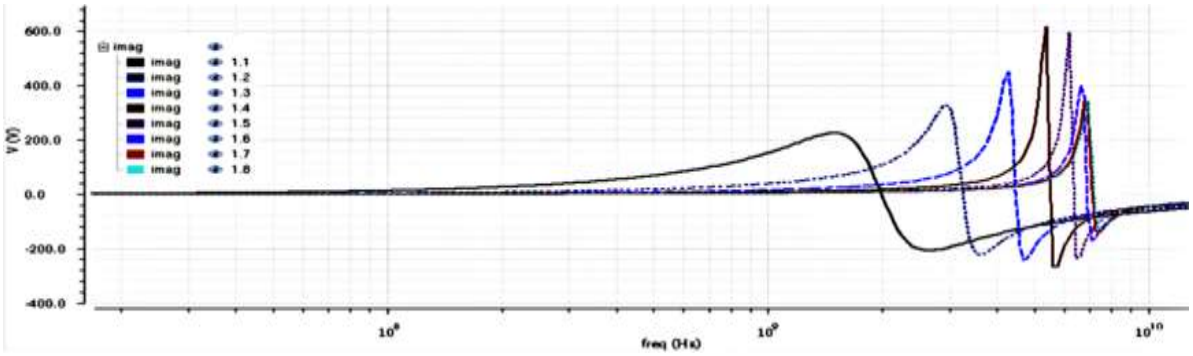


Fig -5 simulated inductance value of negative feedback network cascode active inductor for different control voltage Vct (range 1.1 ~ 1.8 V)

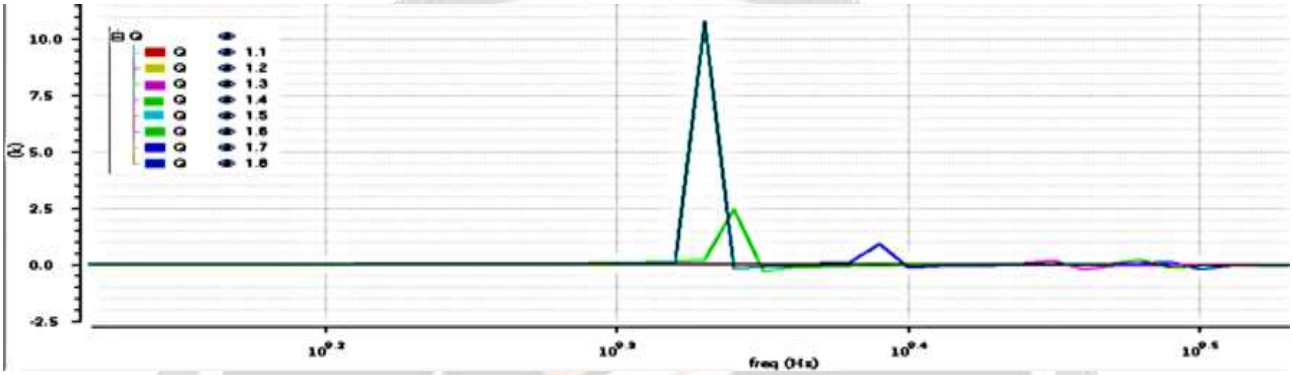


Fig -6 Quality factor of negative feedback network cascode active inductor for different control voltage Vct (range 1.1 ~ 1.8 V)

Table 3: Performance comparison of CMOS active inductor

Ref./Paper	[3]	[4]	[5]	[6]	This work	
					(a)	(b)
Tech.(μm)	0.18	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)	1.8	1.8	1.8	1.8	1.8	1.8
Freq. range	1-2 GHz	1-5 GHz	1-5 GHz	1-6 GHz	6MHz-8GHz	6.68 MHz – 6.31 GHz
L_{max} (nH)	27	35	22.4	15	11.1	18.29
Q-factor	28	68	500	50	2500	10k
P_{DC}(mW)	4	3.6	4.5	4.1	3.2	4.1

The negative feedback network-cascode active inductor circuit was also simulated by using 0.18-μm CMOS process. The supply voltage of the tunable active inductor is 1.8 V and the power consumption is 4.1mW. With 1.5V bias voltage Vct, the maximum Quality factor is 10K, inductance is 11.1nH and the self-resonant frequency at 6.31 GHz. By varying the bias voltage Vct of tunable active inductor, the inductance can be tuned from 7nH to 18.29nH. hence this topology improves quality factor and inductance but decreases tuning range.

4. CONCLUSION

A new high Q and wide tuning range, grounding active inductor was presented in this paper. The proposed active inductor was designed on gyrator-C topology. The use of cascading topology and negative feedback network-cascode active inductor makes it more attractive for high quality factor, inductance and wide tuning range. The tuneable cascode active inductor generates inductance between 1.6-11.1nH with the quality factor > 400 whereas the negative feedback network-cascode active inductor generates inductance between 7-18.29 nH and quality factor up to 10k. The results show that the circuit can be used in RF applications such as RF bandpass filter, trans receiver, oscillators and PLL.

6. REFERENCES

[1] Fei Yuan,"CMOS Active Inductors and transformers- Principle,Implementation, and Application" , Springer,dec.31,2007.

[2] L.-H.Lu,H.-H. Hsieh,and Y.-T.Liao, "A wide tuning-range CMOS VCO with a differential tunable active inductor", IEEE Trans. Microw. Theory Tech., vol. 54, no. 9,pp. 3462-3468,Sep. 2006.

[3] K. Hwang, C. Cho,J. Lee, and J. Kim, "High quality-factor andinductance of symmetric differential-pair structure active inductor using a feedback resistance design," IEEE International Microwave Symposium Digest,pp. 1059-1062,2008

[4] Lai. Q and Mao. J ,"A new floating active inductor using resistive feedback technique,"in IEEE International Microwave Symposium Digest, pp. 1748-1751,2010

[5] H. Feng and K.Mouthaan,"Lossless CMOS active reciprocal two-port inductor and application in a series LC filter," in European Microw. Conf, pp. 364-367,2012

[6] Chien-Cheng Wei, Hsien-Chin Chiu, and Wu-Shiung Feng," An Ultra-Wideband CMOS VCO with 3-5GHz Tuning Range",IEEE International Workshop on Radio-Frequency Integration Technology, , Singapore ,Nov 30-Dec 02, 2005.

[7] Chao-Chih Hsiao, Chin-Wei Kuo, Chien-Chih Ho, and Yi-Jen Chan," Improved Quality-Factor of 0.18-µm CMOS Active Inductor by

Feedback Resistance Design", IEEE Microwave and Wireless Components Letters, vol. 12, no. 12, Dec ,2002.

[8] M. Nair, Y. Zheng, and Y. Lian. "An active inductor based low-power UWB LNA".Proc. Int'l Conf. Ultra Wideband, pages 813–816, Sept. 2007.

BIOGRAPHIES (Not Essential)

Student of master of engineering in communication system engineering at L.D.College of Engineering, Ahmedabad, Gujarat.