A NEW TOPOLOGY OF MULTIPORT ASYMMETRIC SEVEN LEVEL INVERTER USING FUZZY LOGIC CONTROLLER

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ABSTRACT

In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three-level Pulse Width-modulated (PWM) inverters. They offer improved output waveforms, smaller filter size, lower Electromagenetic Interference(EMI),lower Total Harmonic Distortion (THD) and others. In this Project, switched-capacitor multilevel inverter with fuzzy logic control is proposed. The proposed cascaded multilevel inverter work with asymmetric DC voltage sources and needs lower number of power semiconductor switches hence the complexity and the cost of the overall system decreases. Pulses for the switches are generated by using fuzzy rule based pulse width modulation. Procedure to generate voltage levels is developed. The inverter inherently solves the problem of capacitor voltage balancing as each capacitor is charged to the value equal to one of input voltage every cycle. The rules of the FLC will control the amplitude of the PWM sine wave with respect to the error voltage. The seven level MLIs offers improved performance with FLC when compare with conventional inverters .

Keywords – *Fuzzy logic controller, switched capacitor multilevel inverter*

1. INTRODUCTION

Multilevel inverter with large number of steps can generate high quality voltage waveforms, good enough to be considered as suitable voltage source generator. Multilevel Inverters [MLI] produce a stepped output phase voltage with a refined harmonic profile when compared to a two-level inverter. The concept of multilevel inverters, introduced about 30 years ago, entails performing power conversion in multiple voltage steps to obtain power quality. Three commercial topologies of multilevel voltage source inverters are the most popular being the diode-clamped, flying capacitor and cascaded H- bridge structures. Among these inverter topologies, the cascaded H-bridge multilevel inverters require the least number of total main components. Multilevel Inverters [MLI] has the capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion and asymmetrical multilevel inverters can be obtained. Asymmetric multilevel have the same topology as symmetric multilevel inverters. They differ only in the rating of input dc voltages and control strategies. For many applications it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, a scheme is proposed which uses lesser number of bridges. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high-power application

2. BLOCK DIAGRAM OF PROPOSED SYSTEM

Figure 1 shows the block diagram of seven level switched capacitor multilevel inverter with asymmetric input sources. Switched capacitor multilevel inverter with fuzzy loop control is used. Two asymmetric dc sources is given to the multilevel inverter .The pulses for the switches are generated by using fuzzy rule based pulse width modulation. Each capacitor is charged to a value equal to one of the input voltage every cycle. The rules of the FLC will control the amplitude of the PWM sine wave with respect to error voltage generated by the load. Thus, they offer a improved performance of output voltage with reduced harmonic distortion and lower number of switching devices.

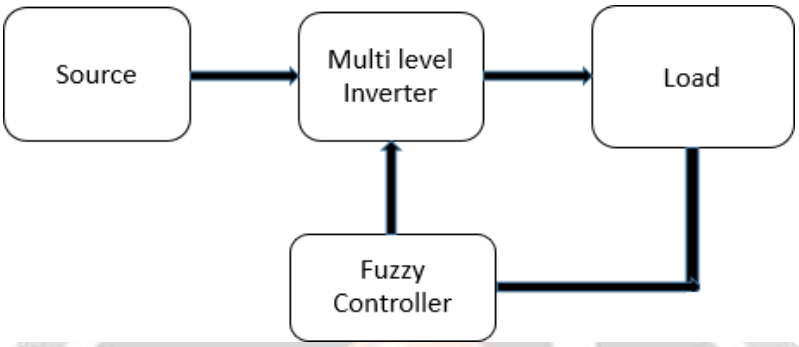

Fig-1: Block diagram of multiport asymmetric seven level inverter using fuzzy logic controller

3. CIRCUIT DIAGRAM

Figure 2 shows the block diagram of 7 level Switched Capacitor Multilevel Inverter. It consists of a SC based DC-DC converter which employs two input sources (Vin0 and Vin1), three transistors (S1a, S1b, and S1c), two diodes (D1a and D1b) and a capacitor (C1).SC DC-DC convert input voltage to integral multiple output levels without utilizing inductors .DC levels obtained at the inverter DC bus include Vin0, Vin1, Vin0+Vin1.The common feature in all Switched Capacitor Multilevel Inverter topologies is the back –end H –Bridge inverter. The H-bridge inverter employing transistors Q1 to Q4 effectively produces 6 bipolar levels and a zero (0, ±Vin0,±Vin1,±(vin0 + Vin1))across the load. For primary analysis, it is assumed that the switches and the voltage sources employed are ideal, capacitance is large enough to maintain a constant voltage and supply constant output current and the voltage ripple across them is small enough to be neglected. Number of output levels can be enhanced by increasing the number of input voltage sources, SC and power switches in the front end converter .It has four modes of operation. Table 1 explains the switching logic of the 7 level switched capacitor multilevel inverter.

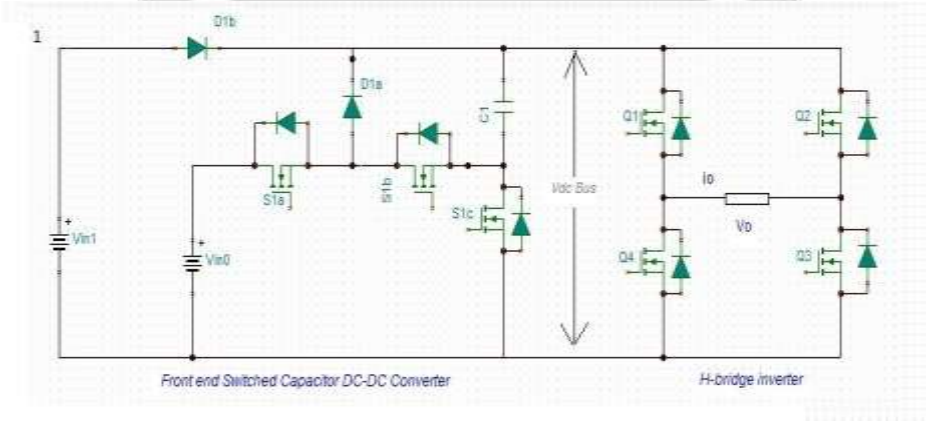

Fig-2: Circuit diagram of 7 level Switched Capacitor Multilevel Inverter

4. PROPOSED TOPOLOGY AND OPERATING PRINCIPLE

4.1 Output voltage =V_{IN1} state

Capacitor C_1, is charged to the input voltage V_{IN1} through D_{1b} by turning ON transistor S_{1c}. Transistors S_{1a}, S_{1b} and diode D_{1a} remain turned OFF. The DC bus voltage at this state is equal to V_{IN1} as V_{IN0} is blocked by turning OFF transistor S_{1a}. Voltage source V_{IN1} alone supplies power to the load. Fig 3 depicts the equivalent circuit for $V_0 = +V_{IN1}$.

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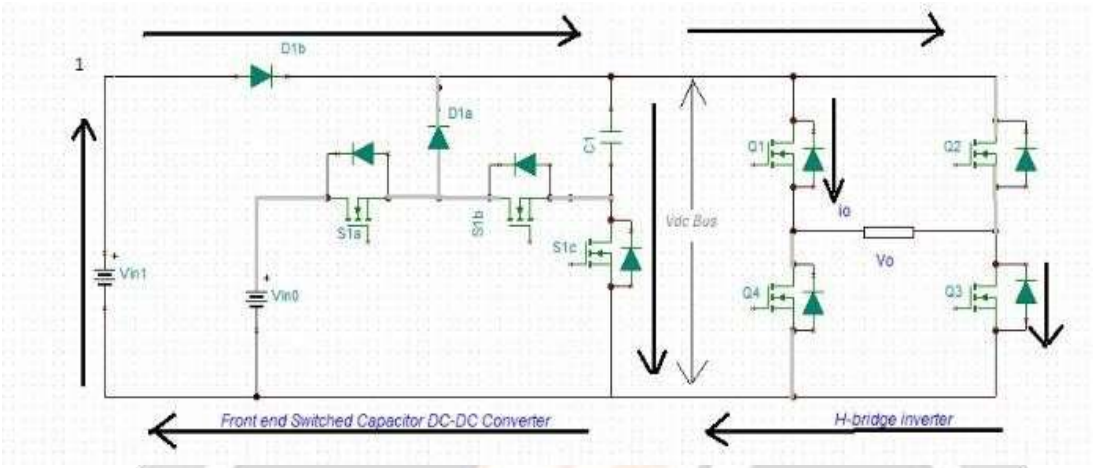

Fig- 3: Equivalent circuit for V0 = +Vin1

4.2. Output voltage =V_{IN0} state

Figure 4 shows the equivalent circuit for V0 = +Vin0.For normal operation of the proposed inverter, Vin0 > Vin1. In the DC - DC converter, only transistor S1a is turned ON while other transistors are turned OFF. Therefore, Vin0 is connected to the DC bus through diode D_{1a}. As Vin0 > Vin1, diode D1b is reverse biased and hence blocks Vin1. The capacitor C_1 is open during this state. Therefore, its voltage remains at V_{IN1}.

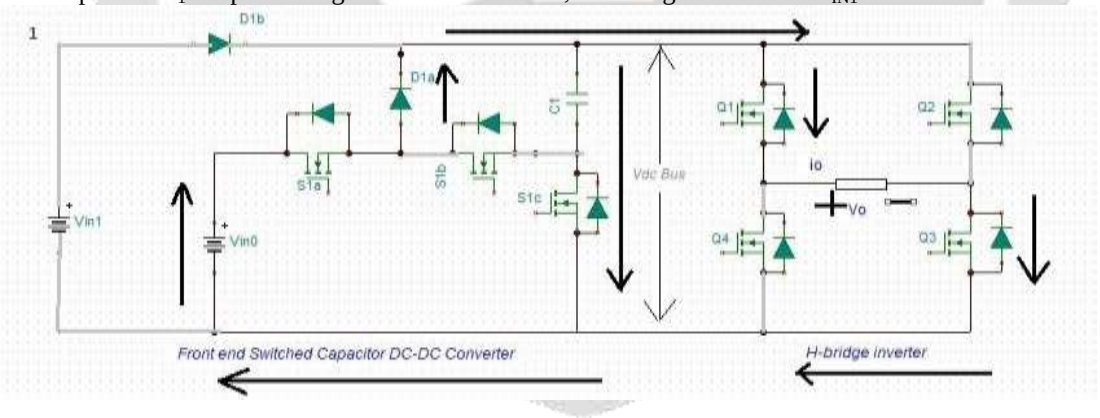

Fig-4: Equivalent circuit for V0 = +Vin0

4.3. Output voltage = (V_{IN0} + V_{IN1}) state

Figure 5 shows the equivalent circuit for V0 = +(Vin0 + Vin1).Capacitor C_1, charged toVin1, is connected in series with input voltage Source Vin0 by turning ON transistors S1a and S1b. Diode D1b is reverse biased and blocks Vin1. The net voltage that appears across the DC bus now is equal to Vin0 + Vin1. In this state, input voltage source V_{IN0} and capacitor C_1 supply power to the load.

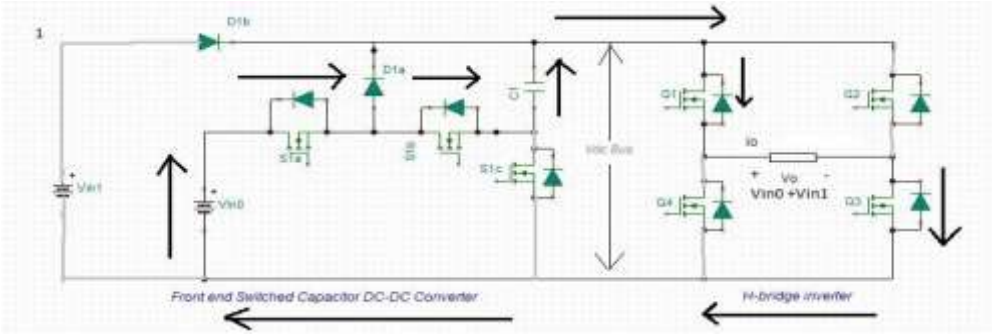

Fig-5: Equivalent circuit for V0 = +(Vin0 + Vin1)

4.4 Output voltage = 0V state

Figure 6 shows the equivalent circuit for v0 = 0V.To obtain zero level at the output after the positive half cycle, only transistor Q_1 is turned ON, while all the other switches in the H-bridge inverter remain turned OFF. The body diode of transistor Q_2 is employed for free-wheeling. Similarly, to obtain zero level at the output after the negative half cycle, only transistor Q_4 is turned ON, while all the other switches in the full bridge inverter remain turned OFF. In this case, the body diode of transistor Q_3 is employed for free-wheeling. The switches in the front-end converter remain in their previous states.

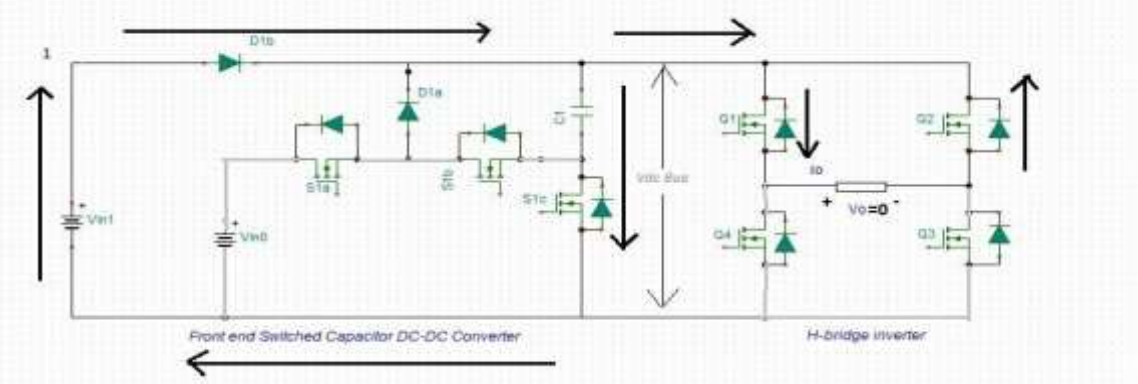

Fig-6: Equivalent circuit for V0 = 0V

TABLE I: SWITCHING LOGIC FOR THE 7-LEVEL SCMLI

S_{1a}	S_{1b}	S_{1c}	Q_1	Q_2	Q_3	Q_4	V_0
0	0	1	1	0	1	0	V_{IN_1}
1	0	0	1	0	1	0	V_{IN_0}
1	1	0	1	0	1	0	$V_{IN_0} + V_{IN_1}$
0	0	1	1	0	0	0	0
0	0	1	0	1	0	1	$-V_{IN_1}$
1	0	0	0	1	0	1	$-V_{IN_2}$

1	1	0	0	1	0	1	$-(V_{IN_0} + V_{IN_1})$
0	0	1	0	0	0	1	0

5. HARDWARE CIRCUIT DIAGRAM

The hardware circuit diagram is shown in the figure 7.The hardware circuit diagram consists of Multilevel inverter, step down transformer,PIC16F877A microcontroller and optocoupler used for producing seven level voltage at the output with reduced harmonics. The operation of the hardware as follows. The 230V AC supply is given to the single phase step down transformer. The voltage is then step down to 12V. The step down voltage is the given to the rectifier where the AC voltage is converted into the pulsating DC voltage. Then the DC voltage is given to the filter to remove the ripples in the output voltage. The output voltage is given to the voltage regulator LM7805 and the regulated to 5V and then it is given to the PIC16F877A microcontroller. The seven transformer are used in the hardware are connected to the switches. All the switches are connected to the controller. In the PIC microcontroller, fuzzy logic was implemented. The controller will control the on and off operation of the switches by varying the firing pulse. The two asymmetric voltages are given to the seven level switched capacitor asymmetric multilevel inverter. It consists of SC based DC-DC converter which employs two input sources (Vin0 and Vin1), three transistors (S1a, S1b and S1c), two diodes (D1a and D1b) and a capacitor (C1). SC DC-DC convert input voltage to integral multiple output levels without utilizing inductors. DC levels obtained at the inverter DC bus inverter DC bus include Vin0, Vin1, Vin0+Vin1. The common feature in all the switched capacitor multilevel inverter topologies is the back – end H –bridge inverter. The H-bridge inverter employing transistors Q1 to Q4 effectively produces six bipolar level and a zero voltage level (0, ±Vin0, ±Vin1,±(Vin0+Vin1) across the load. The output voltage waveform can be measured using the Digital Scope Oscillator (DSO). The voltage can also be measured using the multimeter by connecting across the load.

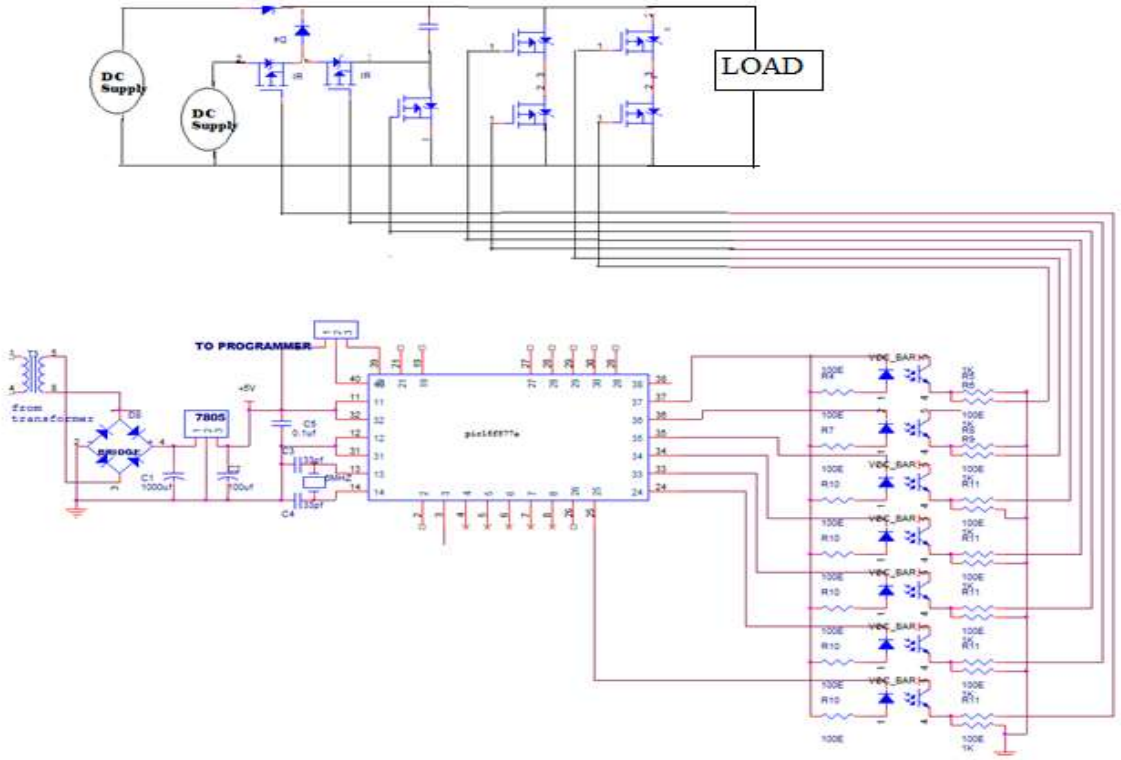

Fig-7: Hardware Circuit Diagram

6. HARDWARE REQUIREMENTS

- Step down transformer
- MOSFET switches
- Rectifier unit
- Filtering unit
- Voltage regulator
- Optocoupler

7. SOFTWARE REQUIREMENTS

MATLAB software

8. HARDWARE KIT

Fig-8: snap shot of hardware

9. OUTPUT WAVEFORM

Fig-9: snap shot of output waveform

10. CONCLUSION

A novel fuzzy controlled topology for HFAC PDS has been implemented. This topology is applicable where unequal DC input sources are at disposal. It is more convenient to employ multiple DC sources as input to a single inverter than to employ several inverters in parallel with their respective solitary DC input sources. This topology does not stack up the voltage sources in series and therefore does not require voltage balancing circuits. Since the switched capacitors employed copy the input voltage every cycle, the problem of voltage balancing has also been eliminated. The harmonic content in the waveform is analyzed and is found to be minimum.

11. REFERENCES

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