A Novel Topology of Cascaded Transformer Ten Switches Multilevel Inverter

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ABSTRACT

The proposed system consists of H-bridge output stage with a bi-directional switch. It can be considered as voltage synthesizer and generates five voltage levels. Single phase low frequency transformers are used in structure. The main functions of the Single phase low frequency transformers are voltage transformation and isolation. Owing to the cascaded transformers, it has a galvanic isolation between an input DC source and output loads.Additionally, since two capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in some other multi level configuration. Here only ten switches have been used which reduces the switching losses to a great extent and since we are using diodes, conduction losses may occur but it is very negligible when compared to the switching losses. By cascading the two transformers the output voltage can be increased and also the cost is less when compared to the conventional methods because of lower switches and power driver circuits. Since the level has been increased the harmonic contents will be less and thus we can obtain a sinusoidal waveform, not a pure waveform but a waveform with less harmonic distortion. By using this method we can reduce the harmonic contents and increase the power quality to a great extent.

Keywords : - *H Bridge, galvanic isolation , diode clamped multilevel inverter ,Split source capacitor*

1 INTRODUCTION

Now a day's many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage. The multi level inverter has been introduced since 1975 as alternative in high power and medium voltage situations. The Multi level inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations. The need of multilevel converter is to give a high output power from medium voltage source. Sources like batteries, super capacitors, solar panel are medium voltage sources. The multi level inverter consists of several switches. In the multi level inverter the arrangement switches' angles are very important.The multilevel converter has a several advantages, that is:it produce common mode voltage, reducing the stress of the motor and don't damage the motor,it can draw input current with low distortion,it can operate at both fundamental switching frequencies that are higher switching frequency and lower switching frequency. It should be noted that the lower switching frequency means lower switching loss and higher efficiency is achieved.Selective harmonic elimination technique along with the multi level topology results the total harmonic distortion becomes low in the output waveform without using any filter circuit.

2 DIODE CLAMPED MULTILEVEL INVERTER

Fig1 shows the circuit diagram of Conventional method of Diode Clamped Multilevel Converter. A diode clamped multilevel inverter typically consists of (m-1) capacitors on the dc bus and produce m levels on the phase voltage. It

shows one leg a full bridge five level diode clamped converter. The numbering order of the switches is Sa1, Sa2, Sa3, Sa4, Sa1', Sa2', Sa3', Sa4'. The dc bus consists of four capacitors, C1, C2, C3, and C4.

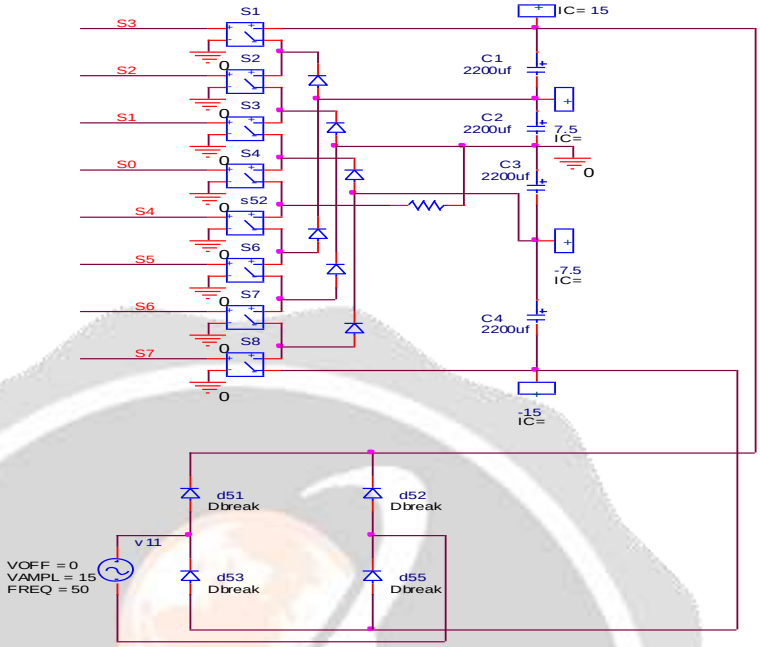

Fig 1 Circuit Diagram of Diode Clamped Multilevel Converter

For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress is limited to one capacitor voltage level $V_{dc}/4$ through the clamping diode. An m-level inverter leg requires (m-1), capacitors, 2(m-1) switching devices and (m-1), (m-2) clamping diodes. The major disadvantage with this methods are Switching losses will be more,the size of the circuit increases as the level increases, therefore the circuit becomes more complex.Cost increases as the components used are more.To overcome this a new topology is proposed.

3 PROPOSED INVERTER

The circuit diagram consists of ten switches and a split source capacitor and two transformers with different turns ratio.Fig2 shows the circuit diagram of a 25 level inverter by cascading two transformers for ac drives. Here it consists of a single dc source which may be a battery or a solar panel and a split source capacitor and two bidirectional switches and eight switches are used. Split source capacitor is used in order to split the voltage equally and the input dc source is 80V.

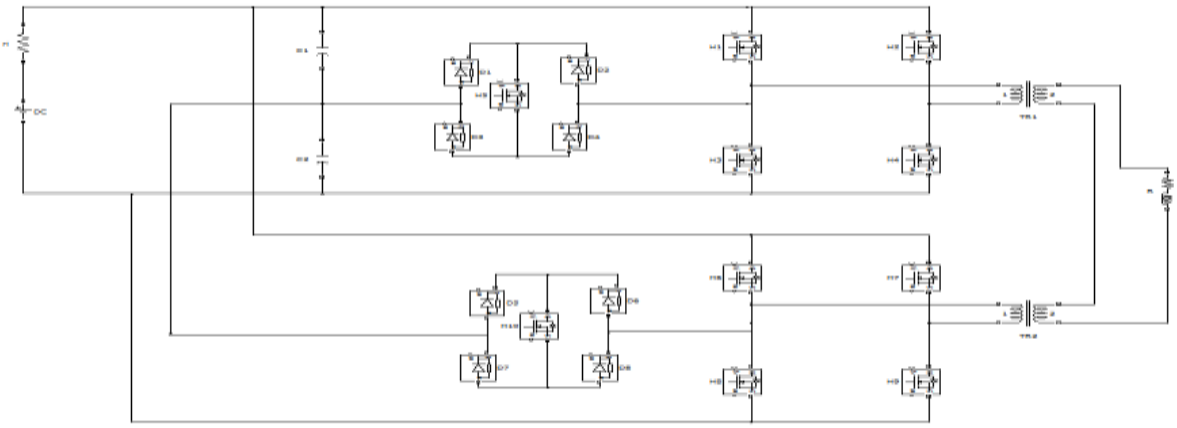

Fig 2 Circuit Diagram of a 25 Level Inverter

Two transformers with different turns ratio have been used, it is in the ratio of 1:5 therefore we can get a output voltage of 400V. By turning the switches properly, the required voltage can be obtained and proper switching control strategies has to be used in order to obtain required voltage levels. Here pulse width modulation technique is used to obtain desired ac voltage

3.1 SWITCHING OPERATION

Table 1: Switching Operation

Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
0	1	1	0	0	0	1	1	0	0	0
Vdc/2	0	0	0	1	1	1	1	0	0	0
Vdc	1	0	0	1	0	1	1	0	0	0
3Vdc/2	0	1	1	0	0	0	0	0	1	1
2Vdc	0	1	0	0	1	0	0	0	1	1
5Vdc/2	1	1	0	0	0	0	0	0	1	1
3Vdc	0	0	1	0	1	0	0	0	1	1
7Vdc/2	1	0	0	1	0	0	0	0	1	1
4Vdc	0	1	1	0	0	1	0	0	1	0
9Vdc/2	0	1	0	0	1	1	0	0	1	0
5Vdc	1	1	0	0	0	1	0	0	1	0
11Vdc/2	0	0	1	0	1	1	0	0	1	0
6Vdc	1	0	0	1	0	1	0	0	1	0
11Vdc/2	0	0	1	0	1	1	0	0	1	0
5Vdc	1	1	0	0	0	1	0	0	1	0
9Vdc/2	0	1	0	0	1	1	0	0	1	0
4Vdc	0	1	1	0	0	1	0	0	1	0
7Vdc/2	1	0	0	1	0	0	0	0	1	1
3Vdc	0	0	1	0	1	0	0	0	1	1
5Vdc/2	1	1	0	0	0	0	0	0	1	1
2Vdc	0	1	0	0	1	0	0	0	1	1
3Vdc/2	0	1	1	0	0	0	0	0	1	1
Vdc	1	0	0	1	0	1	1	0	0	0
Vdc/2	0	0	0	1	1	1	1	0	0	0
0	1	1	0	0	0	1	1	0	0	0

- **LEVEL 1**
  In this first level the output voltage is zero, in order to obtain the first level the switches **S1** and **S2** in the upper leg is turned **ON** as well as the switches **S6** and **S7** in the lower leg is turned **ON**.
- **LEVEL 2**
  In this level the output voltage is Vdc/2, to obtain this the switches **S4** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S7** are turned **ON.**
- **LEVEL 3**
  In this level the output voltage is Vdc, to obtain this the switches **S1** and **S4** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S7** are turned **ON.**

- **LEVEL 4**
  In this level the output voltage is 3Vdc/2, to obtain this the switches **S2** and **S3** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 5**
  In this level the output voltage is 2Vdc, to obtain this the switches **S2** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 6**
  In this level the output voltage is 5Vdc/2, to obtain this the switches **S1** and **S2** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 7**
  In this level the output voltage is 3Vdc, to obtain this the switches **S3** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 8**
  In this level the output voltage is 7Vdc/2, to obtain this the switches **S1** and **S4** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 9**
  In this level the output voltage is 4Vdc, to obtain this the switches **S2** and **S3** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 10**
  In this level the output voltage is 9Vdc/2, to obtain this the switches **S2** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 11**
  In this level the output voltage is 5Vdc, to obtain this the switches **S1** and **S2** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 12**
  In this level the output voltage is 11Vdc/2, to obtain this the switches **S3** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 13**
  In this level the output voltage is 6Vdc, to obtain this the switches **S1** and **S4** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 14**
  In this level the output voltage is 11Vdc/2, to obtain this the switches **S3** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 15**
  In this level the output voltage is 5Vdc, to obtain this the switches **S1** and **S2** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 16**
  In this level the output voltage is 9Vdc/2, to obtain this the switches **S2** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 17**
  In this level the output voltage is 4Vdc, to obtain this the switches **S2** and **S3** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S9** are turned **ON.**
- **LEVEL 18**
  In this level the output voltage is 7Vdc/2, to obtain this the switches **S1** and **S4** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 19**
  In this level the output voltage is 3Vdc, to obtain this the switches **S3** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 20**
  In this level the output voltage is 5Vdc/2, to obtain this the switches **S1** and **S2** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 21**
  In this level the output voltage is 2Vdc, to obtain this the switches **S2** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**

- **LEVEL 22**
  In this level the output voltage is 3Vdc/2, to obtain this the switches **S2** and **S3** in the upper leg is turned **ON** and in the lower leg the switches **S9** and **S10** are turned **ON.**
- **LEVEL 23**
  In this level the output voltage is Vdc, to obtain this the switches **S1** and **S4** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S7** are turned **ON.**
- **LEVEL 24**
  In this level the output voltage is Vdc/2, to obtain this the switches **S4** and **S5** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S7** are turned **ON.**
- **LEVEL 25**
  In this level the output voltage is 0V, to obtain this the switches **S1** and **S2** in the upper leg is turned **ON** and in the lower leg the switches **S6** and **S7** are turned **ON.**

4 SIMULATION RESULTS OF CONVENTIONAL METHOD

Fig 3 consists of DC source of 24V as input and eight switches. Here in order to increase the level we have to go for more number of switches.

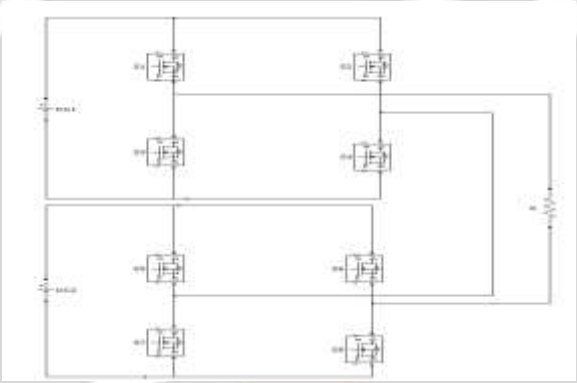

Fig 3 Conventional Cascaded Multilevel Inverter

4.1 INPUT WAVEFORM

Fig 4 shows the input voltage waveform of the conventional method and the input supply for both DC source is 24V.

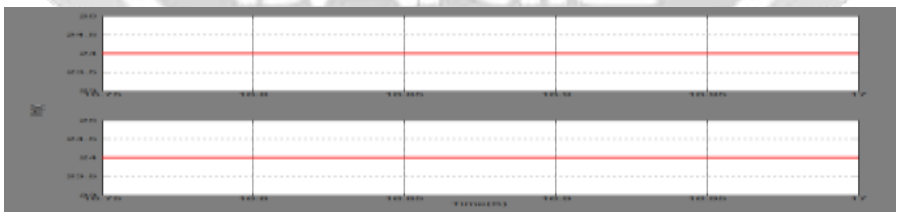

Fig 4 Input Voltage Waveform

4.2 OUTPUT VOLTAGE

Fig 5 shows the Output voltage of a Multilevel inverter based on switched dc source with R load.

Fig 5 Output Voltage Waveform

4.3 OUTPUT CURRENT

Fig 6 shows the Output Current of a conventional cascaded multilevel inverter with R load.

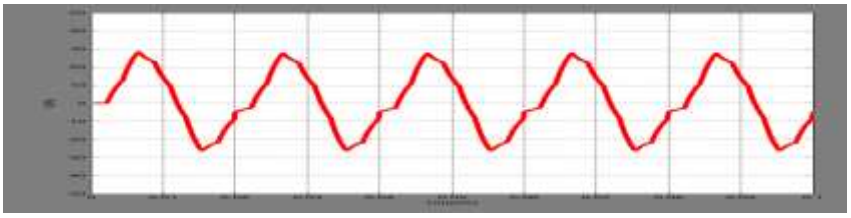

Fig 6 Output Current Waveform

4.4 THD OF OUTPUT CURRENT

Fig 7 shows the total harmonic distortion of the conventional method and THD% is 41.12%.

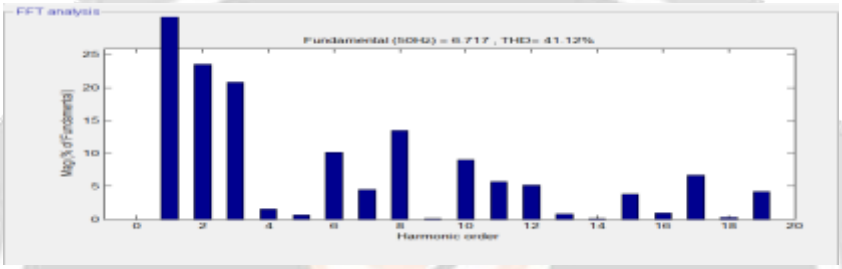

Fig 7 THD of Output Current

5 SIMULATION RESULTS OF 25 LEVEL INVERTER

Fig 8 shows the simulation diagram of 25 level inverter which consists of 10 MOSFETS, 8 diodes, a split source capacitor and two transformers of different turns ratio.

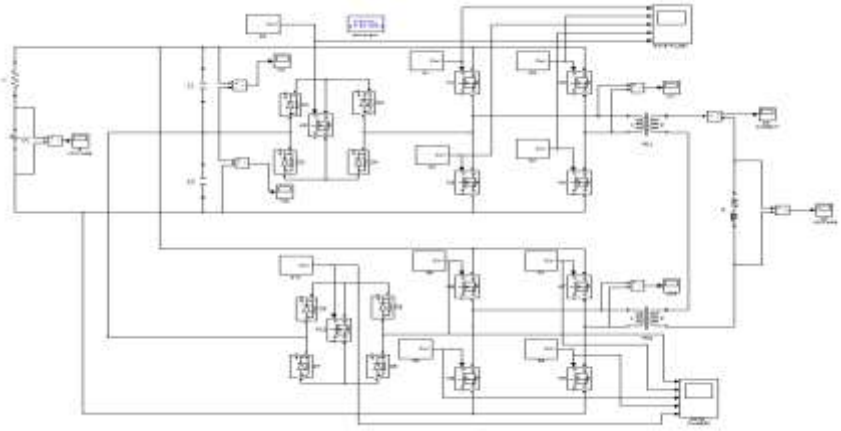

Fig 8 Simulation Diagram of 25 Level Inverter

The gate pulses are given to the switches using PWM(Pulse Width Modulation) technique and the output is viewed in scope and the respective current and voltage values are measured using current and voltage measurement block.

5.1 INPUT VOLTAGE

Fig 9 shows the input voltage waveform. The input voltage given to the circuit is Vdc.

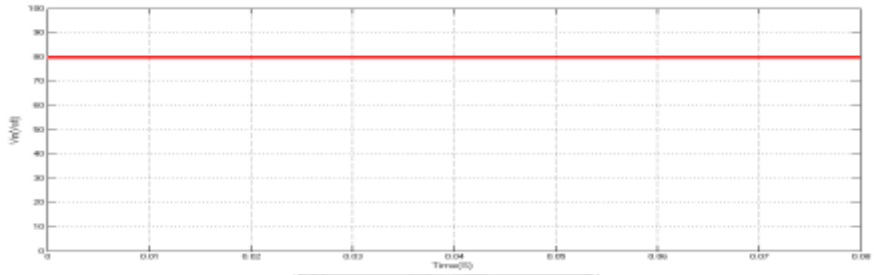

Fig 9 Input Voltage Waveform

5.2 TRIGGERING PULSES

Fig 10 shows the triggering pulses for each MOSFET and the pulses are given by using PWM (Pulse Width Modulation technique). There are 4 gate driver circuits used to supply the triggering pulses to the switches.

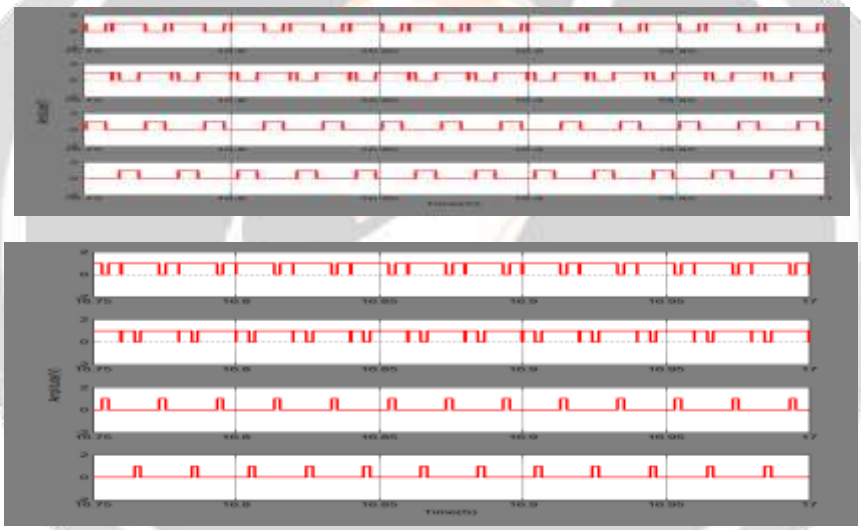

Fig 10 Triggering Pulse

5.3 OUTPUT VOLTAGE

Fig 11 shows the output voltage waveform of 25 level inverter. It is a staircase waveform with 25 levels from peak to peak. It is observed that as the level increases the waveform looks like sinusoidal waveform.

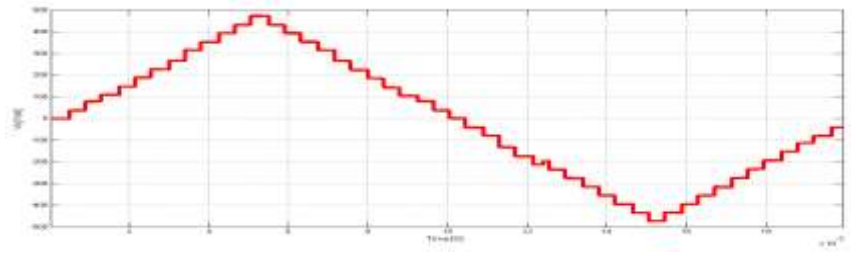

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Fig 11 Output Voltage Waveform

5.4 OUTPUT CURRENT

Fig 12 shows the waveform of the output current for 25 level inverter which is a sinusoidal waveform.

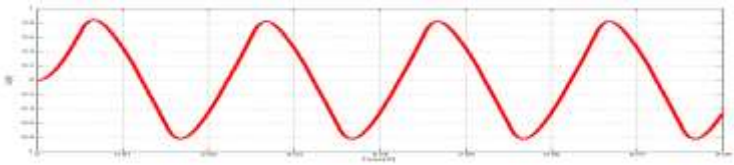

Fig 12 Output Current Waveform

5.5 THD OF OUTPUT CURRENT

Fig 13 shows the graph of Total Harmonic Distortion of output current for 25 level inverter. The percentage magnitude of fundamental harmonics is very high for lower harmonic order and it decreases as the order increases.

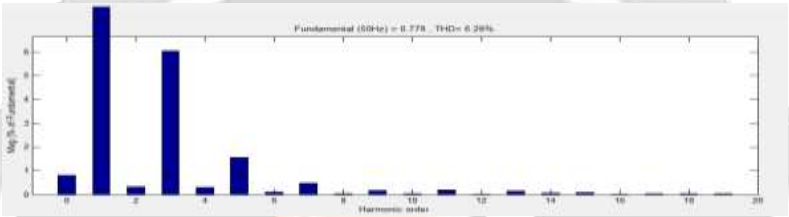

Fig 13 THD of Output Current

6. HARDWARE IMPLEMENTATION

The hardware circuit is designed with fast switching device MOSFET to have fast switching operation. The designing plan is done to have the hardware circuit to be compact and ease in controlling.

6.1 HARDWARE CIRCUIT OF 25 LEVEL INVERTER

Fig 14 shows the complete hardware circuit diagram. The hardware is designed in order to produce 25 different levels of AC output from a single DC source. This is made possible by the different switching mechanisms by using Pulse Width Modulation technique. The gate pulses are produced using gate driver circuits. The control to the entire system is done by using Microcontroller. The dc supply of 5 V and 12 V is given to the gate driver circuit. Thus by increasing the levels we can reduce the harmonics to a great extent.

The hardware design consists of three main circuits viz., Power Circuit, Isolation Circuit and Isolation Circuit. Our focus was towards the power circuit. The power circuit consists of eight MOSFET, two bidirectional switches and a split source capacitor. The output is increased by transformers of different turns ratio and the load used is a resistive load. The Controller circuit consists of microcontroller AT89C51. It is a 40 pin IC with 4 ports of each 8 bit. The ports are used to give the input signal and the output is fetched. A crystal oscillator is connected to the microcontroller which is used to define the speed of the controller. The pulses are given from the microcontroller to the buffer circuit to increase the current of the pulse. The buffer used is 74LS244A. The buffer used is an 8 pin buffer, therefore only 8 pulses are given through the buffer to the gate driver circuits. The remaining two pulses are produced by two opto isolator circuits, which are used for isolation. The gate driver IC used is IR2110. The opto isolator used is TLP250. The supply to the IC's are given using two step down transformers (5 volt and 12 volt).The voltage from the power circuit may damage the microcontroller. So, in order to protect the microcontroller from damage the isolation circuit is connected between the power circuit and the controller. The output current gain of the pulse is very low , therefore the buffer circuit is connected for current amplification.

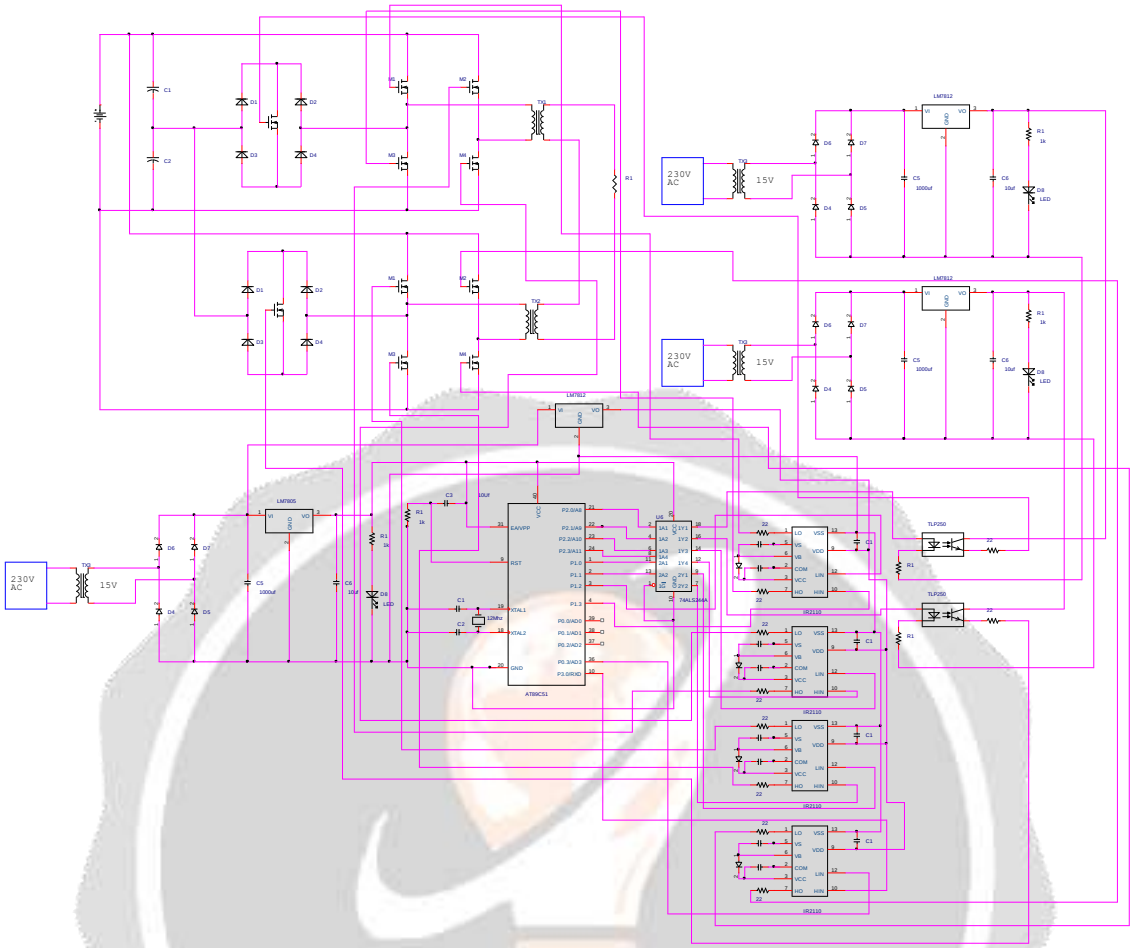

Fig 14 Hardware Circuit Diagram

6.2 HARDWARE SETUP

Fig 15 Hardware Setup

Fig 15 shows the Hardware setup of the 25 Level Inverter. It includes the power circuit , controller circuit and isolation circuit. The battery used is 15 volt battery and the connections are made as per the hardware circuit diagram.

6.3 HARDWARE RESULT

Fig 16 Hardware Result

Fig 16 shows the Hardware Result of the 25 Level Inverter. The output voltage waveform is displayed in the CRO and the 25 level output was verified.

7 CONCLUSION

In this paper, a novel twenty five level inverter was proposed. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by this topology. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology. This paper mainly analyzes 25 level inverters.The proposed inverter can be applied to grid-connected photovoltaic system and electrical network of EV, because the multiple dc sources are available easily from solar panel, batteries, ultra capacitors, and fuel cells.

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