

A Quasi Single Stage Buck-Boost Inverter with High Reliability and Efficiency

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Abstract

Modern power-electronic interfaces must deliver regulated AC from variable DC sources such as photovoltaic strings, battery packs, and electric-vehicle DC buses. This paper presents a control-oriented averaged model of a quasi single-stage buck-boost inverter targeting 230 Vrms at 50 Hz. The model integrates buck/boost duty-dependent DC-link relations with the inverter fundamental under sinusoidal PWM and includes LC filter dynamics. A one-cycle RMS estimator and a discrete feedforward-plus-PID duty controller regulate the output under input-voltage and load disturbances. The complete model is implemented as a modular Simulink architecture assembled by an auto-build MATLAB script, enabling efficient simulation and extension.

Keywords—Buck-boost inverter, quasi single-stage, high efficiency, Simulink, renewable energy, power electronics.

1. INTRODUCTION

1.1 Background and Motivation Modern power-electronic interfaces must deliver regulated AC from DC sources whose voltage varies (PV, batteries, EV buses). The converter therefore requires both step-down and step-up capability while maintaining high efficiency and robustness.

1.2 Limitations of Multi-Stage Converters A common architecture uses a DC-DC converter to create a stiff DC-link followed by a DC-AC inverter. Cascaded stages increase device count, losses, size, and failure probability.

1.3 Quasi Single-Stage Buck-Boost Inverter The QSS buck-boost inverter integrates the buck/boost function with the inverter stage. It behaves as a buck converter when input voltage is high and as a boost converter when input is low, reducing redundant power processing.

1.4 Objectives Objectives: (i) build a control-oriented averaged model for 230 Vrms, 50 Hz output; (ii) implement a discrete RMS-regulation loop with duty control; (iii) create a modular Simulink model using an auto-build script; (iv) evaluate behaviour under input and load disturbances.

1.5 Dissertation Organization Chapter II reviews related work. Chapter III details system modelling. Chapter IV covers control strategy and Simulink implementation. Chapter V presents results. Chapter VI concludes and suggests future work.

2. LITERATURE REVIEW

2.1 Buck-Boost Conversion and Inverters Buck-boost conversion enables wide input operation. In inverter systems the regulated variable is typically the AC fundamental amplitude or RMS rather than instantaneous voltage.

2.2 Single-Stage and Quasi Single-Stage Structures Single-stage and quasi single-stage inverters reduce stage count relative to boost + inverter solutions. Reported approaches include impedance-source, differential and integrated buck/boost H-bridge families.

2.3 Regulation and RMS Control Controllers range from linear PWM-based loops to sliding-mode and predictive control. Practical digital implementations often regulate RMS using cycle-based estimation or fundamental extraction; PID remains common due to simplicity and

robustness.

2.4 Averaged Modelling in MATLAB/Simulink Averaged switching models replace high-frequency switching with duty-dependent relations while retaining slow-scale dynamics. This makes long simulations and controller tuning computationally efficient.

2.5 Summary The research focus here is a modular averaged model plus a practical RMS feedback loop for disturbance testing and future extension to detailed switching models.

3. SYSTEM DESCRIPTION AND MODELLING

3.1 System Overview The system contains an integrated buck/boost stage, inverter fundamental generation and an LC output filter. The design aims for 230 Vrms at 50 Hz from a variable DC input.

Conceptual QSS Buck-Boost Inverter Topology

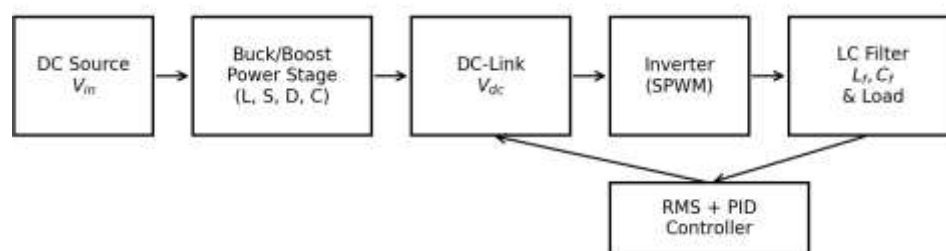


Fig. 3.1: Quasi single-stage buck-boost inverter topology (conceptual representation).

3.2 Buck and Boost Relations To create the required DC-link level, the averaged model uses: buck mode $V_{dc} = D \cdot V_{in}$, and boost mode $V_{dc} = V_{in}/(1-D)$. Mode selection is based on whether V_{in} is greater than the required $V_{dc,ref}$.

3.3 Inverter Fundamental under SPWM The inverter is represented by its fundamental component: $v_{inv}(t) = (m/2) \cdot V_{dc} \cdot \sin(\omega t)$, where m is modulation index and $\omega = 2\pi f_{out}$. This captures line-frequency behaviour without explicit switching.

3.4 LC Filter Dynamics The LC filter is modelled using discrete-time integrators: $di_L/dt = (v_{inv} - v_{out})/L_f$ and $dv_{out}/dt = (i_L - v_{out}/R)/C_f$. This retains resonant dynamics important for control assessment.

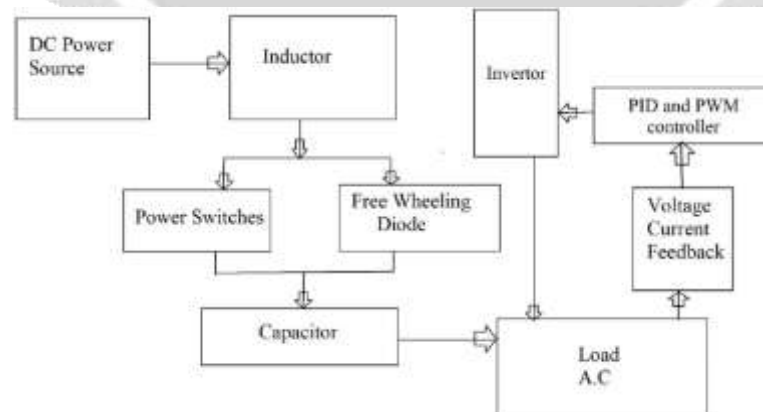


Fig. 3.2: System-level block diagram (paper representation).

4. CONTROL STRATEGY AND SIMULINK IMPLEMENTATION

4.1 Control Objective The controller regulates duty cycle to maintain output RMS at 230 Vrms. The modulation index m is kept constant and the DC-link is adjusted through buck/boost duty control.

4.2 One-Cycle RMS Estimation A circular buffer stores one fundamental cycle of output voltage samples. The RMS is computed as $\sqrt{\text{mean}(v^2)}$ over that buffer, producing a stable measurement aligned to the 50 Hz period.

4.3 Feedforward plus PID Trim A feedforward duty estimate is computed from steady-state relations for buck or boost operation. A discrete PID generates a small trim to correct RMS error; the duty is saturated between 0.02 and 0.98.

4.4 Modular Simulink Architecture The model is assembled by an auto-build MATLAB script into five subsystems: input profile, feedback control, power stage, measurements/efficiency, and scopes.

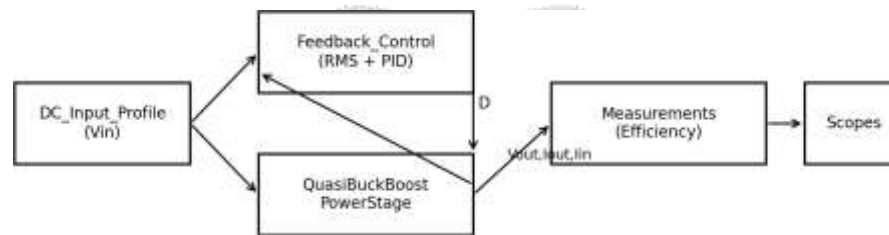


Fig. 4.1: Simulink subsystem architecture used for the QSS buck-boost inverter model.

4.5 Parameters

Parameter	Symbol	Value
AC fundamental frequency	f_{out}	50 Hz
PWM carrier reference	f_{sw}	20 kHz
Discrete sample time	T_s	20 μ s
Modulation index	m	0.90
RMS reference	$V_{ref,rms}$	230 V
Input voltage (initial/step)	V_{in1} / V_{in2}	200 V / 150 V
Input ripple (amp, freq)	A_{rip}, f_{rip}	5 V, 2 Hz
Filter inductance	L_f	2 mH
Filter capacitance	C_f	2.2 μ F
Load (before/after step)	R_1 / R_2	100 Ω / 50 Ω
Simulation stop time	T_{stop}	10 s

5. SIMULATION RESULTS AND DISCUSSION

5.1 Input Disturbance

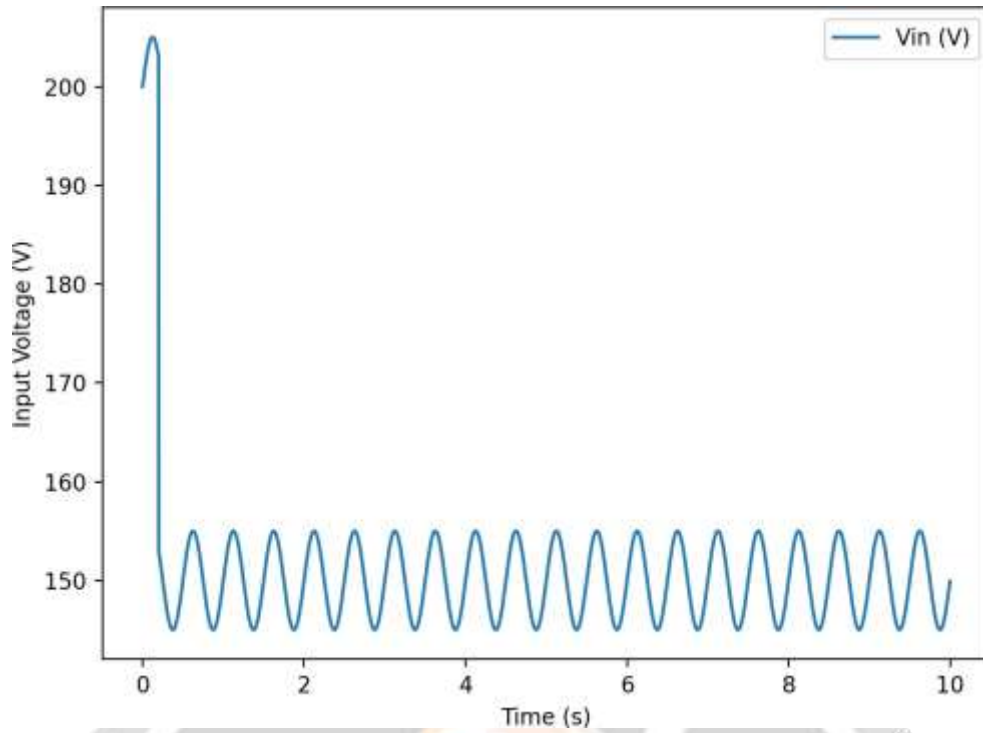


Fig. 5.1: DC input profile used in simulation (step + ripple).

5.2 DC-link Behaviour

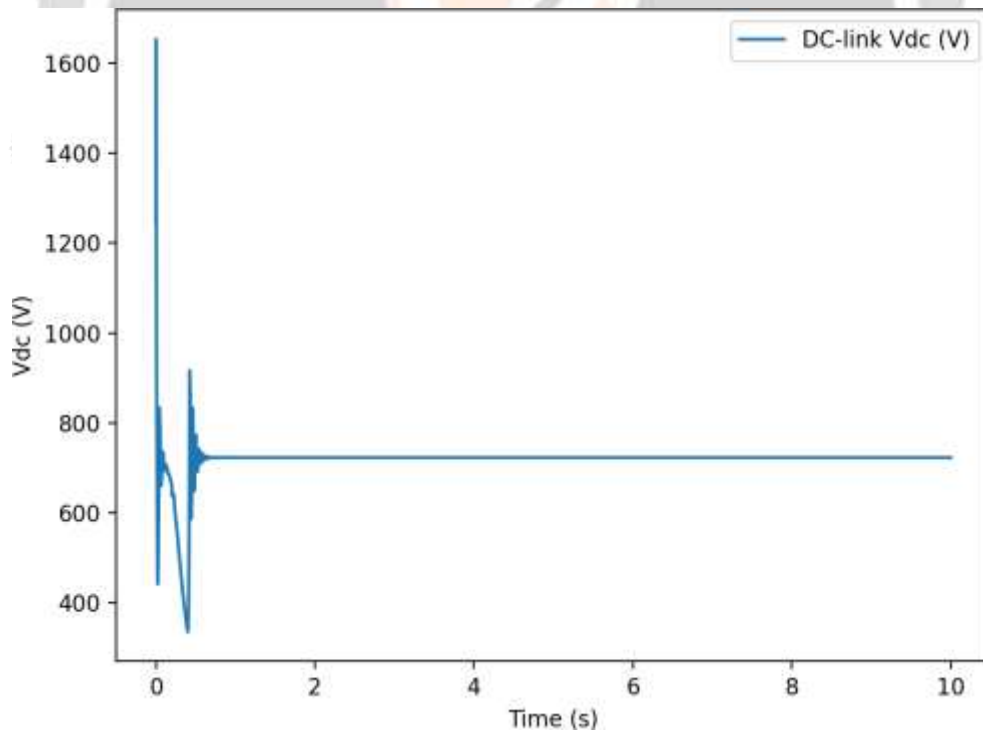


Fig. 5.2: DC-link voltage response computed by the averaged buck/boost relation.

5.3 Output Voltage

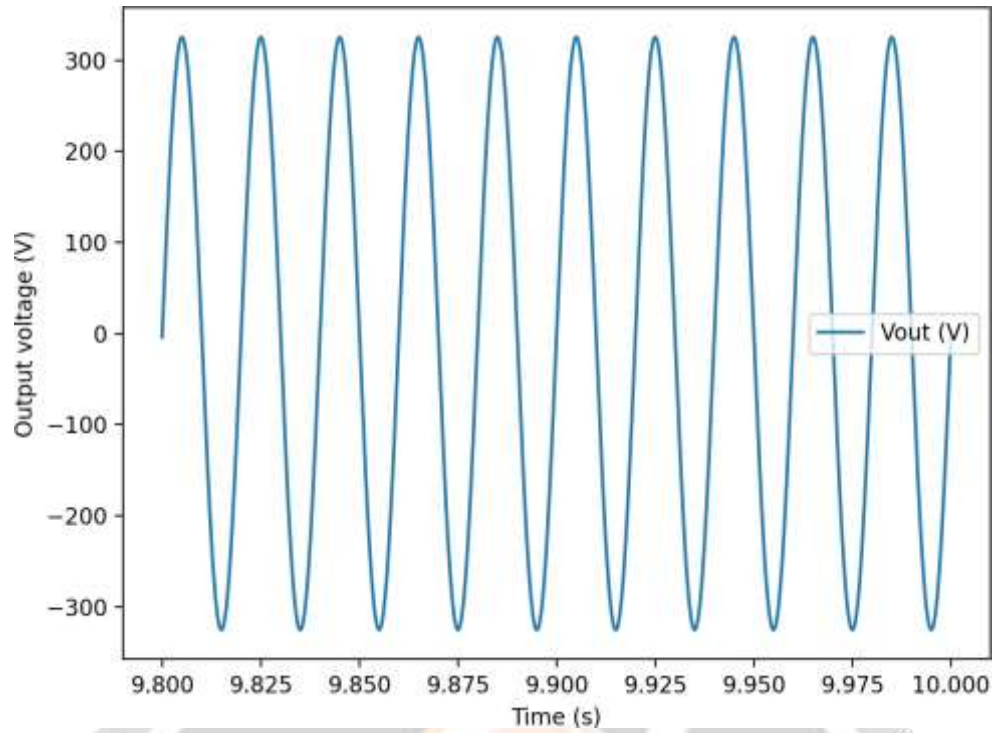


Fig. 5.3: Output voltage waveform after LC filtering (50 Hz fundamental).

5.4 RMS Tracking (230 Vrms)

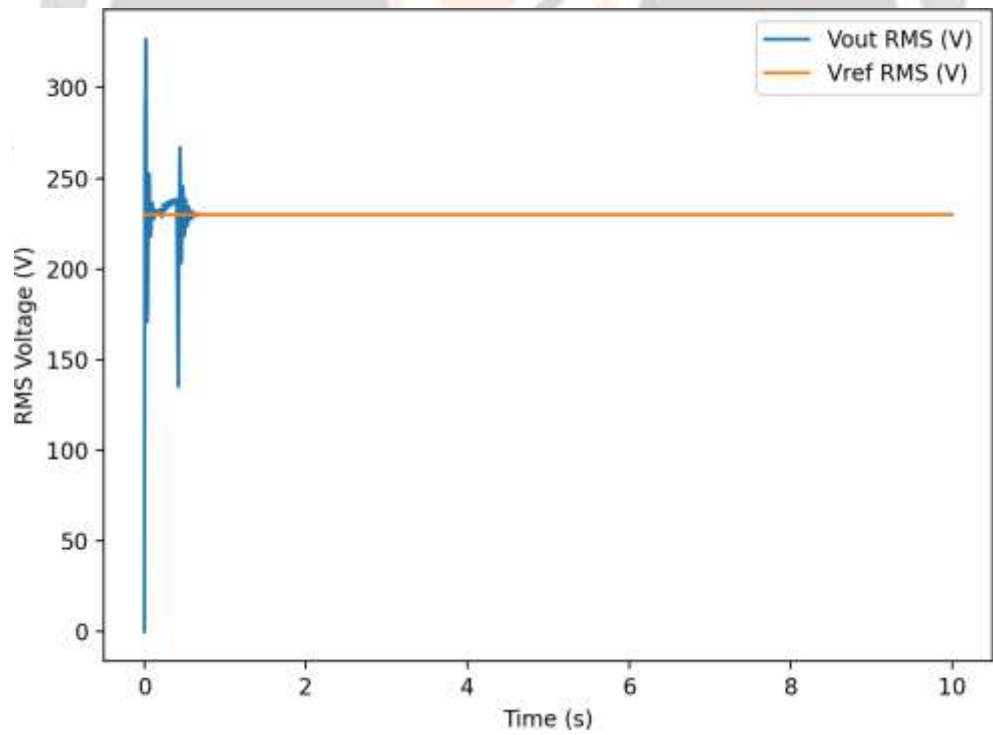


Fig. 5.4: One-cycle RMS estimate tracking a 230 Vrms reference.

5.5 Duty-Cycle Response

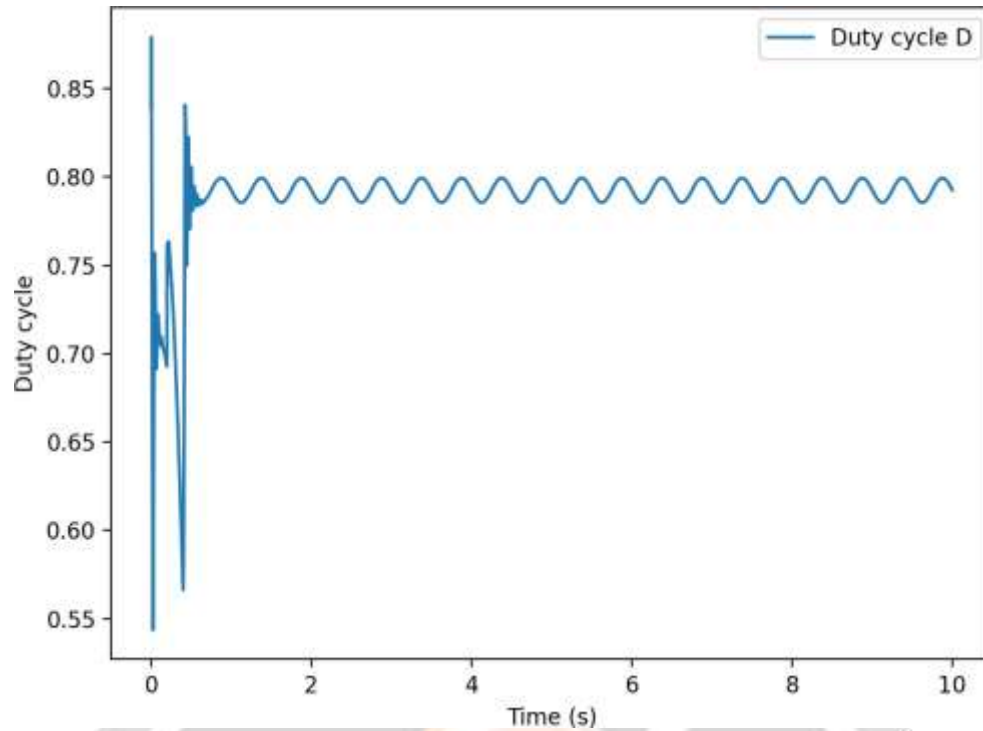


Fig. 5.5: Duty-cycle response produced by feedforward selection plus PID trim.

5.6 Estimated Efficiency

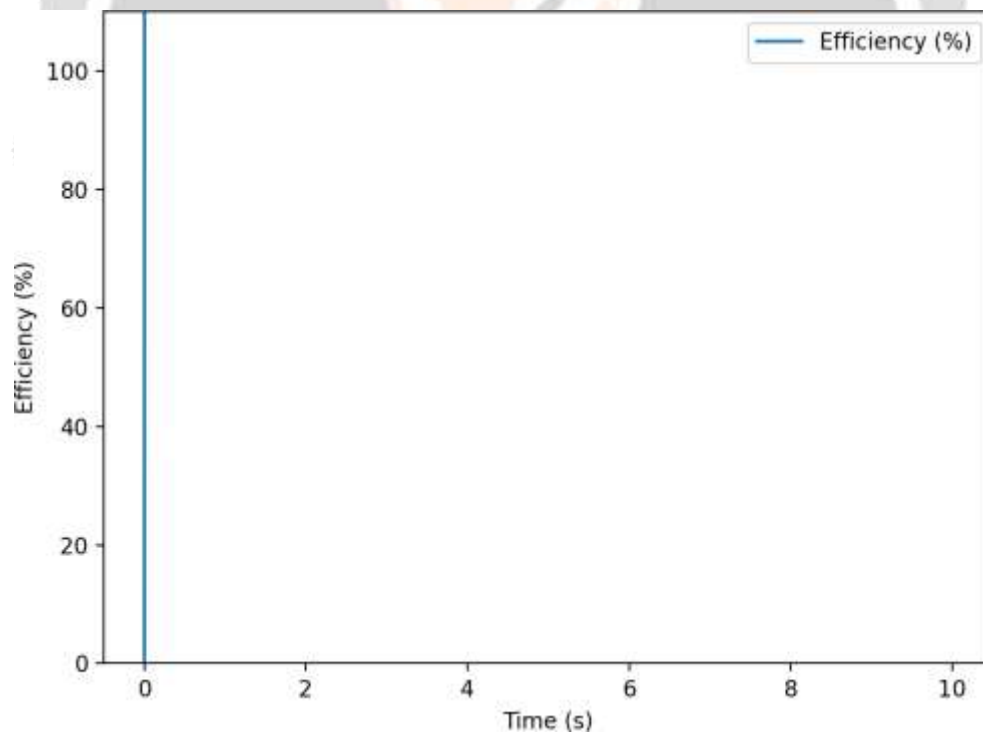


Fig. 5.6: Estimated efficiency based on filtered input and output power.

5.7 Performance Summary The simulated responses show stable RMS regulation under both input-voltage disturbance and load change. The controller maintains the duty command within saturation bounds and preserves the 50 Hz output after LC filtering.

6. CONCLUSION AND FUTURE SCOPE

6.1 Conclusion The dissertation developed an averaged QSS buck-boost inverter model with an RMS-regulating duty controller targeting 230 Vrms at 50 Hz. Simulations show stable RMS regulation under input and load disturbances and highlight the potential efficiency benefit of reduced conversion stages.

6.2 Future Scope Future work: detailed switching model (THD/EMI/stress), non-linear loads, resonant or predictive control, MPPT integration for PV sources, and experimental validation with a laboratory prototype or HIL platform.

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