A REVIEW OF SPEED MULTI - LANE LVDS INTER – FPGA COMMUNICATION LINK

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ABSTRACT

In this paper we are presenting a review of multi lane LVDS inter FPGA communication link. In this paper we are main focus of LVDS and FPGA communication link. This paper describes a review of a multi-lane Low Voltage Differential Signaling (LVDS) interface to form 10 Gbps full duplex communication link interconnecting multiple FPGAs on a board. We also developed a Bit Error Rate Tester for evaluating each individual LVDS physical lane operating at 625 Mbps. Data rates of more than 455 Gbits/s inchips can be achieved using LVDS interface technique. As Integrated Circuit's communication speeds has increased differential signalling is used to handle high speed. Design of high speed LVDS (Low Voltage Differential Signalling) bus interface controller using FPGA is presented. Source synchronous clocking is used to achieve this high speed data transfer.

Keyword : *- LVDS, FPGA, Design, Data Rates, Speed, Signal etc.*

1. INTRODUCTION

This application note describes a method of utilizing dedicated Select IO technology deserializer components (ISERDESE2 primitives) in 7 series FPGAs to interface with analog-to-digital converters (ADC) with serial, low-voltage, and differential signalling (LVDS) outputs. The associated reference design illustrates a basic LVDS interface connecting a Kintex -7 FPGA to an ADC with high-speed, serial LVDS outputs. The high-speed ADCs used today have a resolution of 12, 14, or 16 bits with possible multiple converters in a single package. Each of the converters in the package can be used in standalone mode or converters in the package can be combined and used in an interleaved mode to double or quadruple the conversion (sample) speed. In both standalone mode or interleaved mode, one or two physical serial outputs can be used as a connection to the interfacing device. One set of differential outputs is called a data lane. Using one data lane means that the converter is used in 1-wire mode and two data lanes are called 2-wire mode. For every possible data output combination there is always one high-speed bit clock and one sample rate frame clock available. A simpler test system for the complete functional testing of VLSI devices with large pin count can be developed. The architecture of main test system which is to develop a scalable low cost test system for high pin count VLSI deviceshas the following parts. The main parts are: - PC controller mainly controls the whole testing which is used to input the data vectors in the required format to the controller and also take the resultant vectors from the controller. It compares the values obtained from the Device Under Test with a set of expected values already present. Then it gives the functional PASS or FAIL for the test which was conducted. Then it decodes the data vectors and selects the module and writes to that module. At the end of test it sends back the captured data from the module to the PC. Pin Electronics drives the desired waveform at the pins at the desired times at the proper voltage level and also capture the response from the IC pin. The design includes formatting of the tester dat received from PC and sending it to Pin Electronics using LVDS. The data packet to be sent should include header and data. The header includes many control fields. The interface between communication card and PE is done using Low Voltage Differential Signaling interface to attain high speed data transfer. LVDS is chosen to drive these high speed transmission lines due to its speed, low power consumption, noise control and cost advantageous for data communications. LVDS is currently one of the best point to point interfaces suitable for gigabit per second data rates. Encoding scheme is also applied on the data for security and reliability.

2. LVDS TRANSMITTER UNIT

The transmitter module takes 16 bit data on the parallel side encodes it and performs serialization for each LVDS channel and the given to OBUFDS to obtain the differential signals. The deformatted data from FIFO is encoded using 16B/20B block encoding scheme where the 16 bit input is encoded to 20-bit value and the 20 bit parallel data is converted to serial form using a serializer.16B/20B protocol is used to encode a 16 bit word to 20 bit codes that will result in a dc balance serial stream. The serialization is done by OSERDES block. A 16B/20B transmission scheme incorporates the ides of the 8B/10B transmission code by combining two 8b/10b modules. The input data is provided to both the 8B/10B encoder. In 8B/10B encoding the 8 bit input is divided into two blocks of MSB 3 bit and LSB 5 bit which is converted to 4 bit and 6 bit respectively. The extra bits that are added for encoding depends on the disparity of each blocks of input data disparity of a binary digit is the difference between the number of 1's and number of 0's. The detailed steps in code construction are described in.

3. LVDS RECEIVER UNIT

The receiver in PE card receives the differential signal which is given to Differential Signaling Input Buffer (IBUFDS), which generates the serial data and then performs deserialization and decoding. ISERDES is used for deserialization in the thesis. After deserialization we get 24 bit data where the last 4 bits are zeros. The zero bits are removed and then the 20 bit is decoded to get the 16 bit data that is transmitted. The receiver block includes IBUFDS, ISERDES and decoder. The differential signals are given to IBUFDS, an input buffer that supports low-voltage, differential signaling. In IBUFDS design, its input is represented as two distinct ports and serial output is obtained. The deserializer is done using ISERDES block. The Input Serial-to-Parallel Logic Resources (ISERDES) in Virtex-5 FPGAs is a dedicated serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high speed source synchronous applications. The ISERDES avoids the additional timing complexities encountered when designing deserializer in the FPGA fabric. A single ISERDES component can only deserialize 6 bits. Therefore two ISERDES components are used to deserialize up to 8bits in SDR mode. Decoding is the reverse process of encoding, it restores 20-bit code groups from the input 16-bit code group according to the original code table. A 10B/8B decoder block is used for each upper and lower byte of incoming data. Decoding of data can be done by the examination of just 6 and 5 bits. The required bit translation for decoding can be extracted from table provided in.

4. FPGAS SUPPORT LVDS INTERFACES OVER COMMUNICATION LINK

Nowadays, systems involving multiple FPGAs are used for various scientific applications. Such systems require a data bus dedicated to the communication between FPGAs, which could be done through a LVDS type. Another important factor is that the routing that interconnects the LVDS pins on the platform should be precisely developed to avoid instabilities in communication. Unfortunately, many platforms available in the market do not observe such restrictions, limiting the throughput of the bus. Platforms that involve multiple field-programmable gate arrays (FPGAs) have been the target of several study fields such as prototyping of MPSoCs (multiprocessor system-on-chip), acceleration, and encryption algorithms. For these systems to work efficiently using existing resources in FPGAs, an efficient communication must exist between the FPGAs available on the platform. This type of communication in next-generation FPGAs is usually established through type interfaces low-voltage differential signaling (LVDS) . This type of signaling allows signal sending at high speed through a differential pair of parallel wire. The use of this feature enables data transmission between devices to be performed more efficiently, allowing a more secure communication when facing electromagnetic interference . This configuration enables busses to achieve transfer rates of about 10 Gbps by using more advanced devices such as the Xilinx Virtex family of FPGAs. Currently, many FPGAs support LVDS interfaces, and by being properly allocated on the platform, they can provide data communication at a high transmission rate by using their transceivers. However, some platforms available in the market were not designed to accommodate the LVDS FPGA pin resources in their communication lines, thus preventing the LVDS transceiver use and therefore hindering the implementation of communication channels with high performance. Other factors such as distance between tracks, resistance, and capacitance balance are important and need to be observed by this type of platform manufacturers. Data transmission performed without these resources can lead to errors in data transfer when the transmission rate is high, as there is no guarantee that data integrity is maintained. This is because of all FPGA I/O (Input/Output) pins that are generally subject to physical

interference. Due to this possible low performance in data transmission, systems using these resources will have to reduce their logic module speed to suit the channel and thereby reduce the incidence of communication error.

5. FPGA modules

There are some applications that I have had a hard time finding easy to interface modules to an FPGA including LVDS modules and low cost camera modules. This is where the LOGI Cam design concept came from. Where we wanted to be able to easily interface between any number of camera modules and Pmod connectors. The LOGI cam is able to adapt to many of the omnivision cameras and interface to the camera using the standard 8/10 bit parallel interface. I have been interested in interfacing with some of the LVDS camera modules available to increase bandwidth and or to reduce pin count while communicating with a camera. I have a prototype of a mt9V LVDS camera module that I will be working with. It has the option to function using a parallel 8/10 bit data bus or using LVDS, which will be a great starter LVDS experience in a relatively low cost manner.

6. HIGH-SPEED INTERFACE TECHNOLOGIES OVERVIEW

Differential technologies generally share certain characteristics but vary widely in performance, power consumption, and target applications. Table 1 lists various attributes of the most common differential signaling technologies.

Table -1: Industry Standards for Various LVDS Technologies

	Industry Standard	Maximum Data Rate	Output Swing (V_{OD})	Power Consumption
LVDS	TIA/EIA-644	3.125 Gbps	± 350 mV	Low
LVPECL	N/A	10+ Gbps	± 800 mV	Medium to High
CML	N/A	10+ Gbps	± 800 mV	Medium
M-LVDS	TIA/EIA-899	250 Mbps	± 550 mV	Low
B-LVDS	N/A	800 Mbps	± 550 mV	Low

The 350 mV typical signal swing of LVDS consumes only a small amount of power and therefore LVDS is a very efficient technology, delivering performance at data rates up to 3.125 Gbps. The simple termination, low power, and low noise generation generally make LVDS the technology of choice for data rates from tens of Mbps up to 3 Gbps and beyond. Over the past ten years, several SerDes architectures have flourished to meet the diverging needs of a growing number of applications. The popularity of FPGAs, desire to reduce board traces, and demand for higher bandwidth is resulting in growing adoption of intelligently-partitioned architectures like the FPGA-Attach SerDes. Understanding the advantages and disadvantages of each allows the designer to fit the SerDes to the application to maximize performance and minimize system cost and complexity. Applications such as communications often must guarantee a very stringent Bit Error Rate (BER) such as less than 1-bit error in 1012 or 1015 bits. The total jitter will determine the extent of bit errors. Since total jitter includes random jitter, the established method to fully guarantee these bit error rates is by sending enormous amounts of pseudo random data and validating each bit for errors in a technique known as Bit-Error-Rate Testing (BERT). High speed FPGA to FPGA communication is a key design issue. Such communication is desirable for unified operation of the system. Communication link implemented with differential signaling has advantages over single ended signaling, such as improved noise immunity to common mode noise, higher data transfer speeds, lower power consumption and less electromagnetic interference. It is difficult to find data interfaces above 10 Mbps or longer than half meter that do not use differential signaling. Differential signaling standards vary widely in performance, voltage swing, power consumption, and target applications.

7. COMMUNICATION ERROR TEST

In the presented test, one wrong bit was inserted in a period of 4 ms. The transfers were probed at 100 MHz, and the package size was equal to eight words. The amount of transferred data was of 633.30 Gb, the same amount used in the tests at 100 MHz and normal conditions. Table 5 presents the results. The number of retransmissions performed in this test was of 849,871, indicating that this was the number of packages captured in the receiver that did not

match the checksum. Despite the great number of errors, the retransmitted data amount was of just 25.93 Mb, causing no major impacts in relation to the total communication time. The time required for these retransmissions was approximately 144 ms. This time was measured consider- ing the difference between the test with and without error insertion. After the analysis of these test results, observations showed that the communication was successful despite the errors that had been deliberately inserted in the bus. Therefore, a stable communication between the FPGAs can be obtained under similar conditions.

Table - 2: Results at 150 MHz

Package size	Transfer rate (Gbps)	Data amount (Gb)	Transmission time (s)
8	1.98	894.06	3600
16	3.24	894.06	~2200
32	4.76	894.06	~1500

4. CONCLUSIONS

The system is designed for high-speed data transmission, with low cost and power. A high speed LVDS data bus interface controller applicable in an ATE system for data transmission and reception is been coded in VHDL and has been synthesised for the Virtex5 FPGA board using XILINX ISE13.2. LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high-performance data transmission applications. LVDS not only achieves great benefits in existing applications, but opens the door to many new ones. Systems employing multiple FPGAs to handle distributed processing require data communication among FPGAs for unified operation. This paper describes implementation of a multi-lane Low Voltage Differential Signaling (LVDS) interface to form 10 Gbps full duplex communication link interconnecting multiple FPGAs on a board. The design utilizes advanced IO resources available in the latest Virtex and Spartan series of FPGAs from Xilinx. We also developed a Bit Error Rate Tester for evaluating each individual LVDS physical lane operating at 625 Mbps. Challenges involved in the board design, related to implementation of the interface, are also discussed in this paper. The presented work describes a bi-directional inter-FPGA communication bus using a DDR interface for data transmission. An architecture was designed as a reconfigurable platform, requiring only few parameter settings on the transmitter and receiver to port for different configurations.

6. REFERENCES

[1]. Zhang Huixin, He Qi, Liu Suhua and Yang Haiguang, "The Design for LVDS High Speed Data Acquisition and Transmission System Based on FPGA", IEEE International Conference, 2011, pp. 383-386.

[2]. Parikshit Godbole, Anshul Batth, Nandakumar Ramaswamy, "High Speed Multi-lane LVDS Inter-FPGA Communication Link", ICCIC 2012 IEEE International Conference, Dec. 2010, pp.1-4.

[3]. HeweiNing, Guyong Zhen, Yongfeng Ren,"An Optimal Design of LVDS Interface", ICCSNT International Conference, Dec 2011, Vol. 3, pp. 2024-2026.

[4]. Widmer A X, Franaszek P A, "A DC-Balance Partitioned Block, 8B/10B Transmission Code", IBM Research and Development, Sep. 1983, vol. 27, issue 5, pp. 440-451.

[5]. Suma M. S, Rekha S. S, "16B/20B CODEC Development and Its ASIC Implementation", ICFCC International conference on April 2009, pp. 622-626.

[6]. Wu Jun, "Design of 5B6B Codec Based on FPGA", ICEEE International Conference, Nov. 2010, pp.1-3.

[7]. National Semiconductors, "LVDS Owner's Manual: Low- Voltage Differential Signalling", pp. 8-22, 3rd edition, 2004.

[8]. Xilinx, "Virtex-5 FPGA: User Guide", UG 190, chapter 8, pp. 353-381, March 2012.

[9]. LVDS Application and Data Book, *Texas Instruments*, November 2002.