A REVIEW: IN ORBIT RE-PROGRAMMABILITY OF DIGITAL SUBSYSTEMS OF SATELLITE

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ABSTRACT

Every Spacecraft/ Satellite has many digital subsystems which are widely used for a various kind of controlling and data processing applications. Field Programmable gate arrays are one of the most common elements of these subsystems considering the last minute programmability. Presently, One Time Programmable (OTP) and SRAM based FPGAs are used in the space programs. SRAM based FPGAs are reprogrammable, however this advantage of re-programmability is not used in the space applications as there is no means exist for re-programmability in space of these FPGA device. It means once the functionality of FPGA is fixed at ground, then it cannot be altered in space.

Re-programmability of these devices would be useful to fix the bugs, change the functionalities or addition of the new functionalities in due time course resulting in extension of mission life.

Here in this project the concept of the partial re-programmability and full re-programmability of SRAM based FPGA as part of the satellite or space craft would be demonstrated.

Here we project the solution to this problem. We are providing the solution by achieving re-programmability with unique protocol. This protocol will be supplied to satellite through tele-commands from the earth-stations. The decoder in the design will debug the information and will supply data to particular location in the memory. Full re-programmability can be achieved by providing whole file through tele-commands. Partial re-programmability can be achieved by providing selected amount of data for particular locations in the memory. This approach will reduce the time.

Keyword: - *SRAM based FPGAs, Re-programmability, Space applications*

1. INTRODUCTION

1.1 Which type of FPGA is to be used?

Main two types of FPGAs are used in space missions. One is Antifuse technology based FPGA and other is SRAM based FPGA. In Antifuse technology based FPGAs once the design is fused then it cannot be changed. But in space missions after launching the satellite no change can be done in this type of FPGAs. One advantage of Antifuse technology based FPGA is no radiation can affect its contents in space grated devices. But the main disadvantage is its one time programmability. Unlike Antifuse technology based FPGAs, SRAM based FPGA are multiple time programmable. On power up the data stored in the memory goes serially into FPGA to configure it. So we can say that on power up FPGA is configured through memory. But one disadvantage of SRAM based FPGA compared to Antifuse technology based FPGA is its radiation performance is not that much good.

1.2 Which type of memory is to be used?

The memory which we use in space should be non-volatile. It should be multiple times programmable. Its radiation performance should high. Area and power used by the memory should less.

1.3 Programming of memory

Three basic steps to program the memory are as follow:

1. Prepare a PROM file

2. Set the DIP switches to set the configuration mode

3. Program the memory using JTAG port

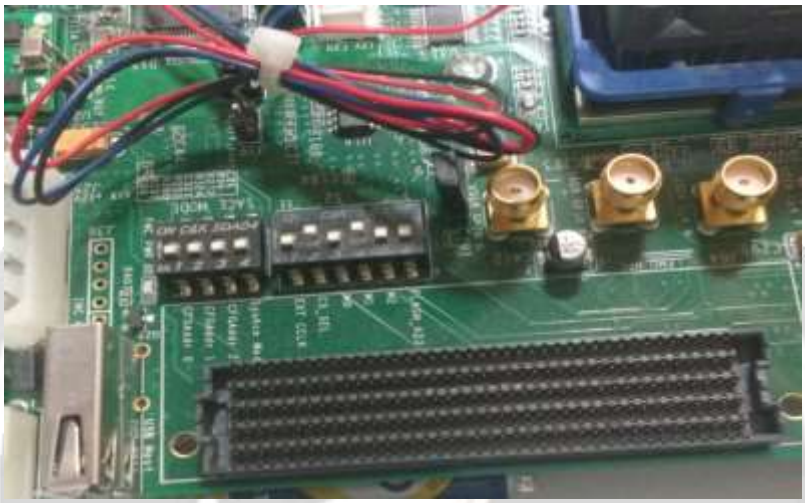

Fig. 1.1 Switch settings in FPGA board

2. LITERATURE REVIEW

Robert Giterman, Lior Atias , and Adam Teman [1] The limited size and power budgets of space-bound systems often contradict the requirements for reliable circuit operation within high-radiation environments. The smallest solution for soft-error tolerant embedded memory is given. The proposed complementary dual-modular redundancy (CDMR) memory is based on a four-transistor dynamic memory core that internally stores complementary data values to provide an inherent per-bit error detection capability. A dynamic memory-based solution, lacking internal feedback, which utilizes CDMR and single-bit parity to achieve per-bit error detection and single bit error correction capabilities. The proposed 4 T CDMR memory array was implemented in a 65-nm technology within a silicon footprint that is 47% smaller than a conventional 6-T SRAM bit cell and 2.5×–5× smaller than other state of-the-art radiation-hardened bit cells. In addition, the static power consumption of the proposed topology is more than 48% lower than the other soft-error tolerant bit cells across the entire operating range.

Xiaoxuan She and N. Li [2] The proposed scheme calculates failure probability based on critical FPGA configuration bits and performs placement and routing to reduce the failure probability as much as possible. If the calculated failure probability is still greater than the required failure rate, partial triple modular redundancy is implemented to reduce critical configuration bits until the calculated failure probability is less than the required failure rate.
It reduces area and power overhead and improves SEU vulnerability when compared with some previous schemes. A single radiation event may cause bit flipping in the storage elements. Single-event upsets (SEUs), may cause the stored value to be incorrectly changed when a radiation induced transient pulse occurs and propagates to a critical

node in memory. SEUs are a major cause of concern for static random-access memory (SRAM)-based FPGAs. The main drawback of TMR is excessive area overhead. TMR has more than 200% area overhead than the original circuit after taking into accounts the majority voter.

Zhonghua Zhou, Kang Wang, Jiapeng Wu, Qunyang Wang, Dongbo Pei [3] Due to the development of space technology, SRAM-based FPGAs, which have large scale of logic resource and restructure ability, are increasingly used by spatial electronic equipment (e.g. Navigation Receiver and many types of Space-Ground communicators). Xilinx has provided many types of highly quality SRAM-based FPGAs which can suffice the requirement of the Total Ionizing Dose (TID) of the space radiation along the lifecycle of the planet. However, the influence from Single Event Upset (SEU) is still the most important obstacle which restricts the application of these FPGAs.

An online reconfigure system for space-borne large-scale SRAM-based FPGAs with low requirement of memory space is proposed. In order to improve the reliability of the SRAM-based FPGA in space radiation environment and rehabilitate the SEU's effect, an Antifuse FPGA is used to achieve the online reconfiguration. And a pair of PROM is used to ensure the data in flash device is right. A compress algorithm is given and the corresponding decompress algorithm to save the hardware room.

Sadia Ahmad, Minahil Zahra, Salma Zainab Farooq, Adnan Zafar [4] DDR memory used for data storage in space applications is subjected to different errors. These errors are caused by various perturbations such as cosmic radiations, solar radiations, galactic noise, electromagnetic radiations and extreme temperature in space, which can corrupt the data stored in the DDR memory. Error detection techniques allow detecting such errors, while error correction enables reconstruction of the original data. These error detection and correction techniques enable reliable delivery of digital data over an unreliable communication channel. The analysis is done on the basis of time complexity, space complexity, error correction and detection capabilities, code rate and bit overhead. This paper includes comparison of Hamming, Hadamard, Golay, Repetition, Berger, Single Parity, Four Dimensional Parity, BCH and Reed Solomon Codes.

Richard Dorrance, Student Member [5] This paper compares the memory cell for the factors like cell-size, total power consumption, area used, etc. the comparison table is given below.

	SRAM	DRAM	Flash (NOR)	Flash (NAND)	MRAM	STT-RAM
Non-volatile	No	No	Yes	Yes	Yes	Yes
Cell Size [F^2]	50-120	6-10	10	5	16-40	6-20
Read Time [ns]	1-100	30	10	50	3-20	2-20
Write/Erase Time [ns]	1-100	15	1µs/1ms	1ms/0.1ms	3-20	2-20
Endurance	10^{16}	10^{16}	10^{5}	10^{5}	$>10^{15}$	$>10^{15}$
Write Power	Low	Low	Very High	Very High	High	Low
Other Power Consumption	Leakage	Refresh	None	None	None	None
High Voltage Required	No	3V	6-8V	16-20V	3V	<1.5V

Fig. 2.1 comparison of different memories

This paper concludes that the STT-MRAM and MRAMs are more suitable as per our requirement. Both have good qualities that should be considered in the space projects.

3. PROBLEM STATEMENT

1. The radiation performance of the memories used up to now is not too good. So the content of the memory is changed due to SEU.
2. Scrubbing should be done to detect and correct the error.
3. This consumes more time as well as hardware.
4. Thus the area and power of the device increases.

4. OBJECTIVES

1. Our main objective is to achieve re-programmability in orbit.
2. As well as the memory to be used should have good radiation performance.
3. It should be non-volatile and multiple times programmable.
4. As well as the scrubbing should be eliminated so that the area and power used in the device can be decreased.

5. CONCLUSIONS

From the literature review we can conclude that the memory which we should use should be non-volatile and its radiation performance should be high. As well as it should be multiple times programmable. So in our case we can use MRAM (Magnetoresistive random access memory) with SRAM based FPGA.

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