A SURVEY PAPER ON PERFORMANCE ANALYSIS OF VEDIC MULTIPLICATION TECHNIQUE USING FPGA

[1]Gaikwad Minal Nivrutti
[2]Bendkule Priyanka Devram
[3]Sonawane Punam Pandit
[4]Prof.Rana. S. Mahajan

[1]Gaikwad Minal Nivrutti, [2]Bendkule Priyanaka Devram, [3]Sonawane Punam Pandit,
[4]Prof.Rana S. Mahajan, Electronics & Telecommunication, SIR VISVESVARAYA INSTITUTE OF TECHONOLOGY, Maharashtra, INDIA

ABSTRACT

Today, it is necessary to increase the speed of multiplier as the need of high speed processors is increasing. Multiplier is a main block of any processor. Conventional processors need great hardware resources and take more time in multiplication operation. This paper present a high speed multiplier based on ancient popular Vedic mathematics. Implementation is done on digital circuits. Vedic multiplication is accomplished in the same way as that of normal multiplier using digital hardware. In this paper a comparison of concerned multipliers in 8, 16 and 32bits multiplications is performed. 8 bit and 16bit urdhva algorithm shows 50% improvement in delay than that of nikhilam, whereas 100% better than that of binary multiplier. 32bit nikhilam multiplier gives 52% improvement in delay than that of urdhva multiplier and 16% better than that of binary multiplier. Multiplication is an important factor in arithmetic operations and is carried Out in variation of digital signal manage applications. As multipliers take a long time for execution so there is a need of fast multiplier to save the execution time. This paper describes the multiplication using ancient indian vedic mathematics multiplication techniques. Vedic mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 sutras. The techniques described in this paper are nikhilam sutra, urdhva tiryakbhyam and Karatsuba-of man and the performance analysis of these techniques is obtained. Modalism tool is used for simulation and the results obtained are compared on the basis of time delay of multiplication. This paper also describes the deliberateness and the fastness of different multiplier techniques Compared with each other.

Keyword: - *Vedic mathematics, binary multiplier, urdhva triyagbhyam, nikhilam, Vedic multiplier, speed.*

1. INTRODUCTION

Veda is the Sanskrit word which means knowledge. The word Vedic is derived from the word Veda. The concept of ancient Vedic Mathematics was brought by Sri Bharati Krishna Tirthain 1965. This concept is based on sixteen sutras or principles or aphorisms. It is a system of reasoning and mathematical working based on ancient Indian teachings called Veda. This method is very fast, efficient and easy to learn and use. It simplifies arithmetic and algebraic operations (multiplication, divisibility, complex numbers, squaring, cubing, and square and cube roots).With the latest technological developments in the field of computers and signal processing applications, the need for high speed processing has increased. Speed, area and power are very

Important factors to be considered and to improve the performance of any processor. The multiplier is a hardware block of any computing system. Multipliers are the commonly used architectures inside the processor. Multipliers hold a significant role in different DSP applications such as digital filtering, digital communication and Fast Fourier transform. The amount of circuitry involved is directly proportional to the square of its resolution. For multiplication, algorithms performed in DSP applications latency and through put are the two major factors.

For delay consideration. Real delay of any computation of a function is latency. Throughput is the measure of how many multiplications can be performed in a given period of time. Multiplier is not only a high delay block but also a major source of power dissipation .Hence this reason to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations. Data processing applications, digital signal processors and microprocessors in specific integrated circuits use the arithmetic operations of two binary numbers. Thus multipliers and Binary adders are important building blocks in VLSI Circuits. A huge set of components have been used in high performance systems such as ALU, filters, microprocessors, digital signal processors, etc. Multiplier is necessary because most of the DSP calculations involve the use of multiply accumulate operations. It is one of the most essential hardware blocks in image scheming, signal processing and arithmetic operation. In case of higher order multiplication, a huge number of adders are to be used to perform the partial product operation. The need of low power and high speed processor requires high speed multiplier. The Vedic multiplication technique is based on 16 Vedic principles. With technological advancement, a lot of researchers have been tried to design multipliers which other either of the following regularity of layout, low power consumption and not only less area but also combination of these in a multiplier. The Vedic mathematics is concerned with the Vedic mathematical formulae and it uses in application to various branches of mathematics and is considered very close to the way a human mind works.

1.1 Objective and Aim of Work

The primary Goal of this project is the use of Vedic mathematics lies in the fact that it reduces the typical calculation in the conventional mathematics to very simple once. Vedic mathematics is a several effective algorithms, ancient Indian Vedic mathematics, which has utilized for multi-plication to improve speed, area parameters of multipliers. After implementing the sutra it has been observed that Vedic multiplication is efficient in terms of speed.

2. LITERATURE SURVEY

S. Kokila et.al. (2012) analyzed VHDL implementation of fast 3232 multiplier based on Vedic mathematics. High speed, low power, less area and delay can be achieved by designing multiplier in VHDL, as it give effective utilization of structural modeling. Usage of carry save addition in the multiplier architecture reduces the delay in the multiplier design. It provides a systematic design methodology for fast and area efficient digital multiplier based on Vedic mathematics the architecture of the designed Vedic multiplier comes out to be very similar to that of the popular array multiplier and hence it should be noted that Vedic mathematics provides much simpler derivation of array multiplier than the conventional mathematics. Many digital signals processing operation requires several multiplication and for the same we need very fast multiplier for a wide range of requirements for hardware and also for high speed applications. This paper presents a systematic design methodology for fast and area efficient digit multiplier based on Vedic mathematics. It consumes less power when compared with other multiplier designs and the design complexity gets reduced for inputs of large number of bits and modularity gets increased. Padmanabin Gopala Krishna and Gangavarapu Kiran Kumar (2013) described modeling of towering speed and area competent Vedic multiplier using Urdhva Tiryaghbhyam sutra. The implemented design is efficient in terms of area and speed compared to its implementation using array and booth multiplier architecture. It can be easily implemented in hardware and by using basic nibble multiplication unit, the higher bit multiplication can be construct which will make modification easier. The implemented design made debugging easier and efficient in area and speed and hence area consumption is less. Therefore the multiplier architecture uses fewer resources such as less number of multipliers and adders and is flexible in design.

Reliable and robust operation is significant for metro systems. As pointed in, driverless train operating systems require trains to stop at any point if necessary, such as the evacuation of people in emergency circumstances and train malfunctions. It is showed that the long-term unreliability can reduce the passenger demand and metro effectiveness. The increase in the level of automation enhances the reliability and robustness of urban rail transit

3. FEATURES

- The use of Vedic mathematics lies in the fact that it reduces the typical calculation in the conventional mathematics to very simple once.
- Vedic mathematics is a several effective algorithms, ancient Indian Vedic mathematics, which has utilized for multiplication to improve speed, area parameters of multipliers.
- After implementing the sutra it has been observed that Vedic multiplication is efficient in terms of speed.

4. ADVANTAGES

- The main advantage is its regularity when compared to other multipliers.
- It is easy, simple, direct and straightforward.
- The partial products and their sums are calculated in parallel.
- The Sutras are easy to understand, easy to apply and easy to remember, and the whole work can be truthfully summarized.

5. APPLICATIONS

- Mainly used in Digital Signal Processor.
- Can be applied in those designs in which smaller blocks are used to build higher blocks.
- Can be efficiently applied in any Signal Processing applications.

6. FUTURE SCOPE

- Future work includes the integration of the divider block, multiply and accumulate (MAC) unit, thereby making it into a Vedic Arithmetic and Logical unit (ALU).
- Reducing the time delay is very essential requirement for many applications and Vedic Multiplication technique is very much suitable for this purpose.
- The idea proposed here may set path for future research in this direction.

7. CONCLUSION

Thus we have implemented the formulas of Vedic Multiplier to implement in SPARTAN 3 using VHDL and compare the speed, delay, and use of adder.

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