A THERMALLY OPERATABLE BOOSTER WITH INTERNAL STARTUP CIRCUIT WITHOUT USING EXTERNAL VOLTAGE

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Abstract

In this paper, design for complete thermal energy harvesting power supply for boost converter without using any reference voltage. The designed power supply includes an internal startup and does not need any external reference voltage. The startup circuit includes a prestart up charge pump (CP) and a startup boost converter. The prestart up CP consists of an ultralow-voltage oscillator followed by a high efficiency modified Dickson. Forward body biasing is used to effectively reduce the MOS threshold voltages as well as the supply voltage in oscillator and CP. The steady-state circuit includes a high-efficiency boost converter that utilizes a modified circuit. The system is designed so that no failure occurs under overload conditions. Using this approach, a thermal energy harvesting power supply has been designed using 130-nm CMOS technology with low dropout regulator. Finally the output obtained is 2.5 V in 1 second with the load of 100 kiloohm . The circuit is simulated using Tspice and simulation results are verified.

Keywords- *Thermoelectric Generator, Modified Dickson circuit, Charge pump, Internal startup.*

1. INTRODUCTION

As the ultra large scale integration is attained now, one of the major problem faced by any electronic devices are their batteries. The size of the battery does not become small in size in comparison with the transistor sizing. Even when the transistor size is reduced to great extend, the device does not get small because of large area occupied by the battery. One of the alternatives to replace the battery in any electronic device is by using energy harvesting technique. In this paper, thermal energy harvesting power supply is designed. This could eventually replace battery in any electronic device.

A pacemaker is a small device, contains a powerful battery, electronic circuits, and computer memory that together generate electronic signals. One of the main problems about pacemakers is their batteries. As the capacity of the batteries is limited, they limit the lifetime of pacemakers. After a period of five years, one should undergo a surgical procedure to replace the battery of the pacemaker. In addition, approximately 60% of the volume of a pacemaker is taken up by its batteries. Eliminating these batteries effectively reduces the dimensions of the pacemaker.

Another case is implementing the TEG which will eliminate the use battery in the electrical device like pacemaker by using the temperature difference from body making it use of by means like battery to provide 2.5v using boost converter with internal startup circuit.

A voltage source in series with an internal resistance is a representative of TEGs. The open-circuit output voltage of the TEG is proportional to the temperature gradient. The voltage regulator is used for providing the regulated voltage to the internal startup circuit to operate with high reliability to get the output steady state in just milliseconds.

In Existing System, a design is proposed to obtain the 2.5 v from 50mv that obtain the steady state in 1 seconds. Existing system contain a thermal energy harvesting power supply has been designed using 180 nm CMOS technology. Final output of the thermal harvesting system with internal startup circuit for pacemaker was obtained as 2.5 V in 8s, which had quit large delay compare to proposed system.

2. PROPOSED SYSTEM

An ultralow-voltage low-power oscillator generates the required clock phases for a CP system. A high-efficiency modified Dickson CP is used to increase the input voltage to the extent that is needed for the whole circuit to operate successfully. The output voltage of the TEG is applied to the input of CP. Consequently, CP begins to charge a small internal capacitor (CPST*)* placed at its output and the capacitor voltage (VPST*)* begins to rise.

When VPST reached a predefined value, the output of the comparator 1 (VCMP) sets. This enables the startup boost converter (SUBC) to work. The SUBC provides the required clock phases for the steady-state boost converter (SSBC), while the SSBC output voltage (VOUT) does not reach a preset value. When this is achieved, the output of the comparator 2 (VCMP2) sets and the normal operation of the system begins.

In this mode, the SSBC itself generates its clock phases. A multiplexer is used to select the source of the required phases for the SSBC based on the VCMP2, whether from SUBC (VPH,ST*)*, or a self-generated one (VPH,SS*)*. In normal operation, the SSBC no longer requires the pre-startup CP and SUBC, so it can continue to work on its own. It is designed so that VOUT becomes a regulated output voltage with a low voltage ripple.

If, for any reason, VOUT falls out of the range of the output voltage, immediately, the SUBC becomes active and charges the output voltage until it comes within the range. This operation takes time no more than 400 ms. Therefore, the system offers high reliability.

3. BLOCK DIAGRAM

The Block diagram shown in Fig 1 is the proposed system architectural design of the a thermally operatable booster with internal circuit.

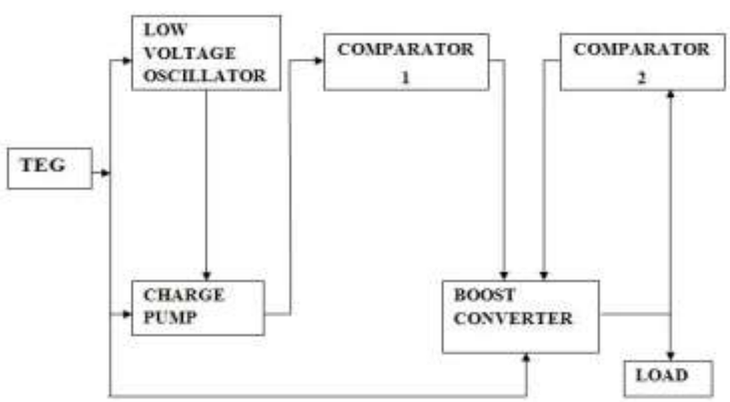

Fig -1: Block diagram of proposed system

A voltage source in series with an internal resistance is a representative of TEGs. The open-circuit output voltage of the TEG is proportional to the temperature gradient. The voltage regulator is used for providing the regulated voltage to the internal startup circuit to operate with high reliability to get the output steady state in just milliseconds. The proposed system is the enhancement of the existing system to their steady state performance.

An ultralow-voltage low-power oscillator generates the required clock phases for a CP system. A high-efficiency modified Dickson CP is used to increase the input voltage to the extent that is needed for the whole circuit to operate successfully. The output voltage of the TEG is applied to the input of CP. Consequently, CP begins to charge a small internal capacitor (CPST*)* placed at its output and the capacitor voltage (VPST*)* begins to rise.

When VPST reached a predefined value, the output of the comparator 1 (VCMP) sets. This enables the startup boost converter (SUBC) to work. When the SSBC output voltage (VOUT) does not reach a preset value. When this is achieved, the output of the comparator 2 (VCMP2) sets and the normal operation of the system begins.

If, for any reason, VOUT falls out of the range of the output voltage, immediately, the SUBC becomes active and charges the output voltage until it comes within the range. This operation takes time no more than 400ms. Therefore, the system offers high reliability.

The maximum allowable load for the boost converter is defined when all of the power of the inductor is transferred to the capacitor. In this way, the inductor current become zero at the end of the clock pulse. The boost converter which boost the input voltage of the 50 mV to 2.2 V by the switching of the transistor and charging and discharging of the inductor. The output of the proposed system can tolerance the load of about 100 Kiloohm and produce the regulated output voltage.

ADVANTAGES

The advantages of proposed system are reached steady state in 1second from 50 mV to 2.2 V and also include the designed circuit can withstand the load of about 100 Kiloohm continuously to provide the maximum power of 260uw.

APPLICATIONS

Its main idea is to be used in bio-electronic device like pacemaker instead of the battery, since it only has few years of durability.

4. RESULTS

The process that is performed in the system is shown through the below snapshots. This project is based on VLSI technology. T-SPICE is the tool which is been used here. In T-SPICE, s-edit is used for schematic process of the project which include the designing the circuit with the required component from library file. In which intent to create a t-edit which is net-list as it used to edit the required parameter on the component and the modification can be processed here.

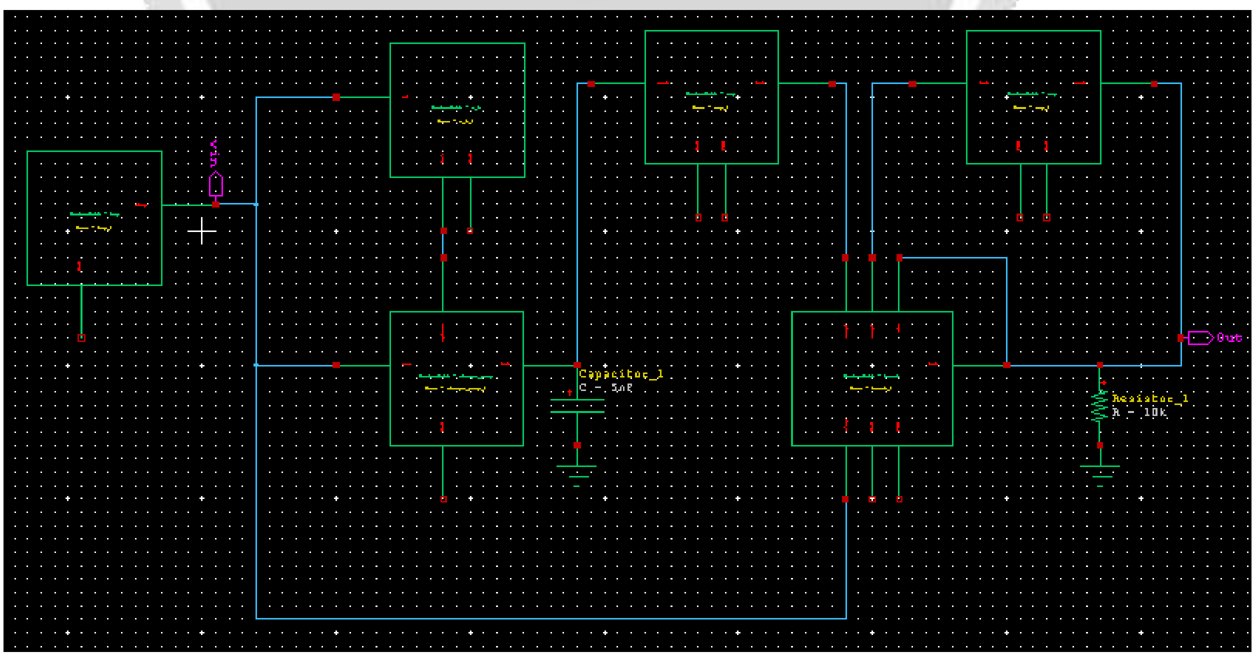

Fig-2: Schematic diagram of proposed system

Figure 2 shows the output obtained for the boost converter which takes the input from TEG of 50 mV and the clock phase from the control circuit to switch the transistor nMOS. The output obtained at boost converter is 2.2 V and reached the steady state in 1s.

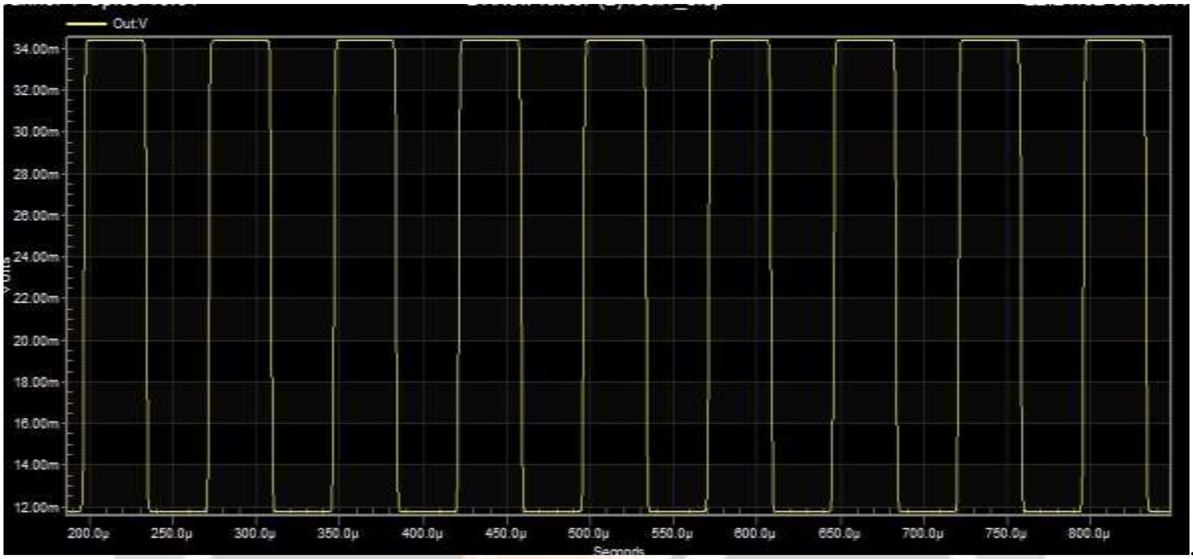

Fig -3: Output of the proposed Low power oscillator

As the fig-3 shows the output of the low power ring oscillator which takes the 50 mV as the input and produce the output of 38 mV clock pulse.

Fig-4 shows the output of the charge pump, which it takes the input from TEG and the output of ring oscillator is provided to it. The charge pump is the proposed modified Dickson circuit that produce the output voltage of about 1 to 2 V. As the Dickson circuit is connected in 5 stages in cascade manner to double up voltage. The output obtained has the ripple voltage which cannot be used for control circuit. In order to eliminate the ripple voltage, the output of charge pump is given to self hysteresis comparator.

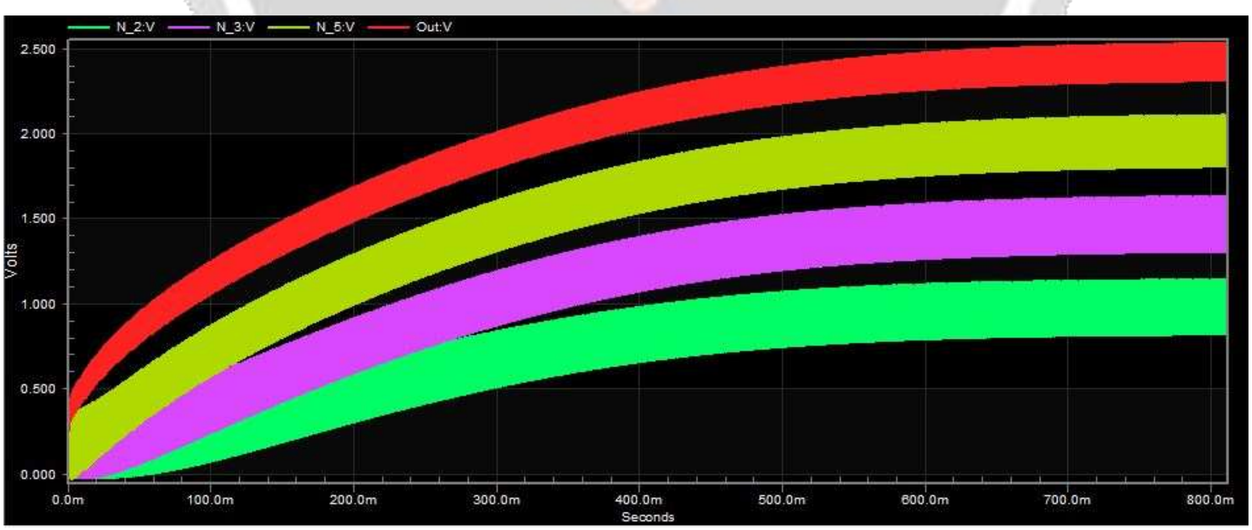

Fig-4: Transient response output of charge pump

As shown in figure 5 When the CMP1 is enabled by the charge pump pre-scale output voltage value of 1.3 to 1.5v, which intent enable the oscillator for the boost converter for switching the transistor.

As the result, the voltage on CPST remains almost constant, and the voltage on COUT rises. VOUT rises until it reaches VTH,H,CMP2. When this is achieved, VCMP2 sets, and the multiplexer disconnects the clock phases of the SUBC from the SSBC and lets the SSBC to generate the clock phases for itself.

From this time, the system can provide the required power for the pacemaker. The comparator high and low threshold voltages are set to be 2.6 V and 1.5 V for comparator 1 and 2.6 and 2.5 V for comparator 2, respectively.

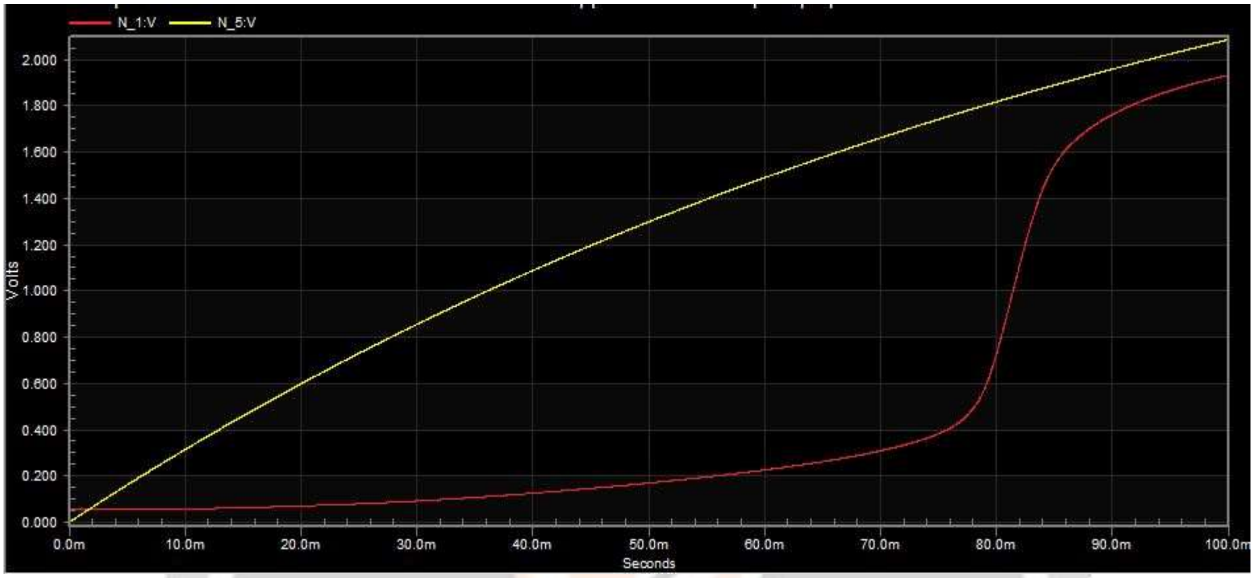

Fig-5 Transient analysis of comparator

Fig-6 shows the output obtained for the boost converter which takes the input from TEG of 50 mV and the clock phase from the control circuit to switch the transistor nMOS. The output obtained at boost converter is 2.2 V and reached the steady state in 1s.

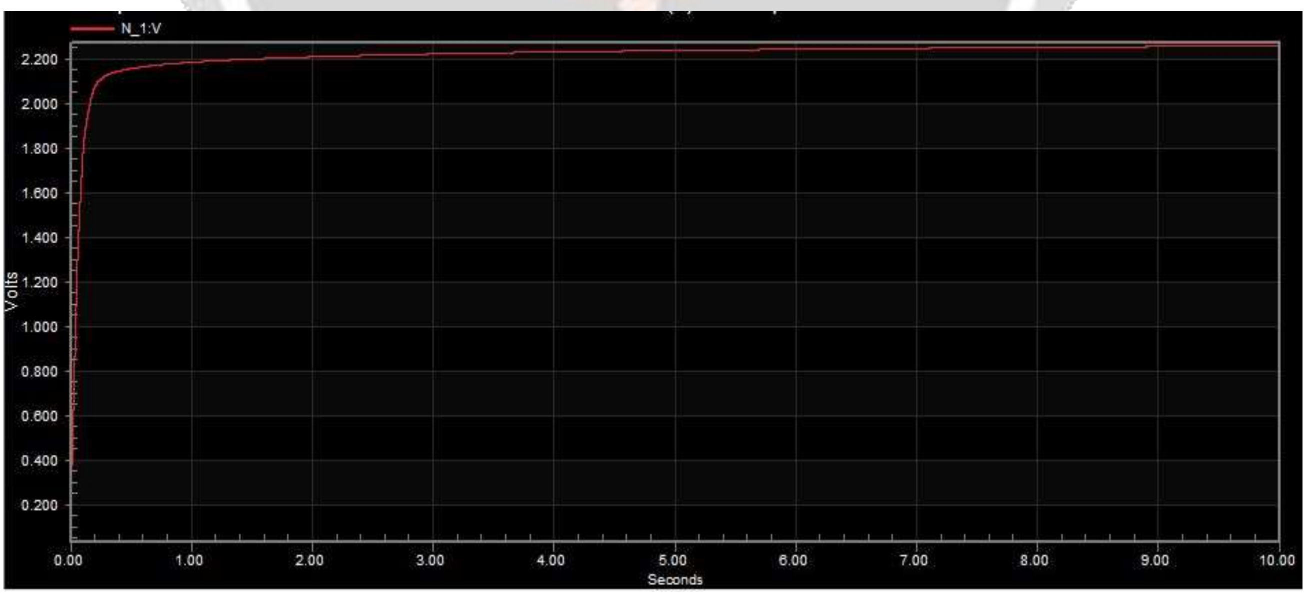

Fig-6: Transient Response of Proposed System

The circuit mode is changed to the startup mode and the load is detached from the whole system. In the startup mode, the circuit charges VOUT until VCMP2 is set. The circuit enters the steady state mode again and normal operation of the circuit is retrieved.

Figure 6 shows the output of the proposed system which delivers 2.2 V with the maximum output power of 260 μW.

4.1. Comparison of existing and proposed system

The Comparison of existing and proposed system of the thermal operate booster without any reference voltage using internal startup circuit is shown the table 4.1. The parameter such as CMOS Technology and output voltage with input voltage is discussed in table 4.1 and compared with existing System.

Table 4.1 Comparison of Existing and Proposed System

Parameter	**Existing System**	**Proposed System**
CMOS Technology	180 nm	130 nm
Input Voltage	50-60 mV	50 mV
Output voltage	(1-3) V	(2-3) V
Maximum Output Power	130 μW	260 μW
Steady State Time	8s	1s

5. CONCLUSION AND FUTURE ENHANCEMENT

A complete energy harvesting power supply for implantable pacemakers has been proposed in this paper. A TEG provides the input voltage for the circuit from the temperature difference found between the body and the ambience. Using the FBB technique, a low-voltage oscillator and a low-voltage CP have been designed and simulated which enable the circuit to start up from input voltages as low as 60 mV. Applying a 40-mV input voltage, the output voltage of the proposed power supply is 2.2 V under any load conditions. The circuit includes an internal reference voltage. No extra reference voltage source is needed. The maximum deliverable power to the load is 130 μW. The circuit was designed in such a way that overload conditions are tolerated. The TSPICE simulation results prove the effectiveness of the proposed circuit.

In future, designed system would be enhanced in increasing the steady state at very shorter duration then the proposed duration and the invention CMOS technology and VLSI design methodology provide the designing of circuit in area efficiency and less power consumption.

6. REFERENCES

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