A THREE PHASE GRID CONNECTED PHOTOVOLTAIC INVERTER WITH DC CURRENT SUPPRESSION FEATURE

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ABSTRACT

The Photo Voltaic inverters without the isolation transformer become more attractive due to higher efficiency and lower weight and other offered mentioned advantages. However, it may have dc offset current while injecting generated AC to the grid which is critical to the power system. In this paper, a simplified control strategy of suppressing dc current injection to the grid connected for PV inverters is analyzed using MATLAB simulink software. It is based on the idea of accurately sensing the dc offset voltage of PV inverter output which is fed to Grid. Since dc component of the inverter output can be eliminated, dc injection to the grid can be effectively suppressed. To show the effectiveness of the proposed method FFT analysis has implemented to the proposed method.

Keyword: - *Inverter, DC offset suppression, FFT analysis, PV, Grid.*

1. INTRODUCTION

The rapid development of renewable generation boosted the need for efficient, cheap, and robust converters that would interface them to the grid, without compromising the quality of supply for the end user. Most renewable provide a dc source of electric power, thus proper interfacing to the grid requires at least an inverter. Often, due to the low voltage acquired from sources such as domestic wind turbines, solar arrays or fuel cells, a boost converter or/and a transformer (if isolation is required) is added at the dc or ac side, respectively, in order to boost the voltage to the appropriate level. The most common type of commercial inverter used for this kind of applications is a variation of sinusoidal pulse width modulation full-bridge inverter. The simplicity of the design provides robust operation and simple control, but the harmonic content of the output requires a low-pass filter to comply with the standards.

Two disadvantages of this application are the increased size and cost due to the filter and the losses of the semiconducting switches performing the inverting operation at the inverter bridge (four) and the boost converter (one), usually, at a non acoustic frequency. Several PWM methods have been developed in order to reduce the harmonic content. Selective harmonic elimination solves the transcendental equations characterizing harmonics, so that appropriate switching angles are computed for the elimination of specific harmonics at the output [1]–[3].
Theoretically, these methods can provide a satisfying harmonic content. However, the solution of these equations is computationally intensive, thus, quite difficult to be done online. In small-scale applications, where powerful digital signal processors (DSPs) are not currently an option due to their higher cost, either switching angles are calculated offline [4]–[8], or the equations are liberalized before they are solved [9], [10], or an approximate solution is sought where the topology permits it [11]. Other methods include modification of the carrier signal [12]–[14] or the reference sine wave [15], [16]. All of them, though, are open-loop control schemes, which assume a known and perfectly constant dc source (i.e., harmonics induced to the grid by an inductive source are ignored) and ignore the existing harmonic content of the grid voltage or the distortion caused by the load. In simple terms, they aim to reduce the harmonics created by the PWM itself, rather than improve the harmonic content at the terminal bus, which is affected by the PWM only partially.

Authors in [17] and [18] suggested a sine-wave modulated buck–boost converter cascaded with a polarity changing inverter. Simulation results demonstrate that this topology works exceptionally well, producing an ac sine-wave output, which depends upon the reference sine-wave amplitude Furthermore, switching losses are practically limited to the single semiconducting switch of the buck–boost converter. Additionally, there is no need for a big and expensive stabilizing electrolytic capacitor at the dc bus. Low inertia is required at the common bus of the two converters, so thin-film, low capacity, and long life capacitor is used, instead. However, there are drawbacks for this topology and the previously presented modulation methods, which are not mentioned in [17] or [18]. First, voltage is usually not zero when the inverter swaps output polarity. Low-order odd harmonics are created and THD is compromised. Second, when the dc source is inductive, e.g., a wind turbine generator, the output of the sine-wave modulated buck–boost converter is not an ideal rectified sine anymore. In this case, the waveform peaks are shifted to higher angles than 90◦; a distortion which is visualized as a significant third harmonic in the Fourier analysis.
In this study, we present a simple, but effective, improvement of the sine-wave modulation of the buck–boost converter, so that the output capacitor's remaining voltage is minimized when the inverter swaps output polarity. Additionally, a low-order harmonic elimination method, superimposed on the buck–boost modulation, is presented. The initial aim of the method was to remedy the output distortion due to the inductive power source, but in practice it improves the harmonic content of the output whether the reason of the distortion is the source, the load, the synchronized grid, or a combination of the aforementioned elements. Similarly, to the methods reviewed in [13], specific harmonics are injected in order to improve the harmonic content of the output. However, these methods share the feature that the injected harmonic amplitudes are pre calculated, according to the expected harmonic distortion created by the PWM itself [14], [15].

Sharma first introduced a detecting method of dc offset voltage. A small 1:1 voltage transformer and an *RC* circuit were used to detect the dc offset voltage at the inverter output in the full-bridge grid-connected inverter. And the dc offset in the grid current was eliminated by feeding back the dc offset voltage to the PI controller. Alfock and Bowtell [19] continued studying this method by establishing the mathematical model and verified it. He and Xu [16] used a voltage sensor at the inverter output consisting of a differential amplifier and a low-pass filter. DC offset detected at the output of the low-pass filter is fed back to the controller. A mathematical model is provided in this paper. However, the experimental results under grid mode were not given. The voltage-detection control method uses sensors to detect the dc voltage offset across the ripple filter [15]. This method implies that very low dc voltage across the filter is measured, which is sensitive to noise. A dc offset detection method is proposed by Buticchi [16]. However, this method needs a nonlinear inductor. Hence, a customized inductor should be designed according to specific systems. In this paper, a novel control strategy to suppress dc current injection of transformerless PV inverters to the grid is investigated.

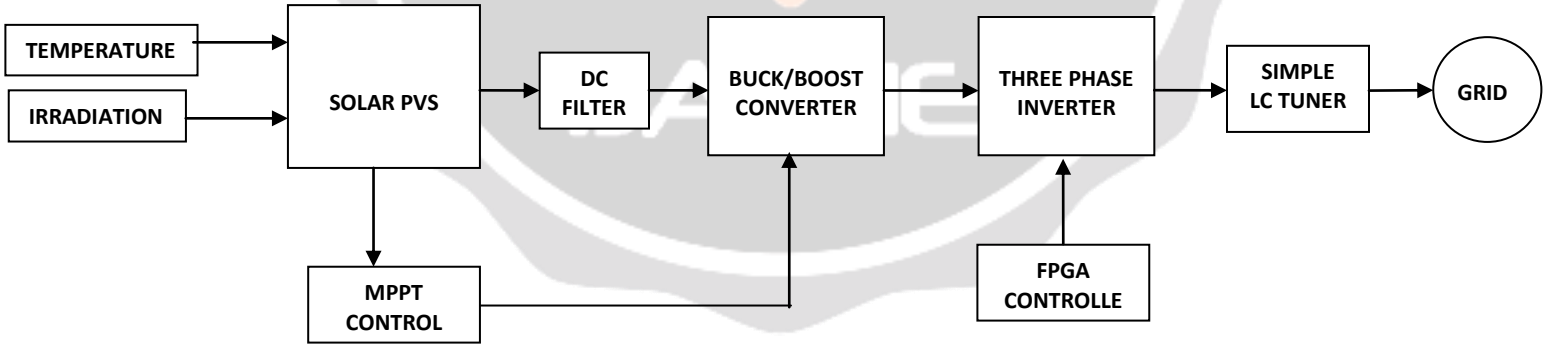

Fig-1: Block diagram of proposed system

2. PROPOSED TECHNIQUE

The full-bridge PV inverter without output isolation transformer is shown in Fig. 1. From Fig. 1, the grid current reference *i*ref can be expressed as

$$i_{ref} = I_{ref} \cos \theta \ldots\ldots\ldots\ldots\ldots(1)$$

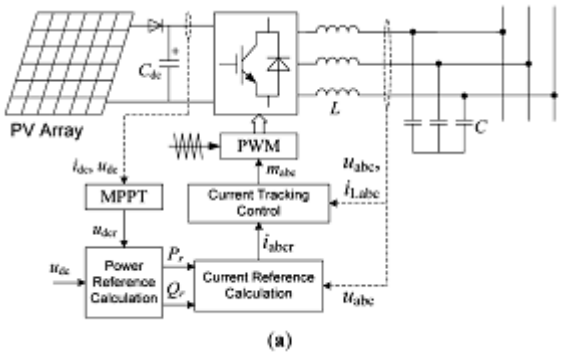

Fig-2: Existing scheme diagram of PV grid-connected inverter.

where *I*ref is the amplitude of grid current command, and θ is the phase angle of grid current which is synchronized with grid voltage by phase-locked loop. PV inverter output generally has dc offset voltage component, which results from disparity of power modules, asymmetry of driving pulses, detection error of current, etc. Traditionally, a transformer is inserted between the PV inverter and the grid. Although the PV inverter output may have dc voltage component, there is no dc current injection to the grid. However, in the case of the PV inverter without isolation transformer, the inverter output dc offset may cause a significant dc current injection to the grid, which may violate the grid connection standards and cannot be neglected [20]. In order to effectively restrain dc current injection to the grid, a control strategy for a single-phase PV inverter without the isolation transformer is shown in Fig. 2 [17], [24]. Compared with Fig. 1, an extra dc offset voltage suppression loop is added to the previous control scheme. The dc suppression loop is composed of a differential amplifier, a low-pass filter, and a dc controller.

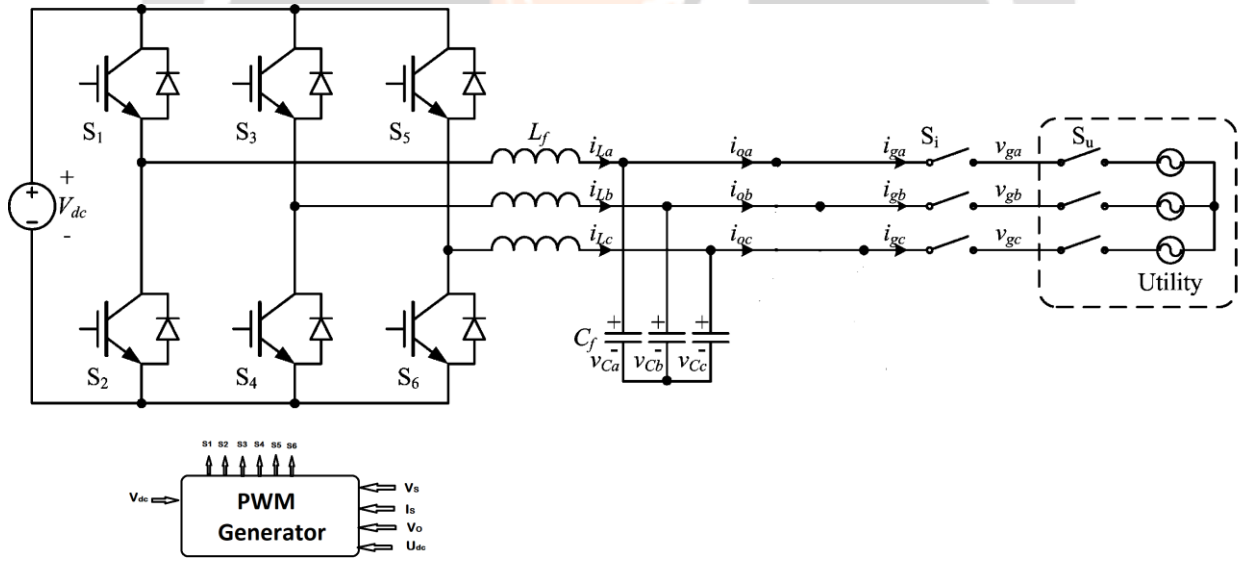

Fig-3: proposed scheme for PV grid-connected inverter planned for three phase system

The input of dc suppression loop is u_{AB} , which is a high frequency PWM waveform sampled between the point A of inverter bridge-leg 1 and the point B of inverter bridge-leg 2. DC offset voltage of *uAB* is accurately extracted by a differential amplifier and a low-pass filter. Then, it is compared with inverter dc voltage reference U_{dc} ref which is set to zero, and dc offset voltage error is obtained. The error is regulated by the integral controller. Finally, the output of dc controller ΔUdc, which is also the output of dc suppression loop, is added to the grid current reference *i*ref of the grid current control loop.

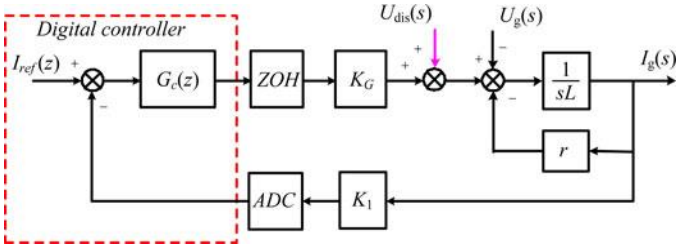

Fig-4: Control diagram for PV grid-connected inverter.

The novel control strategy has two significant features. The first is that the differential amplifier is used to sample the dc offset voltage between the two bridge-leg middle points of full bridge inverter. To accurately detect the dc offset voltage of the inverter switch-side output voltage *uAB* , a high-precision differential amplifier with low offset and high common-mode rejection ratio is needed. The using of differential amplifier can not only reduce the cost, but also avoid the zero-drift by using Hall-effect sensors. The second one is that dc suppression loop can suppress inverter output disturbances. Therefore, the dc current injected to the grid can be effectively suppressed.

3. ANALYSIS OF DISTURBANCE SUPPRESSING EFFECT

The control block diagram of PV grid-connected inverter is shown in Fig. 4.3, which is derived from Fig. 4.1, where *I*ref (*z*) is current reference of the inverter, *Gc* (*z*) is digital controller of current loop, and *KG* is the gain from the output of current controller *Gc* (*z*) to inverter switch-side voltage. *U*dis(*s*) represents the disturbance caused by the turn-on and turn-off difference of the four switches, the saturation voltage difference of the four switches, the gate drive signal delay difference of the four switches, and so on. *L* is the output filter inductor. *r* is the equivalent resistance of output filter inductor *L*. *Ig* (*s*) is the grid current of the inverter. *K*1 is the feedback gain of current loop. ADC is the analog-to-digital converter which converts the analog sampling value of *Ig* (*s*) to digital one. *ZOH* is zero-order holds which is connected in series between the output of digital controller and *KG*. From Fig. 4.3, the transfer function in s-domain from disturbance source *U*dis(*s*) to grid current *Ig* (*s*) with the original control scheme can be derived as follows:

$$\frac{I_g(s)}{U_{\text{dis}}(s)} = \frac{s \cdot e^{-(T_s \cdot s)}}{s(sL + r) + K_1 K_G (K_{pi} s + K_{ii})} \qquad (2)$$

where *Kpi* and *Kii* are the proportional and integral coefficient of current controller, respectively. $e^{-(s \cdot T\ s)}$ is the delay effect considering time delay caused by ADC, digital computation and ZOH, where *Ts* is the duration of sampling period [38], *Ts*=1/*fs*, *fs* is switching frequency of PV inverter.

In theory, if both the feedback gain of current loop *K*1 and ADC are accurate enough, the dc offset of grid current can be eliminated with PI regulator. However, it is actually limited by ADC resolution and accuracy of the current sensor. The maximum grid dc current detecting error Δ*Ig* can be calculated as

$$\Delta I_g = \Delta I_{g1} + \Delta I_{g2} \qquad (3)$$

where Δ*Ig*1 represents error caused by ADC resolution. Δ*Ig*2 represents error caused by the error of current sensor and conditioning circuit.

A. Analysis of Detecting Error Caused by ADC

When *N*-bit ADC is adopted, the DSP sampled digital value *Igs* of the grid current *Ig* for the PV grid inverter can be expressed as

$$I_{gs} = I_g \times \frac{2^N}{(1+\beta) \times I_{p\_p}} \qquad (4)$$

where *Ip p* is peak to peak value of the rated grid current, and β represents the overload coefficient of the grid current. From (4), the detecting error of the grid dc current Δ*Ig*1 caused by the ADC resolution is given by

$$\Delta I_{g1} = \frac{(1+\beta) \times I_{p\_p} \times \Delta I_{gs}}{2^N} \qquad (5)$$

where Δ*Igs* is ADC error of the DSP.

B. Analysis of Detecting Error Caused by a Current Sensor and Conditioning Circuit

The grid dc current detecting error Δ*Ig*2 caused by the error of the current sensor and conditioning circuit is given by

$$\Delta I_{g2} = \frac{\Delta I_{\mathrm{Lem}}}{K_1'} + \frac{\Delta I_{\mathrm{Con}}}{K_2'} \qquad (6)$$

where Δ*I*Lem and Δ*I*Con represent the error caused by current sensor and conditioning circuit, respectively. *K*_1 is current conversion ratio of the current sensor. *K*_2 is gain of the conditioning circuit. Therefore, by substituting (5) and (6) into (3), the maximum gird dc current detecting error Δ*Ig* can be calculated as

$$\Delta I_g = \frac{(1+\beta) \times I_{p\_p} \times \Delta I_{gs}}{2^N} + \frac{\Delta I_{\mathrm{Lem}}}{K_1'} + \frac{\Delta I_{\mathrm{Con}}}{K_2'}. \qquad (7)$$

Let us take a PV grid inverter as an example with parameters listed as follows. Rated power *Pe* = 3 kW, rated grid voltage *Ug* = 220 Vrms , peak-to-peak value of the rated grid current *Ip p* = 38.6 A, overload coefficient of the grid current β = 0.2, the current sensor accuracy Δ*I*Lem = ±0.1 mA, and conversion ratio of the current sensor *K*_1 = 0.0015. The conditioning circuit error Δ*I*Con = ±0.2 mA, the gain of conditioning circuit *K*_2 = 0.25. The ADC error Δ*Igs* = ±1.5 LSB.

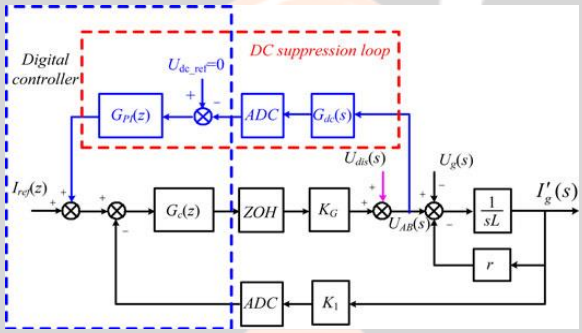

Fig-5: Control block diagram with novel control scheme.

By substituting the above parameters into (7), the relationship between the ADC bit *N* and the total grid dc current detecting error Δ*Ig* is drawn in Fig. 4. The solid line shows the relationship between the ADC bit *N* and the grid dc current detecting error Δ*Ig* with the original control scheme. The dotted line is the dc current limit standard [9]–[11]. It can be seen from Fig. 4.4 that the grid dc current detecting error is larger than the standard value with traditional control.

4.3 TUNING OF PI CONTROLLER IN THE DC OFFSET SUPPRESSION LOOP

Fig. 4.6 shows the equivalent control diagram with dc offset suppression loop, which is derived from Fig. 5.

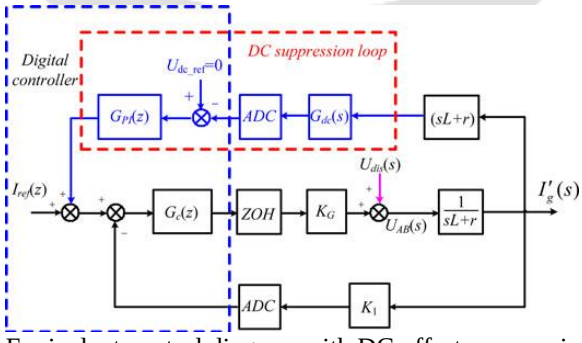

Fig-6: Equivalent control diagram with DC offset suppression loop.

From Fig. 6, the open-loop uncompensated transfer function of equivalent dc suppression loop can be expressed as

$$G_{\mathrm{dc\_offset}}(s)=\frac{K_G\cdot G_{\mathrm{dc}}(s)\cdot\left(K_{pi}s+K_{ii}\right)\cdot(sL+r)\cdot e^{(-sT_s)}}{Ls^2+\left(r+K_G\cdot K_1K_{pi}\right)s+K_G\cdot K_1K_{ii}} \tag{14}$$

where *Kpi* and *Kii* are the proportional and integral parameters of current loop, respectively, which are designed as: *Kpi* = 1.2 and *Kii* = 1560. (The bandwidth of current loop is designed as 800 Hz.) *G*dc(*s*) is the feedback gain which includes differential amplifier and low-pass filter, which can be expressed as

$$G_{\mathrm{dc}}(s)=\frac{2}{\left(1+\frac{s}{2\pi f_{LP}}\right)^2} \tag{15}$$

4 SIMULATION RESULTS

In this section a novel control strategy to suppress dc current injection of transformerless PV inverters to the grid is investigated using MATLAB simulink software. The Fig-7 and 8 represents the overall design of the proposed circuit and solar PV system.

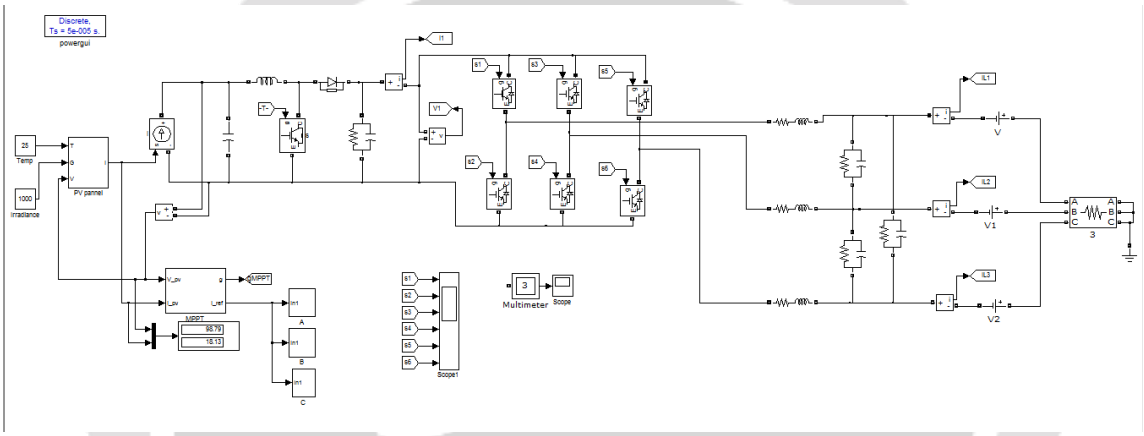

Fig-7: proposed three phase grid connected PV inverter system using MATLAB software

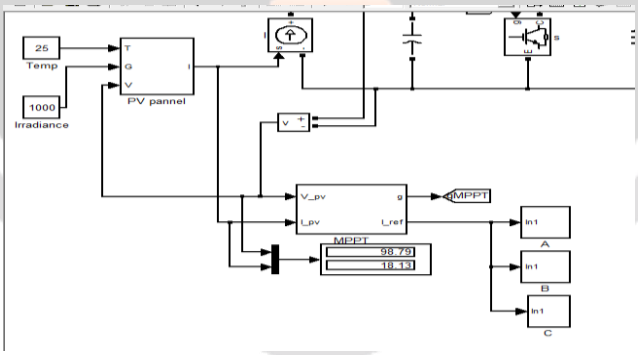

Fig-8: MPPT control solar PV Systems

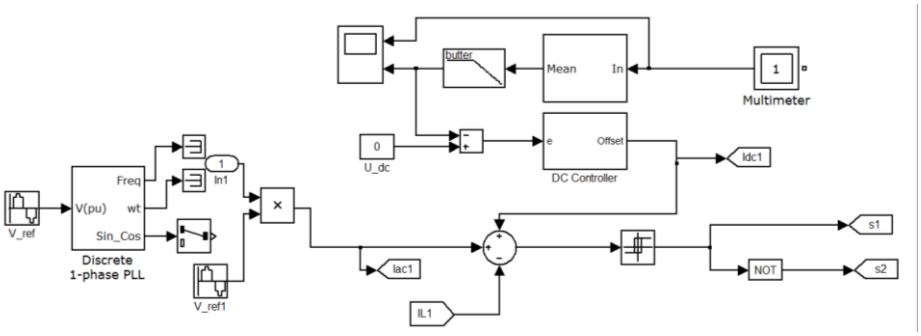

Fig-9: Proposed Control Scheme has extended to three phase inverter scheme successfully

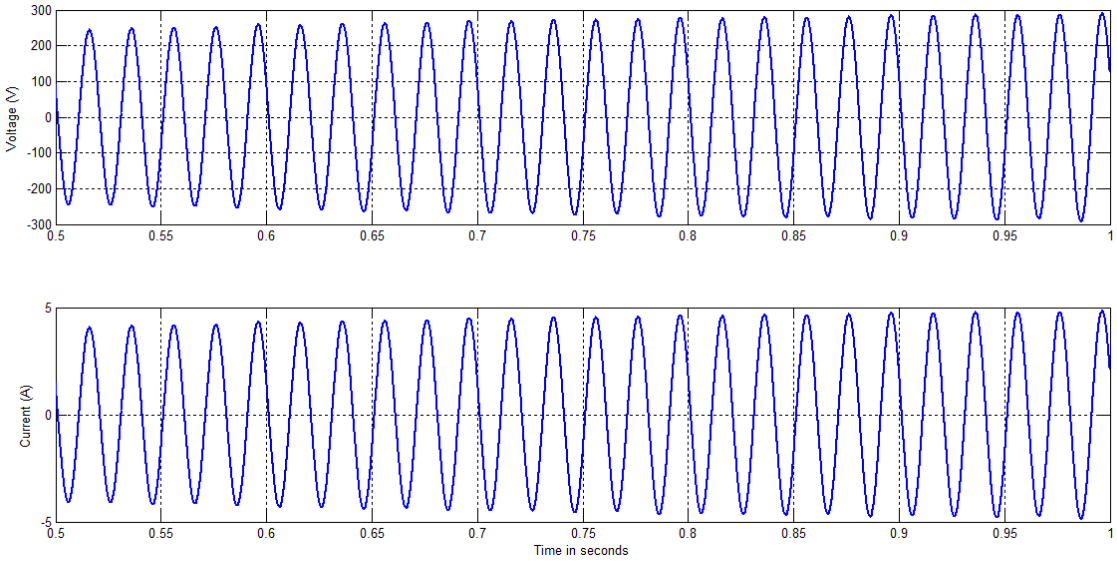

Fig-10: The three phase voltage output of grid connected PV inverter using proposed control scheme

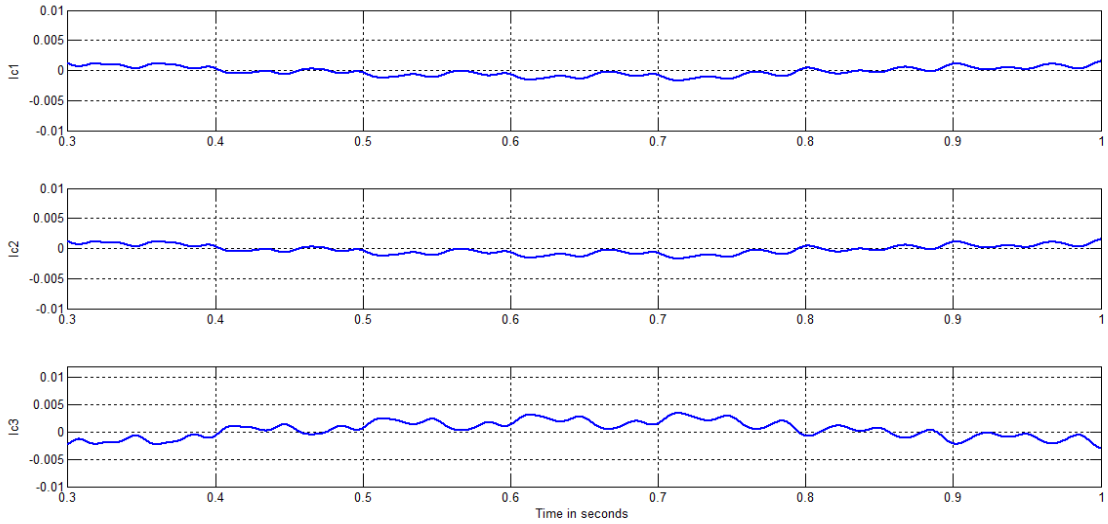

Fig-10: The suppressed DC currents

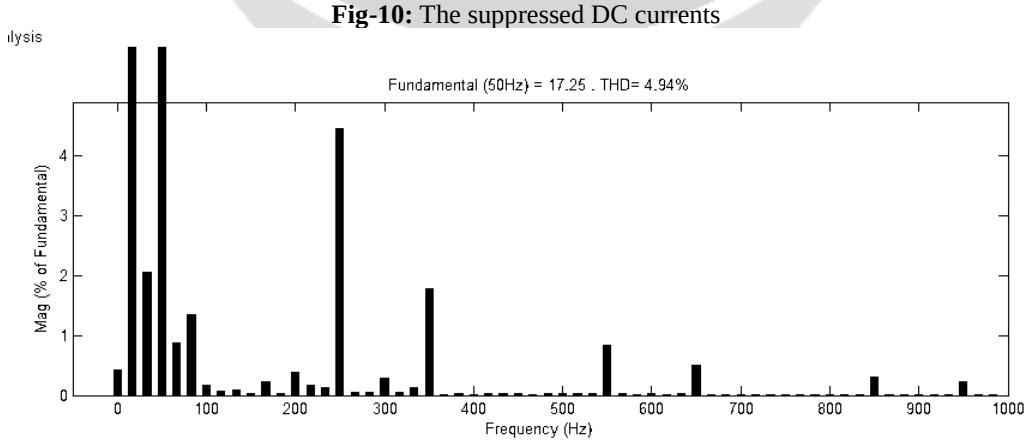

Fig-12: FFT analysis of the grid injected PV Three phase Inverter output voltage.

Fig-9 represents the proposed controller design which has extended for three phase system; fig-10 shows the waveform of three phase output voltage and currents, fig.11 shows the dc currents present in the AC output are suppressed to below 5% and fig-12 represents the FFT analysis of the proposed system which is about 4.94%.

5. CONCLUSIONS

In this project a novel control strategy to eliminate dc current injection to the grid for single-phase and three phase PV inverter without the isolation transformer has investigated. It is based on accurately sensing the dc offset voltage between the two bridge-leg middle points of full-bridge single phase and three phase inverter. The novel control strategy is inherently free from off-set measurement errors. The FFT had drawn using MATLAB Simulink software clearly depicting the effectiveness of the proposed system which is about 4.94%. The Results show that the novel control strategy can effectively suppress dc injection current of PV system under grid-connected condition effectively.

6. REFERENCES

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