# A Novel & Fast Design Structure of Carry Select Adder

Pankaj Sahu[1] Abhilash Sharma[2]
[1] M.Tech Scholar, Dept. of ECE, KNP College of Science & Technology, Bhopal, India
[2]Assistant Prof., Dept. of ECE, KNP College of Science & Technology, Bhopal, India

## ABSTRACT

*The design of high speed processing system is increasing because of development of many applications in signal processing. Less amount of consumption of power and delay of time are necessary demands in many applications High speed adder architecture works an important part in many applications. Development of new technology in the field of Embedded system and VLSI designing, there is an increasing demand of greater speed and less power consumption processor. The basic fundamental arithmetic operation is Addition. Adders are the important element in microprocessors and digital signal processing (DSP). Design of accurate and high performance adder is necessary in modern data processing system. Speed is imported necessity for designing of any circuit in digital system. In digital adders, limitation of speed in addition is determined by carry to transfer through the adder. Different approaches are there to better the performance of the adder. Carry select adder (CSA) is one of them. Adders are used not only addition operation also for subtraction, multiplication, and division. Several types of adder architecture designs have been research to increase the efficiency of the adder. In this paper, we design and implemented a new structure approach of CSA architecture. All architecture is verified with the help of 16, 32 and 64 bit adder circuits. Comparison is done with existing structure of adder and proves the efficiency of our proposed design. In this paper, we also design an architecture that performs high speed addition using modified excess-1 converter (BEC) in carry select adder. These designs are implemented on Xilinx device family.*

**Keywords:** - *Ripple Carry Adder (RCA), Carry Select Adder (CSA), Binary to Excess-1 converter (BEC).*

## I. INTRODUCTION

High speed and area-power efficient design of logic architecture are one of the most fundamental areas of research in this era of VLSI system design. Significant number of applications in VLSI, digital signal processing needs fast performing processors to secure processing of extremely large amount of data. Therefore essence of accurate and high performance adder plays an important function in advance data processing system. One of the important components is adders which are commonly found in microprocessors and many signal processing chips. It is used in many applications like multipliers, in DSP to carry out individual and separate operations. Addition speed in digital adder is limited by the requirement of time for a carry to promote through the adder. In conventional adder i.e. in ripple adder the sum for each bit position is created in sequentially only after the position of previous bit has been added then transfer the carry into the next position [1]. Carry select adder (CSA) is one among them to improve the delay of function independently producing multiple carries and then select a carry to produce the final output of a sum. However, CSA consumes more area since it uses many pairs of ripple adders to generate the partial sum and carry, then the selection of final sum and carry by the use of multiplexers [2]. Hence, the best effective use between speed and area in any of the design is a serious issue. Therefore basic method used in this paper to enhance the speed is to use modified excess-1 converter increase the performance of system [1].

## II. BINARY TO EXCESS-1 CONVERTER (BEC)

Excess-1 converter is used to solve the problem of consuming the area and power in Carry Select Adder [2]. Figure 1 shows the basic structure of 4-bit BEC. The common expressions of the 4-bit BEC is as

$$X0 = \sim B0 \quad (1)$$
$$X1 = B0 \wedge B1 \quad (2)$$
$$X2 = B2 \wedge (B0 \,\&\, B1) \quad (3)$$
$$X3 = B3 \wedge (B0 \,\&\, B1 \,\&\, B2) \quad (4)$$

| Binary[3:0] | Excess- 1[3:0] |
|---|---|
| 0000 | 0001 |
| 0001 | 0010 |
| 0010 | 0011 |
| ⋮ | ⋮ |
| 1111 | 0000 |

**Table 1:** Function Table of 4-bit Excess-1 converter (BEC)

The main target of Binary to excess-1 converter is used in place of the RCA (ripple carry adder) with Cin =1 in order to decrease size of the area and consume less power in the 16-B Carry Select Adder.

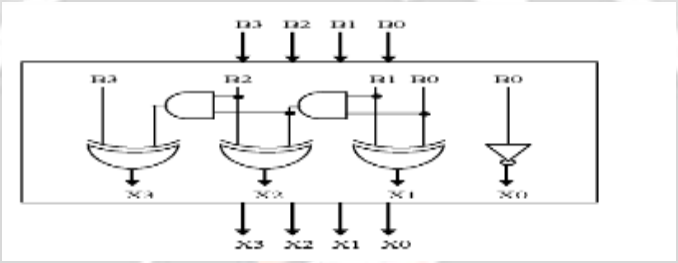


**Figure 1:** 4-bit Binary to Excess-1 converter (BEC)

## III. STRUCTURE OF CONVENTIONAL 16-BIT ADDER USING RCA

Figure 2 presents very basic structure of the 16-Bit Carry Select Adder using Ripple Carry Adder (RCA). The total structure size is separated into five groups with different bit size RCA.

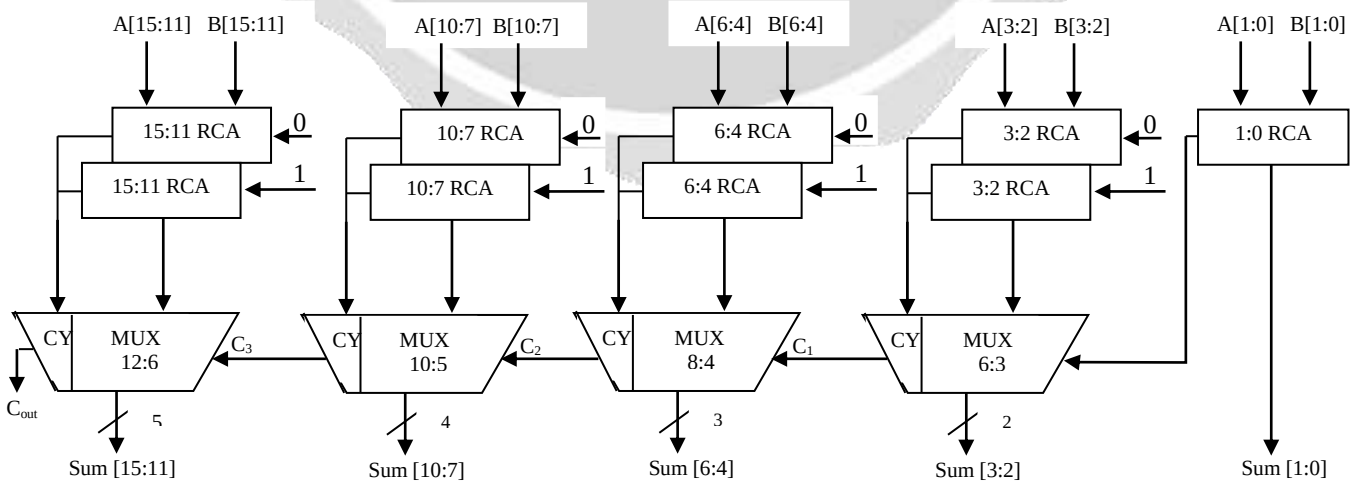


**Figure 2:** 16-Bit Carry Select Adder using Ripple Carry Adder

The simplest form of adder is RCA and their performance is restricted because carry is transferred to the next stages. In a 1st group consist of only one 2-bit size RCA which adds the bit value from input and the carry input then produce results to sum [1:0] and the carry out. The carry out of the Group 1 will acts as the selection input to multiplexer of group 2. If the carry-in is 0, the sum and carry-out of the upper RCA is selected to perform, and if the carry-in is 1, the sum and carry-out of the lower RCA is selected and perform the operation of addition [2]. In the same way the remaining groups will be worked depending on the Cout from the groups of previous blocks.

## IV. PROPOSED STRUCTURE OF 16-B CARRY SELECT ADDER USING MODIFIED BEC

The structure of the modified 16-Bit CSA using BEC is shown in Figure 3. In this architecture instead of the RCA with Ci = 1, BEC block is used. The structure is again divided into five groups with different bit size RCA and modified BEC block. In our proposed work we replaced all the RCA block from 2nd group with modified BEC.

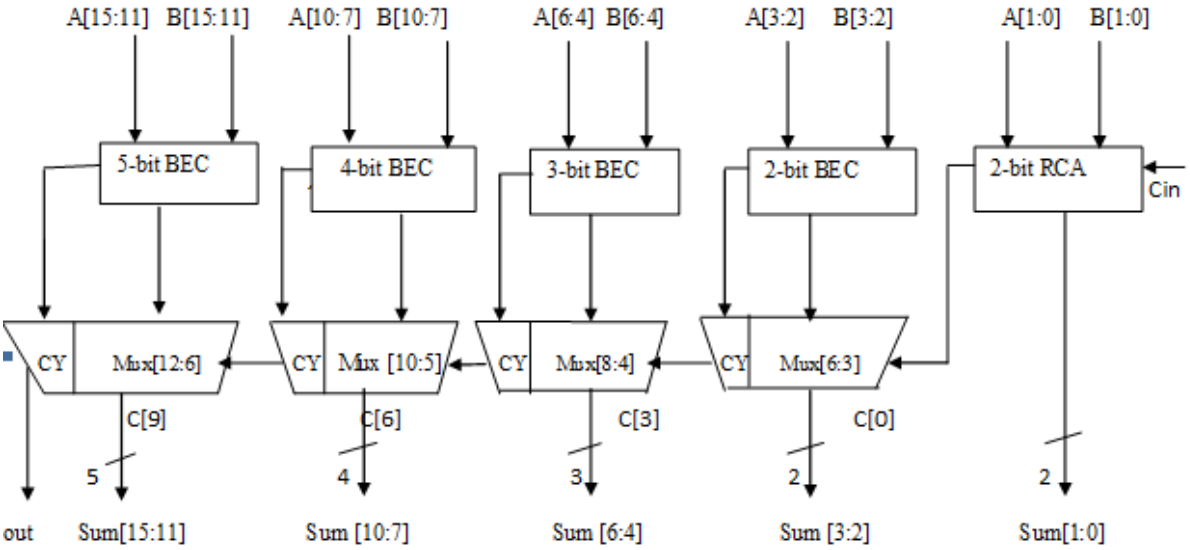


**Figure 3:** Proposed 16-Bit Carry Select Adder using Modified BEC

The Binary to excess-1 Converter is used instead of the ripple carry adder with Cin=1, to decrease the area and power consumption of the regular Adder. In this structure also group 1 consist of one 2- bit RCA and output of this RCA goes to the next group. The first group adds 2 bit binary digit as input value in terms of A and B with the help of RCA block. RCA block is nothing but the full adder which adds three inputs value and produces output value. In the next group it contains again 2 bit binary input value but with the help of excess to 1 converter and produces output value as sum and carry output and carry is transferred into the next position. The third group will adds 3 binary input values and produces sum and carry output and fourth group will adds 4 binary input values. The last group will add 5 binary input values and it produces sum and carry output. Then finally all the 16 bit is added with the help of all different blocks in the design architecture and provides final sum output and carry output.

## V. SIMULATION RESULTS

In an overall designing and scientific experiment regarding algorithm that we have mentioned in this paper is being performed on Xilinx 14.3i Spartan 6, Virtex 6, Virtex 7 family version. Xilinx 14.3i has noticeable features like a low memory requirement, faster solving of problem and low cost.

Xilinx 14.3i has noticeable features like a low memory requirement, faster solving of problem and low cost. It contains modified tools like smart Compile techniques with better design of their computing hardware supply for faster closure of time and produce higher quality of results for a better time to designing solution. Figure 4 and Figure 5 represents the simulation result of Regular 16-Bit CSA with RCA, proposed 16-Bit adder with Modified BEC respectively. In order to perform comparison, various adders regular 16-bit CSA using RCA, proposed 16-bit CSA with modified BEC on Xilinx software done.

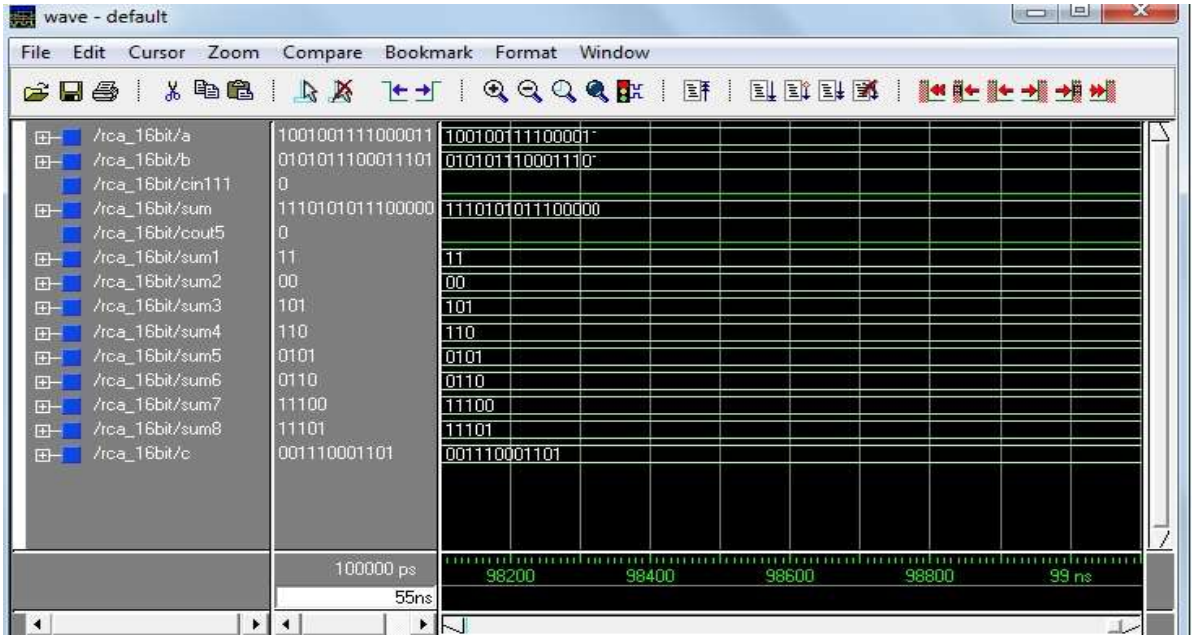


**Figure 4:** Simulation of Regular 16-Bit CSA

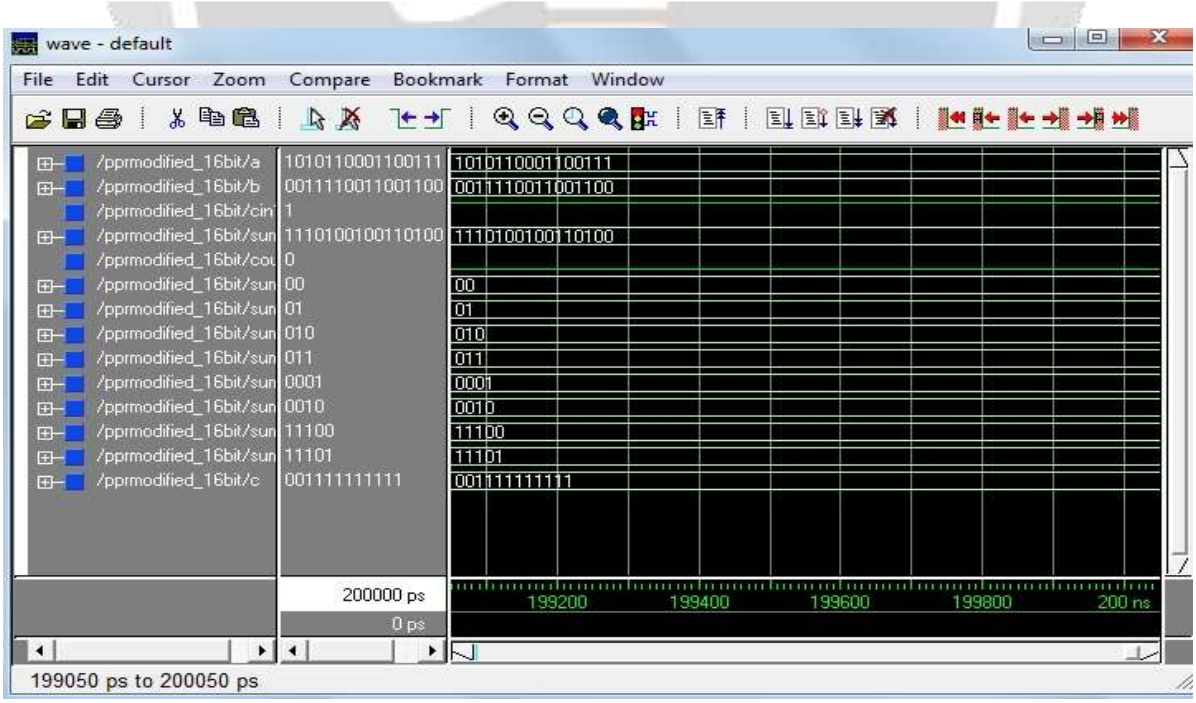


**Figure 5:** Simulation of proposed 16-Bit CSA

Comparison of adders in Spartan 6, Virtex 6, Virtex 7 device family has been done and equipped that the result of our proposed CSA is much better than regular Adder. This comparison is shown in Table 2. The comparison graph of regular carry select adder and proposed carry select adder in terms of delays for word size 16, 32 and 64 is shown in figure 6, 7, 8 respectively. All the experiment and coding designs have been written in VHDL and all the function is analyzed by RTL and gate level simulation.

| **Word size** | **Adder** | **Delay(ns) Spartan 6** | **Delay(ns) Vertex 6** | **Delay(ns) Vertex 7** |
|---|---|---|---|---|
| **16-B CSA** | Regular (Dual RCA) | 15.401 | 5.610 | 4.478 |
| | Proposed (Modified BEC) | 13.127 | 4.073 | 3.257 |
| **32-B CSA** | Regular (Dual RCA) | 24.132 | 9.387 | 7.474 |
| | Proposed (Modified BEC) | 21.438 | 7.887 | 6.320 |
| **64-B CSA** | Regular (Dual RCA) | 42.666 | 17.820 | 14.205 |
| | Proposed (Modified BEC) | 37.850 | 15.343 | 12.275 |

**Table 2:** Comparison Table of Adders for Different Device Family

Figure 6 represent the graphical representation of delay for different adders in Spartan 6, Virtex 6 and Virtex 7 device families. This graph is for 16 bit size.

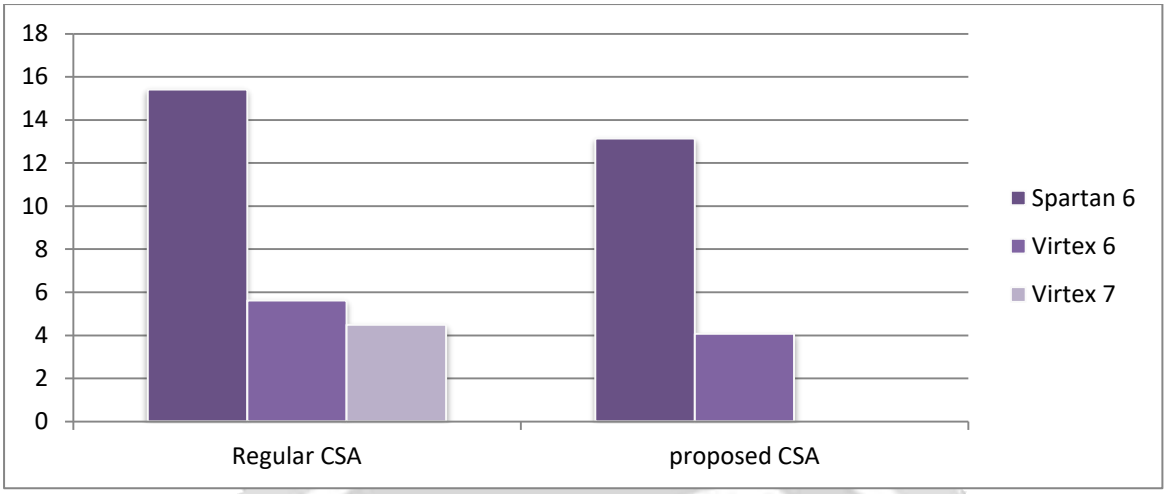


**Figure 6:** comparison of Adder for Delay (Word Size =16 bit)

Figure 7 represent the graphical representation of delay for different adders in Spartan 6, Virtex 6 and Virtex 7 device families. This graph is for 32 bit size.

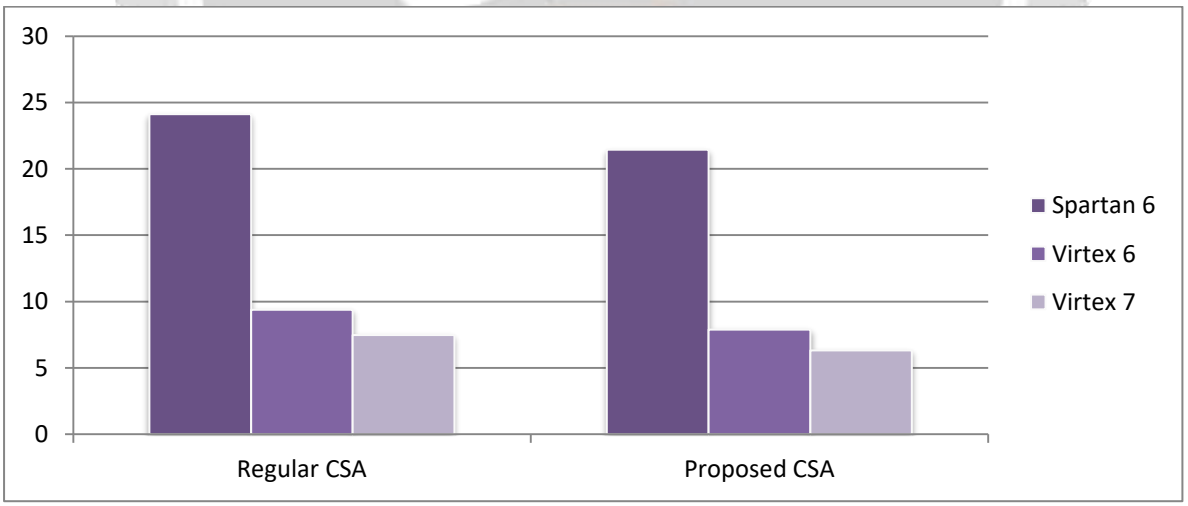


**Figure 7:** comparison of Adder for Delay (Word Size =32 bit)

Figure 8 represent the graphical representation of delay for different adders in Spartan 6, Virtex 6 and Virtex 7 device families. All the adders this graph is shown for 64 bit size.

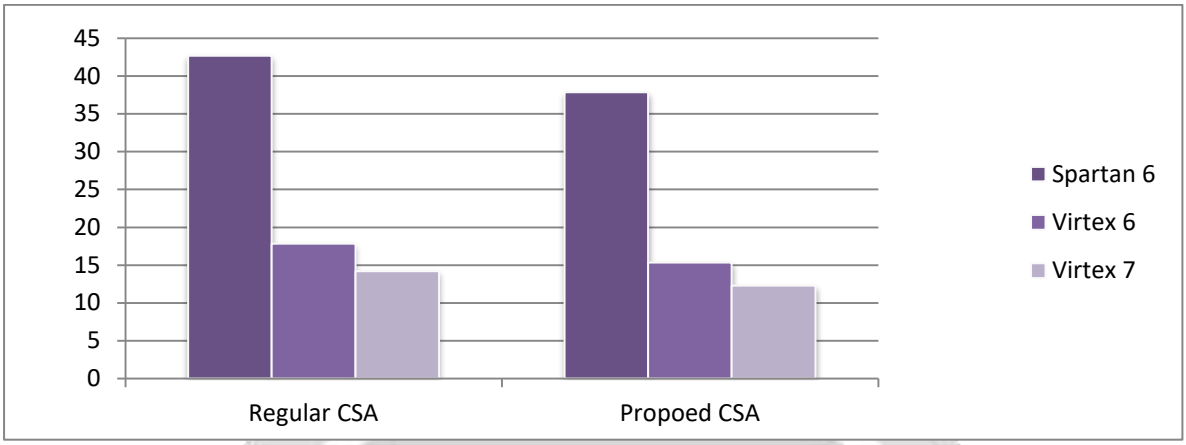


**Figure 8**: comparison of Adder for Delay (Word Size =64 bit)

## VI. CONCLUSION

Modified Carry Select Adder is a simple technique used in this paper to decrease the delay of Carry Select Adder. The decrement of delay of a design allows for 16-bit, 32-bit and 64-bit sizes proves the achievement of the proposed design. The regular CSA has main disadvantage of consumption of wide area and delay. The proposed Carry Select Adder with modified BEC is used to decreases the size of area and delay, when compare to conventional Carry Select Adder. Different technique which is discussed in this paper reduces area and delay. It would be really interesting to test the design for 128-bit.

## VII. REFERENCE

[1] G. Karthik Reddy, D. Sharat Babu Rao "A Comparative study on Low-Power and High Speed Carry Select Adder" IEEE Sponsored 9th International Conference on Intelligent Systems and Control (ISCO) 2015

[2] B. Ramkumar and Harish M Kittur, "Low-Power and Area-Efficient Carry Select Adder", IEEE Transsactions on Very Large Scale Integration (VLSI) Systems, VOL. 20, No. 2 Feb 2012.

[3] Ms. S.Manju, Mr. V. Sornagopal "An Efficient SQRT Architecture of Carry Select Adder Design by Common Boolean Logic", 2015 IEEE.

[4] Sajesh Kumar U., Mohamed Salih K. K. Sajith K.,"Design and Implementation of Carry Select Adder without Using Multiplexers", 2012 1st International Conference on Emerging Technology Trends in Electronics, Communication and Networking 2015 IEEE.

[5] Samiappa Sakthikumaran, S. Salivahanan, V. S. Kanchana Bhaaskaran, V. Kavinilavu, B. Brindha and C. Vinoth, "A Very Fast and Low Power Carry Select Adder Circuit",2011 IEEE.

[6] B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J Sci. Res., vol. 42, no. 1, pp. S3-S8, 2010.