A novel approach of Vedic multiplier using modified CSA with optimized system performance

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ABSTRACT

Vedic mathematics is a Design of mathematics followed in ancient Indian and it is applied in various trees of mathematical calculations. a novel algorithm is designed on Vedic mathematics using bit reduction technique for binary multiplication. There is a total count of 16 vedic sutras or formulas and 13 sub-sutras to ou source the different mathematical operation. For carrying out the multiplication operation there are two sutras- urdhva tiryakbhyam and nikhilam sutra. In this two, the urdhva tiryakbhyam sutra is discussed in this paper to design a multiplier and compared the area and speed with array multiplier. Vedic multiplier is structured using modified square-root carry select adder (MSQRT-CSA). They considered the bring out with numerous adders like CSA, Carry look-ahead adder (CLA), Square root CSA (SQRT-CSA). Collated with other methods, multiplier is faster in MSQRT-CSA. Vedic multiplier is proposed and contrasted with array multiplier in Complex number multiplication is used. The remainder is derived from this sutra by lowering the remainder bit size to N-2 bit. At this moment, the no.of bits of the remainder is statically maintained as N-2 bits. The phase of the proposed algorithm is enhanced with equipoising the power and area. Even though there is a deviation in lower order bits, this method shows maximum difference in higher bit lengths. The paper is organized as follows. In section 2, exhibits the 2x2 and 4x4 Vedic multiplier architectures of proposed architecture. Section 3 explains about the complex number multiplication using Vedic multiplier. The results, comparisons are contained in section 7, while section 8 will holds the conclusion

Keyword : - *Vedic multiplier, Carry lookahead adder, Urdhva Tiryabhyam,*

1. Introduction

In an Ancient India it's One of the technique used for solving arithmetical problems is Vedic Mathematics in easier way. It contains 16 formulas and 13 sub-formulas. These sutras are used in solving complex computa- tions, and executing them manually. It is working on 16 sutras and 13 up-sutras. The principles and algorithms of all sutras were given in. Urdhva Tiryakbhyam Sutra is essentially used for multiplication which means "Vertical and Crosswise". The multiplier depend this sutra is known as Vedic multiplier. It is based on a novel content of array multiplication. In the model and implementation of Triyakbhyam were done and the squaring and cubing helps to compare speed with Nikhilam sutra algorithm.

In the Vedic mathematics algorithm for multiplication was discussed the implementation of Arithmetic unit was used. The arithmetic unit was structured to perform multiplication, addition and subtraction and multiply accumulation operations. A fast multiplier built with Vedic Mathematics algorithm in the MAC unit. The cube, square algorithms along with Karatsuba algorithm have been discussed , to reduce the multiplications required. In, a ROM based multiplier is suggested. From two Inputs, one is fixed here. So this method is being used in matrix

applications and multiplication which use static coefficient multiplication. The faster Vedic multiplier ingests more power than convention ones. In the multiplier based upon Nikhilam sutra was presented with filteration in 2's multiplication block and complement block. 7-bit encoding technique is employed in structure of multiple radix multipliers. The high speed 32 × 32 bit Vedic multiplier was showed . The binary implementation by carry save adder was presented in and consideration result was made.

The iterative Nikhilam sutra algorithm was presented. It deducts two larger numbers in to two smaller numbers by neglecting zeros from the least significant side and performing bit shifting to complete the multiplication operation. In this method demands for closeness of the multiplicands to the power of 10. This algorithm is matched as array multiplier final product can be derived on array of address. The Urdhava Triyagbhyam Vedic is constructed for actual development of multiplication and it is presented. Here the partial products are produced at the same time. In 128 × 128 bit Vedic multiplier is introduced.

In the Urdhava Vedic multiplier is considered with Booth multiplier to analyze their delay and speed. From the results, it is resulted that Urdhava multiplier is superior in power and delay. The speed is extracted to the extent of 32% considered with Booth multiplier. The design of standard cell approach is on Urdhava multiplier. The lower order bits multiplier is helps to construct the higher order bit. In Vedic multiplication is 8085/8086 microprocessors is implemented. A Nikhilam Sutra algorithm multiplication is based on design. In high speed and low power Vedic multiplier depends on Tridhava approach is constructed using BEC (Binary-to Excess-one code converter) based carry select adder. Here, instead of two RCA (Ripple Carry Ad- der), one BEC and one RCA are used. Depends on the carry generation, either BEC or RCA outputs are selected. If Cin = "0", RCA is selected. If Cin = "1", BEC is selected. Using this, power optimal high speed multiplier is designed. In the Vedic multiplier is constructed using modified Carry Select adder. By this, area is reduced by 40%.

2. VEDIC MULTIPLIER

2.1 2X2 bit Vedic Multiplier

Consideration of two 2-bit nos, X and Y where A=a1a0 and B=b1b0. Initially, the least significant bits (LSB) a0 and b0 is multiplied which results the LSB (s0) of the final result. Then, the LSB is multiplied with the next higher bit of the multiplicand b1 by multiplicand a0. The result produces second bit s1 of the final result and carry c1 which was produced gets added with the partial product resulted by multiplying the most significant bits a1 and b1 to give the summation of s2 and carry c2. The sum s2 is the 3rd bit and carry c2 becomes the 4th bit of the final result.

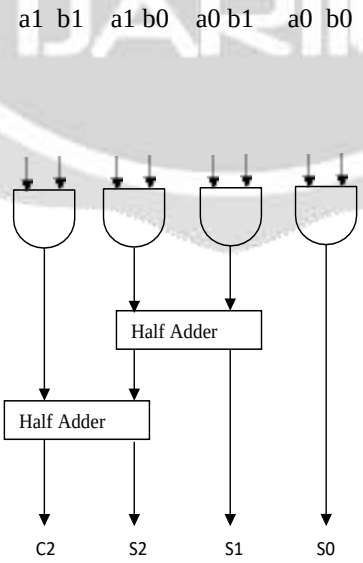

Fig -1: Block diagram of 2x2 Multiplier

$s0 = a0b0$

$c1s1 = a1b0 + a0b1$

$$c2s2 = c1 + a1b1$$

The final result will be c2s2s1s0.

2.2 4x4 Vedic multiplier

The proposed system's diagram of 4X4 vedic multiplier is shown in figure 2.2. To get the final result, Three 4-bit ripple carry adders are required for using 4 two-bit Vedic multipliers. In this proposed system, the 4-bit RC adder is used to sum the two 4-bit operands gained from cross multiplication of the middle 2X2 bit multiplier modules. The two 4-bit operands is added using second 6-bit RC adder i.e., sequenced 4-bit ("00" & most significant two output bits of right hand most of 2X2 multiplier module) and one 4-bit operand we get as the output sum of hand most of 2X2 multiplier module. The 16X16 bit multiplier is structured using four 8-bit multipliers and 8X8 bit multiplier is structured using four 4-bit multipliers and so on.

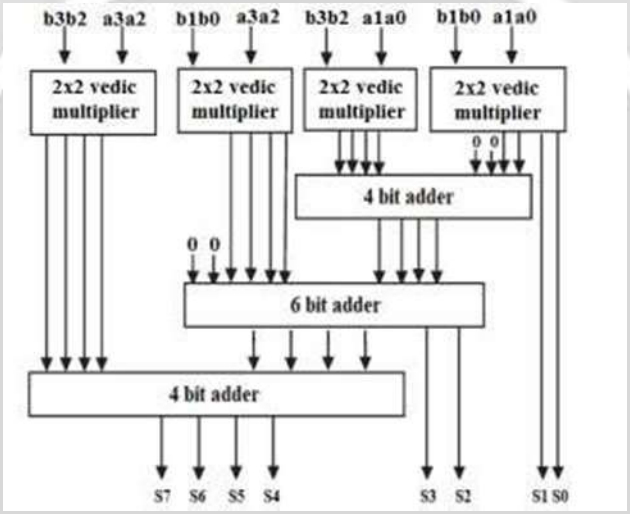

Fig -2: Block diagram for 4x4 Multiplier

Algorithm of two Binary numbers for 4X4 bit vedic multiplier Using Urdhva Tiryabhyam
CP=Cross Product (Vertically and Crosswise)

X3 X2 X1 X0 Multiplicand

Y3 Y2 Y1 Y0 Multiplier

P7 P6 P5 P4 P3 P2 P1 P0 Product

3. COMPLEX NUMBER MULTIPLICATION USING VEDIC MULTIPLICATION

(Font-10, Consider two complex numbers

$$a = ar + j\ ai;$$
$$b = br + j\ bi;$$

The product of a and b is given by

$$pr + j\ pi = ab = (ar + jai\ ) * (br + j\ bi\ );$$

$$pr = (arbr - aibi)$$
$$pi = (arbi + aibr)$$

Where pr and pi represents the real part and imaginary part of the final product p, respectively. The above equations can be alternatively writer as follows

$$pr = arbr - aibi = ar(br + bi) - (ar + ai)bi$$
$$pi = arbi + aibr = ar(br + bi) + (ai - ar)br$$

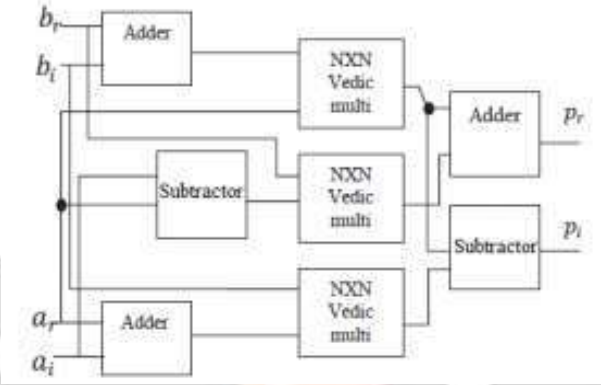

Fig-3: Three real Vedic Multipliers solution architecture for multiplication of two complex numbers

This reduces the number of multiplications from 4 to 3 nxn vedic multiplier as shown in figure 3

4. Algorithm I

Input: A, B Output: P

Step 1: The multiplicands A and B are with N-bits. Their remainders are calculated by taking 2's complement for the remaining N-2 bits and removing first 2-bits. (N-1, N-2 = 11)

$$A = 2^N - r \text{ and } B = 2^N - r$$

r1 = complement (A), r2 = complement (B)

Step 2: Multiplying both remainders using N-2 × N-2 bit multiplier $P_1 = r_1 \times r_2$.

Step 3: Shifting A by N times (P2)

Step 4: Shifting the remainder r2 by N times (P3)

Step 5: The product can be calculated as,

$$P = AB = P_2 + P_1 - P_3$$
$$= (2^N \times A) + (r \times r) - (2^N \times r)$$
$$= A << N + (r_1 \times r_2) - (r_2 << N)$$

The proposed architecture for the multiplier for the MSB values 11 is given in **Figure 4**

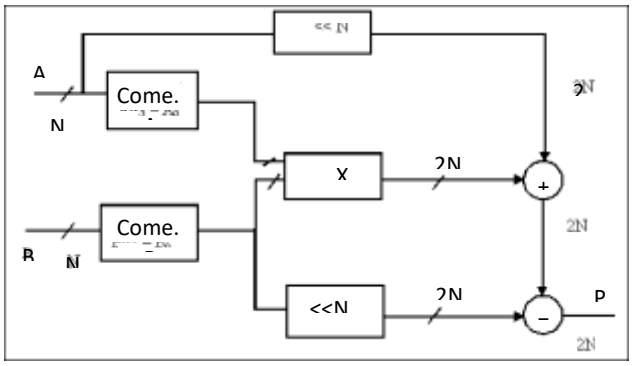

Fig-4 : Architecture for Algorithm I

5. Algorithm II

Input: A, B

Output: P

Step 1: the remainders are determined by taking the numbers without the MSB values. By Calculating remainders for both multiplicands by removing first 2- bits. If the removed bits are 10, (i.e. N-1, N-2 = 10)

$A = 2^{N-1} + r_1$ $r_1 = A$ (without first two bits)
$B = 2^{N-1} + r_2$ $r_2 = B$ *(without first two bits)*

Step 2: Multiplying both remainders using N-2 × N-2 bit multiplier (P_1).
Step 3: Shifting A by N-1 times (P_2)
Step 4: Shifting the remainder by N-1 times (P_3)

Step 5: The product can be calculated as,

$$P = AB = P_2 + P_1 + P_3$$
$$= 2^{N-1} \times A + (r \times r) + (2^{N-1} \times r)$$
$$= A << N-1 + (r_1 \times r_2) + (r_2 << N-1)$$

The architecture for the proposed algorithm is shown in Figure **5**

6. Algorithm III

Input: A, B N bits

Output: P 2N bits

Step 1:Tthe remainders are determined by taking the numbers without the MSB values by Calculating remainders for both multiplicands by removing first two bits. If the removed bits are 01,

$A = 2^{N-1} - r_1$ r_1 = complement (A)

$B = 2^{N-1} - r2$ r_2 = complement (B)

Step 2: Multiplying both remainders using N-2 × N-2 bit multiplier (P_1).
Step 3: Shifting A by N-1 times left side (P_2)
Step 4: Shifting r2 by N-1 times left side (P_3)
Step 5: The product can be calculated as,

$$P = AB = P_2 + P_1 - P_3$$

$= 2^{N-1} \times A + (r \times r) - (2^{N-1} \times r)$

$= A << N-1 + (r_1 \acute{} r_2) - (r_2 << N-1)$

The architecture for the proposed algorithm is shown in Figure 6.

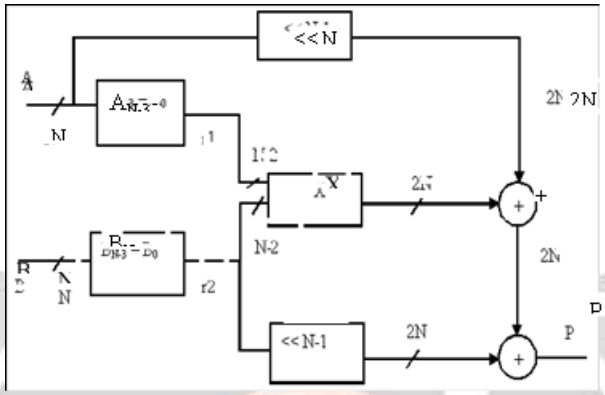

Fig-5 : Architecture for Algorithm II

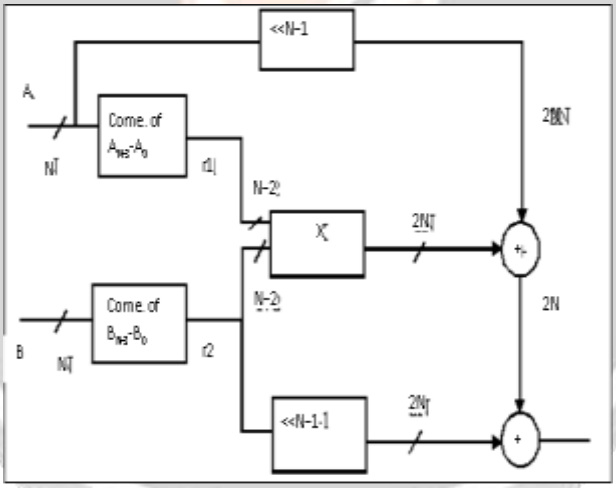

Fig-6: Architecture for Algorithm III

7. Results

A procedure to tackle the number juggling activities effectively and intellectually is Vedic Mathematics. Generally, Urdhva Tiryakbhyam Sutra is known as Vedic Multiplier since it covers all scope of information sources. It signifies "in an upward direction and transversely". In a large portion of the examination papers [2]-[9] recorded in references focused on this sort of multiplier. The equipment execution for twofold numbers is likewise finished. This includes RCA and lower request Vedic multipliers. The equal execution has additionally been done [9] [10]. The Nikhilam Sutra is intended for unique case. It re-fers "all from 9". The strategy is effective when the multiplicands are nearer to the various of 10. There is no ef-ficient equipment execution for Nikhilam Sutra for paired numbers. The calculation is obvious when the two numbers are of with positive or adverse leftover portion. At the point when one number is with positive leftover portion and the other is with adverse remaining portion, the computation is unique.

Contingent upon the worth upon Right part, adjustment is made on left part. In the proposed strategy, all scope of data sources can be given. Karatsuba calculation is effective for higher request multipliers. Karartsuba multiplier utilizes three multipliers dependent on Equation. (3). Be that as it may, in the proposed strategy, the quantities of multiplier is diminished to one and number of pieces of the multiplier is decreased to N-2. Here, Nikhilam sutra and Karatsuba calculation are joined to get the rapid. The execution for different Vedic multipliers is finished utilizing Xilinx Spartan 3e pack. In the fundamental module, the proposed multiplier is itself utilized. The examination with Vedic multiplier for de-lay is recorded. The examination with ordinary techniques .

The proposed calculations are written in VHDL and reenacted utilizing ModelSim . The reproduction result for 32 digit size. We executed the calculations of existing and proposed work in Xilinx SPARTAN 3E FPGA. Moreover, execution bring about Xilinx SPARTAN 6 for the proposed method.While contrasting and SPARTAN 3e, SPARTAN6 conveys high velocity however devours more force. While contrasting postponement and different strategies, the mix of Nikhilam sutra and Karatsuba calculation gives least deferral. the defer contrast between different strategies for higher pieces is high.

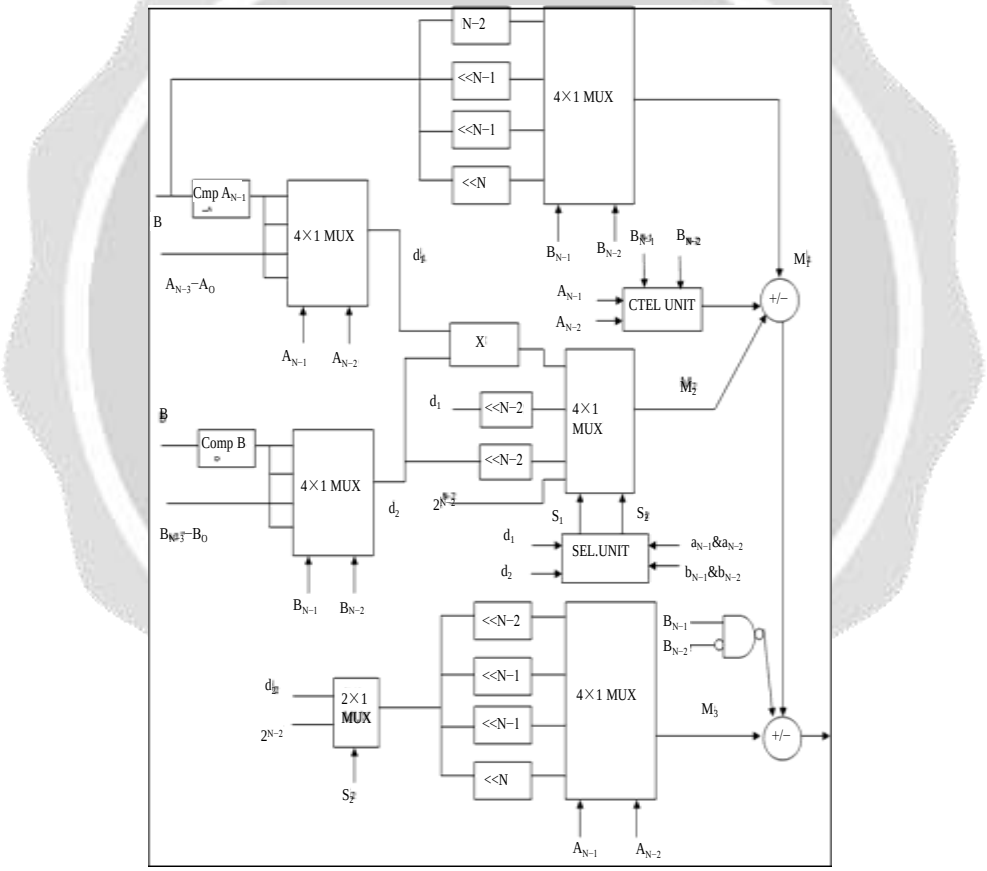

Fig-7 : Combined architecture for multiplier

8. Conclusion and Future Work

In this examination paper, progressive estimation of Vedic multiplier is proposed for fast applications. The

calculation of Karatsuba is changed to lessen the quantity of multipliers needed in the estimation. Rather than parting the twofold number into a large portion of, the number is parted dependent on remaining portion esteem. The rest of calcu-lated utilizing Nikhilam Sutra with the end goal that the quantity of pieces is decreased to N-2. By joining Nikhilam Sutra and Karatsuba calculation, the quantity of pieces to the multiplier is decreased. Four modules were made dependent on re-mainders. From the outcomes', unmistakably the proposed strategy produces yield quicker than different strategies. This half breed multiplier is most appropriate for increasing enormous numbers in fast applications.

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