Advanced Low-Power High-Speed SAFF Implementation with MTCMOS in 45nm

Adarsh Bhardwaj ABES Engineering College

Amar Jyothi ABES Engineering College

Ankit Kumar Bharti ABES Engineering College

Amit Pal ABES Engineering College

Shailendra Bisariya ABES Engineering College

Abstract— ***A sense amplifier based flip-flop has a low power consumption and high speed. It has a new sense amplifier stage and a new one-ended latch stage. It significantly reduces the power consumption and delays. The proposed SAFF has low voltage operation thanks to MTCMOS optimization. Compared to MSFF, SAFF has lower delay and lower power consumption. Our SAFF is designed for low voltages. We adopt MTCMOS optimization techniques. MTCMOS enables efficient power management by powering down inactive circuits or adjusting voltage levels according to the desired performance. The design is based on 45nm technology and is implemented in cadence virtuoso.***

Keywords:- Sense amplifier flip flop (SAFF) , Flip Flop (ff), power consumption, speed.

I Introduction

Very Large-Scale Integration (VLSI) is one of the fastest-growing market trends.The focus of digital circuits is on high speed and low power [1]. A low-power circuit uses less power. This is particularly important for battery powered devices such as smartphones, wearable devices and IoT devices. By reducing power consumption, you can increase battery life, enhance user experience and reduce frequent charging.A high-voltage circuit generates more heat than a low voltage circuit. This can lead to thermal issues such as overheating and low reliability. On the other hand, a low voltage circuit generates less heat, reducing thermal issues and improving the reliability and life of the integrated circuits.Power consumption directly affects the operating cost of electronic devices, especially for large scale deployments such as data centers or sensor networks. Lower power consumption means lower operational costs, which in turn lowers the cost of deployment and maintenance for digital systems.Flip flops are fundamental storage devices. Their delay and power have a direct effect on the performance and power of the digital system.[2]. The flip flop is composed of two latches (master and slave) cascading one on top of the other to create the flip flop. The “pulse-triggered flip-flop” (PFF).[3-6]. The PFF has only one latch and is powered by the clock pulse generator. The PFF takes data immediately after edge of rising clock signal and setup time is very close to zero or negative. One of the main issues with PFF is the correct width of the clock pulse. Too small a width affects the accuracy of the data captured while too wide a width increases the holding time. The longer the pulse width is, the longer the PFF holding time will be. This is known as the sizing problem. This limits the widespread use of the PFF. The SAFF has a setup time close to zero or even negative.[2]. The SAFF is composed of an SA stage and a slave latch. This allows data capture as soon as the rising edge of the clock reaches Clk. The output of the SA stage is retained during the positive half-cycle of the clock, which eliminates the sizing problem in PFF.The SAFF has a near-zero or negative setup time and a limited hold time. This makes it a good alternative to MSFF in standard cell libraries for high -speed design.There are many attractive features of the SAFF. However, it has some drawbacks. Firstly, the SAFF increases power consumption during pre-charging. As a result, the latch structure needs to be fast in order to reduce the time from CK to Q. Secondly, the SAFF must address the low

voltage operation limitations in conventional SAFF designs.

II Working of Sense Amplifier Based Flip Flop

In the first stage, the sense amplifier finds the true and complimentarily differential inputs. In the sense amplifier stage, continuous transitions from the high to the low logic levels are generated on one of the outputs. These transitions are triggered by a leading clock edge, and are captured by the s-R latch and remain in this state until the next leading clock edge is triggered. Thus, the whole structure is flip-flops[7].

The function of the S-R flip flop is as follows: The set input is S. The reset input is R. Both S and R are not allowed to be at a low level at the same time. This condition is ensured by the sense amplifier stage. When S is at a low level, the output of Q is set to high. Q is set to high and Q is at a low. When R is at a low, Q is set to higher and R is set to low. Both Q and R are always delayed relative to each other. The rising edge happens first after one gate delay. The falling edge happens after 2 gate delays. This timing constraint restricts the performance of the SAFF.

The SAFF is based on a sense amplifier that detects and amplifies the small voltage differences of differential inputs. This amplified signal drives the S-R Flip Flop. The S-R Flip Flop captures the state and holds it until the following clock edge. A sense amplifier based flip flop improves on the traditional flip flop design. This design improves the noise immunity and the reliability of the flip flop. The inherent gate delays limit the performance of a flip flop with a sense amplifier. The SAFF is best suited for high speed and low power applications where the state transitions need to be precise and reliable [8].

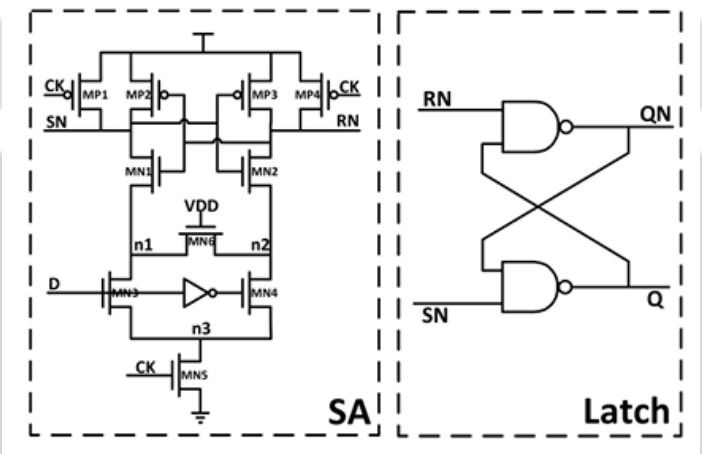

Fig 1: Schematic of ConventionalSAFF

SAFFs, on the other hand, have several benefits over flip-flops without amplifiers. First, SAFFs increase speed and reliability by increasing the voltage difference of small differential inputs. This increases the clarity and sharpness of the transitions. Second, it reduces the susceptibility of the circuit to noise and signal decay. Third, it improves the circuit's robustness. Fourth, it consumes less power. SAFFs handle small input signals efficiently, making them suitable for low power applications [9]. SAFFs have a sense amplifier stage that produces monotonic transitions. This ensures more consistent and predictable performances, which is important in high-speed, high-performance digital circuits. These advantages make SAFFs especially useful in modern, high performance computing and communication systems.

III Proposed SAFF Working

The SA stage increases the SAFF hold time due to the sense amplifier structure. The SA stage is able to capture input data more quickly at the rising edge (CK) of the clock because the internal nodes remain low during operation, which reduces the discharge time. As a result, the SAFF holds time decreases. The SAFF setup time increases slightly due to the faster data capture. However, this increase is minimal as the internal nodes discharge time is very short. SAFF introduces a new single-ended latch. The SAFF combines the benefits of Strollo's latch (see Fig. 3) and Lin's latch (Fig. 2) for faster and more efficient operations.

The latch in stage 1 is very similar to Strollo latch in Figure 3 to ensure smooth operation. Lin's latch, as shown in Figure 2, eliminates glitches, mainly due to inclusion of MN9, when D is high, and DN is low MN9 completely stops the pulldown path to eliminate the glitch. The data storage feedback inverter has been changed to overcome current contention, if Q goes from low to high MN11 gets cut off by feedback inverter, and if Q goes from high to low MN7 gets cut off completely eliminating feedback inverter during the output transition. Because the latch works independently of the Rn, we can reduce the size of the Rn generation transistor in SA stage to reduce power consumption. The flip-flop can provide an extra QN output if required, with the Q / QN delay difference equal to the MSFF inverse inverter delay. Low voltage function failures are caused by the always-on transistor. The detection logic solves the low voltage function failures but the complexity of the detection logic leads to higher delay and higher power consumption. In the present paper, we propose to solve the problem of low voltage

function failures by optimizing MTCMOS. The driving capability of always on transistors should be lower than that of pull down transistors.

The input data D passes through MN8, MN9, and MN11 before reaching the rising edge (CK). The complement DN passes through MN7, MN10, and MN11 after passing through MN8, Q passes through MN9, MN11, and Q passes through MN2, MN6, and MN4. The input data D and DN pass through MN1, MN2, MN3, MN4, and MN5 respectively until QN passes through MN6, MN7, MN8, and MN9 (Q passes through MN1, Q.

During the low-to-high transition, prior to the rising edge of the clock (CK), input data D transitions from low to high, while its complement DN transitions from high to low during the negative half cycle. At the rise edge, SN and RN transition from low to high. In the positive half cycle, SN transitions from low to pre-charge through MN1, MN5, and MN3. Consequently, output Q transitions from pre-charge through MN5. When D is low, MN10 deactivates MN11, ensuring contention-free operation when MN5 deactivates. Throughout Q's positive half cycle, it is maintained by MN5. During Q's negative cycle of the CK, it pre-charges through MN5, which is turned off during this time while MN6 and MN7 maintain Q.

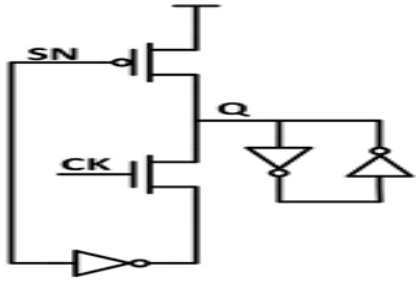

Fig2: Lin's Flip Flop

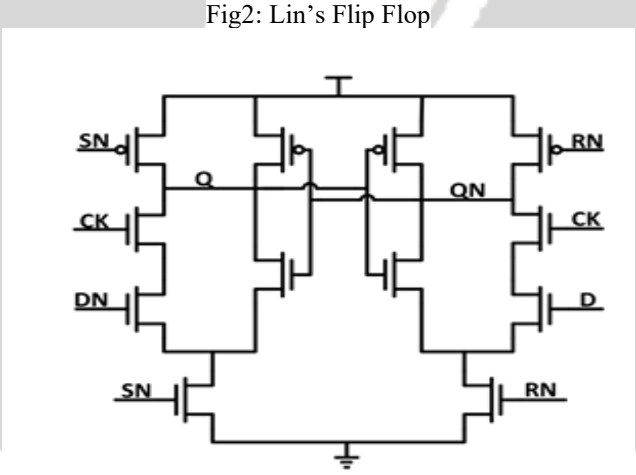

Fig 3: Strollo's Flip Flop

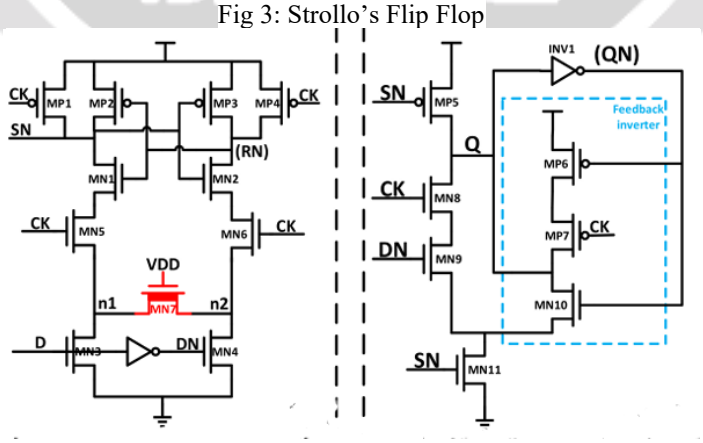

Fig 4: Schematic of Proposed SAFF

IV Design Procedure

We created the circuit using Cadence virtuoso. We are using MTCMOS. One of its main benefits is that MTCMOS significantly reduces static power dissipation in the circuit. In the standby mode of the circuit, the high-threshold transistor is used to minimize the leakage current. In the active operation, the low-threshold transistor is used.

This increases the switching speeds and improves the performance of the circuit.
MTCMOS offers high performance in a dual stage circuit design. It can be used in a variety of applications from battery powered to portable devices. It also improves overall power efficiency and increases battery life without sacrificing the device speed or performance. This is in line with the growing demand for energy-efficient electronic components in modern technology.
The Figure 5 shows the detailed schematic of SAFF proposed by us in Cadence Virtuoso

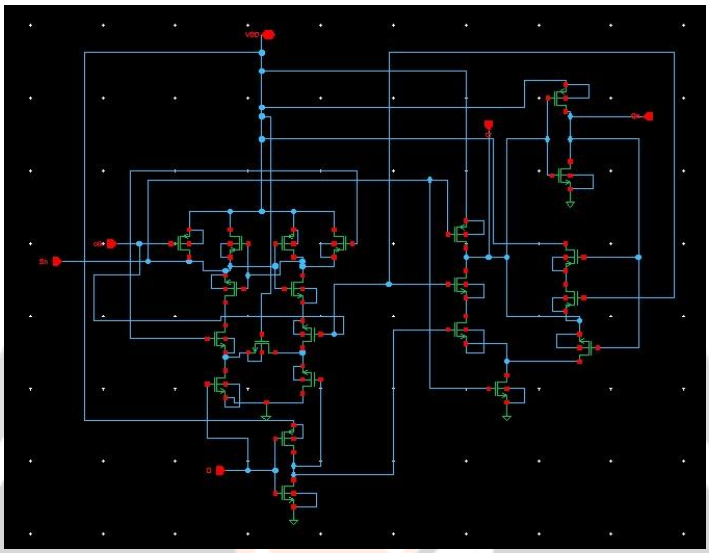

Fig 5:Schematic of Proposed SAFF in Cadence Virtuoso

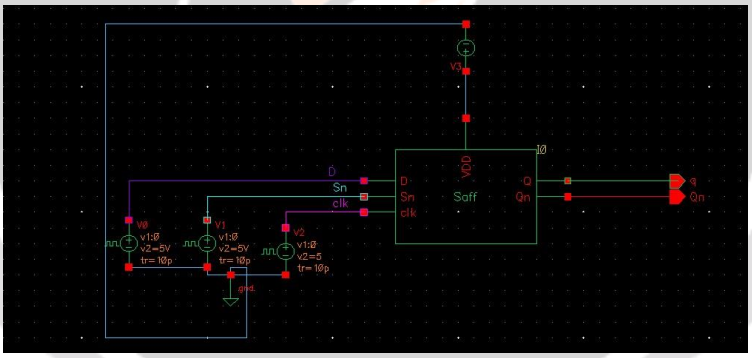

Fig 6:Symbol for SAFF

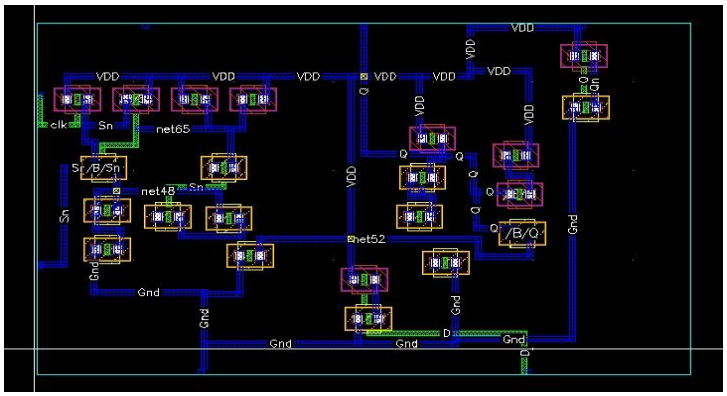

Fig7:Layout of SAFF

V Results

Waveforms as seen for the SAFF Layout are given in Figure 7 to Figure 9

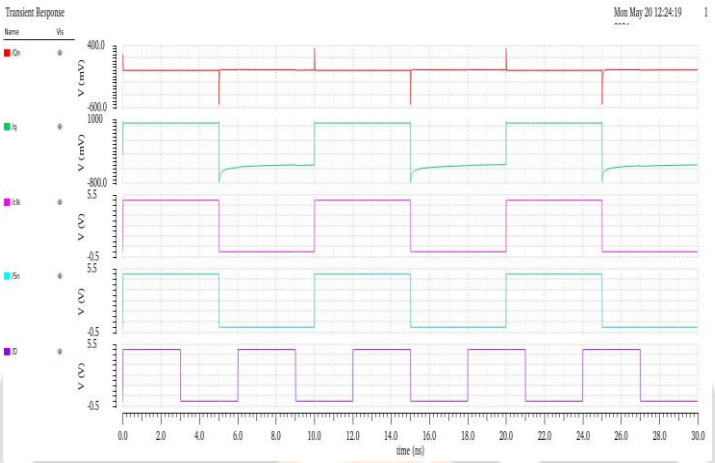

Fig 8 TransientAnalysis

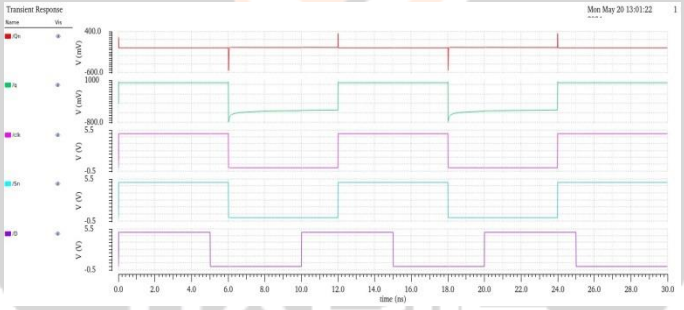

Fig 9 Transient Waveform

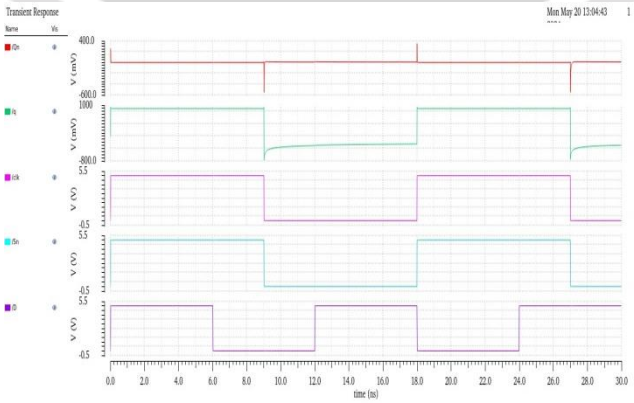

Fig 10 Transient Waveform

V Conclusion

A low power, high-speed sense amplifier-based flip-flop (SAFF) is designed using 45nm technology. The SA stage is designed to minimise the SAFF pre-charge power. The SA stage is equipped with a single-ended latch

that is glitch free and contention-free. The new SA stage and single-ended latch combine to optimise the delay of the SAFF as well as the power consumption. A power-delay product from the proposed SAFF offers a significant improvement compared to the conventional SAFF design. When compared to the MSFF, the SAFF offers superior performance. The advantages of the SAFF are: Reduce pre-charge power Ensure Glitch-Free, Contagion-Free Transitions Provide a Reliable and Efficient Solution for Modern Electronic Applications Adopt the proposed SAFF instead of MSFFs and you will see significant improvements in the overall system performance, especially in applications with high power efficiency and high speed.

VI Future Scope

SAFFs offer advantages over traditional flip-flops in terms of power consumption, operation speed, and noise resistance. SAFFs have become a key component of digital circuit design and are expected to continue to gain traction in the future, particularly as digital systems continue to develop and require higher performance and efficiency.

Lower Power Consumption:

The future of SBA is bright. There is huge potential for SBA in low power, high speed and high-performance computing. SBA's integration into high-tech semiconductor technologies, and emerging fields such as IoT, AI and quantum computing, will drive SBA growth and adoption.

High Speed Performance

As devices become smaller and apps powered by batteries become more popular, SAFFs' low power characteristics become more prevalent. SAFF's consume less energy than a flip-flop and are ideal for use with mobile and portable devices. This trend is only expected to continue as the need for energy-efficient electronics grows.

Advance Process Technology

SAFFs offer high-speed processing, which is a key requirement for high performance computing applications. As demand for high performance processing increases in areas such as data centers, artificial intelligence (AI) and real time processing, SAFF adoption is expected to grow.SAFFs can be optimized to meet the demands of semiconductor manufacturing technology. With the advancement of process nodes from 7nm to 5nm and beyond, SAFFs are able to operate at low voltage and high speed, which makes them suitable for NGEI (Next Generation Integrated Circuit).

Internet Of Things

As IoT devices continue to proliferate, there is a growing demand for low-power, high-speed, and energy-efficient solutions that can provide intermittent, highly-latency communications. This is where SAFFs come in.

Robustness in Advance Conditions

In addition, SAFFs are more tolerant of noise and process variations, which is increasingly important in environments with high levels of electromagnetic interference or temperature variations. SAFFs are therefore suitable for use in automotive, industrial, and aerospace applications where reliability is a priority.

Integration in 3D ICs

SAFFs are playing a vital role in today's 3D market, where several layers are layered to improve performance and reduce size. SAFF's high-speed and low-power characteristics match the vertical communication needs of a 3D IC.

Quantum Computing Interfaces

As quantum computing advances, the interface between quantum processors and traditional control electronics will be crucial. SAFFs' high-speed and low-power capabilities could be utilized in such interfaces to deliver high-fidelity data transfer.

Machine Learning and AI Accelerators

In the rapidly expanding field of AI and ML, high performance accelerators require high-speed data processing circuits that consume low power.SAFFs can be used in the development of high-speed, high-performance AI accelerators in order to improve their performance and reduce their power consumption.

Customizable Architectures

SAFFs can also be designed in a way that allows them to be tailored to a particular application. For instance, a SAFF can be designed for a specific application, such as a customized clock gate to lower power consumption, a dynamic voltage gate, a frequency scaling gate, or another power management method. This flexibility will become increasingly important as more applications are developed.

Research and Development

SAFFs will continue to advance with the development of new materials such as SC or Graphene, as well as novel transistor architectures like FinFET or GAAFET.

References

[1] Teh, C.K.; Fujita, T.; Hara, H.; Hamda, M. A 77%energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40nm CMOS. In Proceedings of the IEEE Int. Solid-State Circuits Conf, San Francisco, CA, USA, 20–24 February 2011.

[2] Suzuki,V.;Odagawa,K.;Abe,T.ClockedCMOScalculatorcircuitry. IEEE J. Solid-State Circuits 1974,8,462–469.

[3] Partovi, H.; Burd, R.; Salim, U.; Weber, F.; Digregorio, L.; Draper, D. Flow-through latch and edge triggered f lip-flop hybrid elements. In Proceedings of the IEEE International Solid-State Circuits Conference, Digest of TEchnical Papers, ISSCC. San Francisco, CA, USA, 8–10 February 1996.

[4] Na ziger, S.D.; Colon-Bonet, G.; Fischer, T.; Riedlinger, R.; Sullivan, T.J.; Grutkowski, T. The implementation of the Itanium 2 microprocessor. IEEE J. Solid-State Circuits 2002, 37, 1448–1460.

[5] Alioto, M.; Consoli, E.; Palumbo, G. General strategies to design nanometer flip-flops in the energy-delay space. IEEE Trans. Circuits Syst. I, Reg. Papers 2010, 57, 1583–1596.

[6] Pan, D.; Ma, L.; Cheng, H.; Min, H. A Highly E cient Conditional Feedthrough Pulsed Flip-Flop for High-Speed Applications. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2020, 28, 243–251.

[7] Matsui, M.; Hara, H.; Uetani, Y.; Kim, L.; Nagamatsu, T.; Watanabe, Y.; Chiba, A.; Matsuda, K.; Sakurai, T. A 200 MHz 13 mm 2D DCT macrocell using sense-amplifying pipeline flip-flop scheme. IEEE J. Solid-State Circuits 1994, 29, 1482–1490.

[8] Borivoje Nikolic´, Member, IEEE, Vojin G. Oklobdzija ˇ , Fellow, IEEE, Vladimir Stojanovic´, Wenyan Jia, Member, IEEE, James Kar-Shing Chiu, and Michael Ming-Tak Leung,Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements,IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 6, JUNE 2000.

[9] Anoop D, Dr. Nithin Kumar Y. B., Dr. Vasantha M. H., High Performance Sense Amplifier based Flip Flop for driver applications,IEEE International Symposium on Nanoelectronic and Information Systems, pp. 129-132, doi: 10.1109/iNIS.2017.35,2017.