AN APPROACH TO FINFET USING TERNARY LOGIC

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ABSTRACT

Ternary Logic is advantageous choice to substitute binary logic as it is energy efficient and due to easiness, as interconnect and chip area are reduced. As CMOS technology is scaling down to nanometer regime there are many problems occurring such as short channel effect, DIBL and Hot electron Effect, these problems can be overcomed by replacing traditional CMOS by FinFET. These two methodologies are of great advantage and can result in new turn in nanoelectronics. Many circuits can be build up by using FinFET working on ternary logic rather than binary and the main is ALU as it is the heart of CPU. So designing circuits by these two methodologies has a great impact on upcoming technologies.

Keywords*: FinFET, CMOS, ALU, Ternary logic.*

1. INTRODUCTION

As nowadays CMOS is been scaled down to nanometer there occurs many drawbacks as short channel effect, Drain induced Barrier Lowering and hot electron effect. FinFET has a great control over short channel effect making it a booming technology. Replacing binary logic with ternary has many advantages as number of connections and complexity is reduced, speed of transmitted information serially is faster. By summing up these two technologies is a boon.

1.1 Ternary Logic

Ternary logic are functions, when third value is added to binary logic. Here 0,1and 2 denote the values as false, undefined, and true, respectively. Any n variable {X1, ..., Xn} ternary function f(X) is defined as a logic function mapping {0, 1, 2}n to {0, 1, 2}, where[2]

$$X = \{X1, \ldots, Xn\}.$$

The basic operations of ternary logic can be defined as follows, where

$$Xi,\ Xj = \{0, 1, 2\}:$$
$$Xi + Xj = \max\{Xi, Xj\}$$
$$Xi \bullet Xj = \min\{Xi, Xj\}$$
$$Xi = 2 - Xi. \quad (1)$$

Here + and • denotes OR, AND respectively and – represents subtraction. By the perspective of theory, multivalued circuits should have below advantages over binary logic: Numbers of connection inside the chip is reduced in MVL as each wire transmits more information as compared to binary. Complexity of circuit is decreased as each MVL element process more information. As large chip contains more pins, the ON and OFF connections are reduced with the use of MVL logic. As the transmitted information per unit time is increased the speed of serial information will be faster.

1.1 FinFET

As the minimum channel length of MOSFET has been shrinking continuously while fabricating. Minimum Channel length results in high speed devices in VLSI [1]. Thus while narrowing down the

conventional bulk devices it results in barrier as per the law of physics which is needed to be overcome while scaling the device. As device technology lowers down to 5nm while extending Moore's, FinFET is the most promising of all. It tackles the problem of sub-threshold leakage, poor short-channel electrostatic behavior and high device parameters variability that plagued planar CMOS as it scaled down to 20 nm. Secondly, it is able to operate at lower supply voltage which extends voltage scaling which was leveling off and allowed further badly needed static and dynamic power savings.

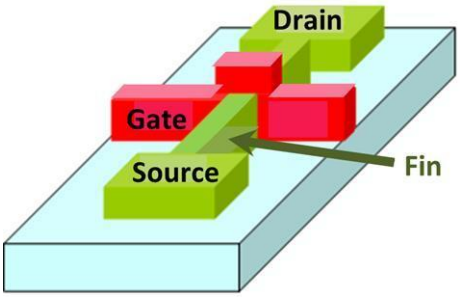

FIG 1. FINFET DEVICE

The advantage of FinFET over MOSFET is that it take more drive current per unit area than planar devices, Next the height of the fin can be used to create a channel with a larger effective volume but still have advantage of a wraparound gate. While at lower power FinFET has additional capability to achieve high frequency numbers.

One important feature of FinFET is the fin thickness, which needs to be smaller than or equal to the gate length. Their scaling does not depend on oxide thickness, which is a big advantage because it's the process lithography that defines the FET characteristics at each new process node

2. TERNARY CIRCUIT DESIGN

2.1 STANDARD TERNARY INVERTER [2]

The fundamental part of most logic is Inverter and other of them are NAND and NOR gates which are constructed according to their structure. The same is valid for radix-3(ternary) and higher of them. Hence, when an efficient design of ternary inverter is implemented it results in enhancement of overall performance. Inverter is a great driver with its operation as well has a great driving capability. Ternary logic has three ways to define inverter as STI, PTI and NTI .PTI and NTI are binary inverters as they give two levels "0" and "2" at output. However, STI is the most e at the output. Below figure describes the schematic of S hich adds output values of a PTI and a NTI cell by means

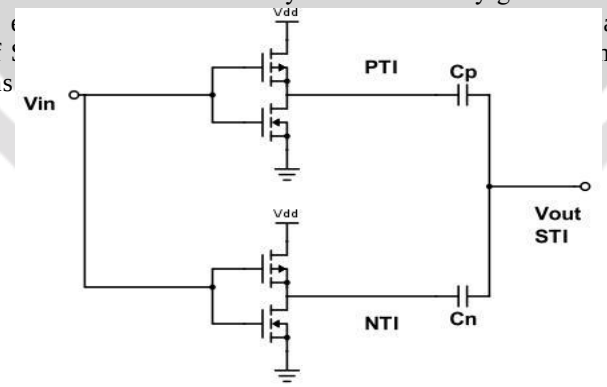

FIG 2. SCHEMATIC OF DESIGN FOR A STI [2]

To have same weighting factor for two Cn and Cp capacitors, they should be identical. Hence the output voltage is as follows:

$$\text{Vout} = \frac{\text{V NTI} + \text{V PTI}}{2}$$

Thus, the output voltage of STI will be 2 the mean value of the NTI and PTI output voltages. Now if , connection node of capacitor is as follows:

$$\text{Vout} = \frac{\text{Cp V NTI} + \text{Cn V PTI}}{\text{Cp} + \text{Cn}}$$

Input is logic "0" the output of NTI and PTI will be logic "2" and then V_{out} is "2". Now again when input is taken as "2" the output of NTI and PTI will be "0" thus V_{out} is "0". Finally input as logic "1"NTI will be "0" and PTI will be "2". Thus by equation above Vout will be "1".

Vin	NTI	PTI	STI
0	2	2	2
1	0	2	1
2	0	0	0

TABLE 1: TRUTH TABLE OF TERNARY INVERTER [2]

The three major advantages are:

1) No static power consumption
2) VDD/2 power supply not needed
3) Compatible with standard CMOS technology and producing three ternary outputs concurrently.

2.2 TERNARY DECODER [5]

Ternary decoder is given a one-input and taken three-output combinational circuit and generates unary functions for an input x.
Response of the ternary decoder to the input x is given:

$$\boldsymbol{Xk} = \begin{cases} \boldsymbol{2, if\ x = k} \\ \boldsymbol{0, if\ x \neq k} \end{cases}$$

INPUT X	OUTPUT X1	OUTPUT X2	OUTPUT X3
0	2	0	0
1	0	2	0
2	0	0	2

TABLE 2: TRUTH TABLE OF TERNARY DECODER [5]

3. COMPARISION OF FINFET OVER MOSFET

A FinFET is a MOSFET with the channel elevated so the gate can surround it on three sides. It has number of advantages over MOSFET. From designer's perspective 1) Higher Transconductance 2) Lower apparent input capacitance for the same gain 3) Less wafer area per transistor 4) Fully depleted structure, enabling better on/off contrast 5) Lower dynamic power consumption. From customer/user perspective 1) Faster Switching Speed

2) lower power consumption.

A Full Adder is designed using CMOS and FinFET technology, both the schematics designed are simulated and some parameters are compared as shown below

Parameters	CMOS based Full Adder	FinFET based Full Adder
No. of Transistors	28	10
Technology used	45nm	45nm
Supply voltage	0.07v	0.07v
Delay	3.94ns	2.35ns
Efficiency	52.3%	96.56%
Leakage Power	1.594Pw	1.09pW
Leakage Current	652.4Na	1.714nA

TABLE 3: COMPARISION BETWEEN RESULTS OF CMOS AND FINFET [4]

By this above comparison it is predicted that FinFET is advantageous than CMOS.
An 8-bit Arithmetic Unit is designed by CMOS as well FinFET and their leakage power is compared.

Design	Technology	Maximum Power Consumed
MOSFET	32nm	42.7mW
FinFET	32nm	25mW

TABLE 4: COMPARISION BETWEEN POWER CONSUMED OF CMOS AND FINFET [7]

By the above comparison it is noted that while working on same technology, the maximum power consumed by FinFET is less as compared to MOSFET.

4. TERNARY ALU

Figure represents the proposed block diagram of ternary ALU. It consists of two inputs A and B, two select lines X and Y and some functions been done by the ALU such as sum, difference, multiply and some logical calculations. The Adder, Subtractor, Multiplier and basic gates are made up from FinFET operating on ternary logic.

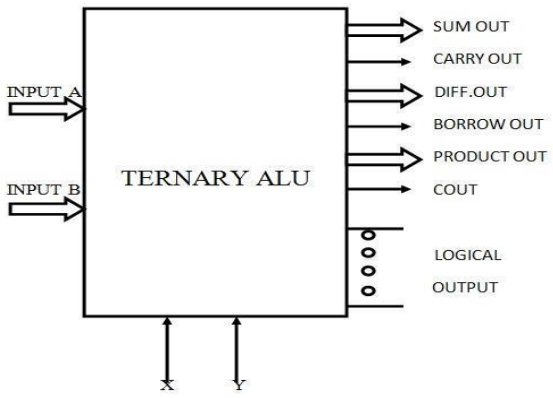

FIG 4: BLOCK DIAGRAM OF TERNARY ALU

5. CONCLUSION

As nowadays CMOS is been scaled down to nano meters there occurs many drawbacks as Short channel effect, Drain Induced Barrier Lowering (DIBL) and hot electron effect. FinFET has great controllability over short channel effect thus making it as a booming technology replacing CMOS. Proposing any circuit based on Ternary Logic using FinFET can be reliable because by Using Ternary Logic, it is possible to accomplish simplicity & energy efficiency in modern digital design.

6. REFERENCES

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