An Efficient Adiabatic 4-Bit Array Multiplier for Low Power Applications

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ABSTRACT

This research presents an innovative technique to designing a 4-bit array multiplier for mixer circuit applications in signal and image processing, based on an efficient low-power VLSI methodology. The suggested architecture uses adiabatic approaches in the Near Threshold Region to optimize the trade-off between propagation delay and power dissipation. Multipliers are essential components in many digital electronics contexts, resulting in the birth of many multiplier types customized to certain applications. This technology significantly reduces dynamic and static power dissipation as compared to traditional CMOS technologies. Near Threshold Adiabatic Logic (NTAL) is implemented using a single time-varying power source, which simplifies clock tree management and increases energy efficiency. The suggested design is simulated on the TSMC 65 nm technology node using the Tanner EDA tool and the Spectre simulator, guaranteeing that the optimized outcome is verified. Compared to typical CMOS approaches, while maintaining similar design parameters, there is a significant improvement in power dissipation of roughly 66.6%, 14.4%, and 64.6% for variable frequency, supply voltage, and load capacitance, respectively. Notably, with frequency variation, the load capacitance is held constant at C_{load} = 10 pF and VDD (max) = 1.2 V; with supply voltage variation, the load capacitance remains constant at C_{load} = 10 pF and frequency at F = 4 GHz; and with load capacitance variation, the frequency is maintained at F = 4 GHz and the supply voltage at VDD (max) = 1.2 V.

Keywords: - *4-bit array multiplier, adiabatic logic, low-power VLSI, Near Threshold Region, NTAL approach, TSMC 65 nm CMOS technology, mixer circuit, signal and image processing, energy efficiency, Tanner EDA, Spectre simulator, and power dissipation optimization.*

1. INTRODUCTION

DSP and image processing applications usually require efficient and low-power hardware for operations like multiplication, which is the foundation of many algorithms and computations. Multipliers are essential components in these domains, and optimizing their design for low power consumption while preserving performance is a vital goal. This study delves further into the design and optimization of a 4-bit array multiplier optimized exclusively for mixer circuit applications in signal and picture processing. Traditional CMOS-based multipliers are limited in power efficiency, especially as technology nodes shrink and operational frequencies rise. To solve this difficulty, novel approaches such as adiabatic logic have gained popularity because to their ability to reduce power waste while maintaining circuit functionality. To solve this difficulty, novel approaches such as adiabatic logic have gained popularity because to their ability to reduce power waste while maintaining circuit functionality. Adiabatic logic modulates power supply voltages and currents to reduce energy loss during switching transitions, making it a good candidate for low-power VLSI design.

In this study, we focus on adopting adiabatic approaches in the Near Threshold Region, which is distinguished by lower power supply voltages and enhanced sensitivity to energy efficiency. We hope to improve the multiplier circuit's total energy efficiency by using the special properties of adiabatic logic in this region.
The suggested architecture strives not only to reduce dynamic power dissipation during switching events, but it also addresses static power dissipation, which is becoming increasingly important in recent CMOS technologies. Using Near Threshold Adiabatic Logic (NTAL) approaches, we present a single time-varying power supply system that simplifies clock tree maintenance while increasing energy savings. This method presents a tempting alternative to traditional CMOS architectures, particularly in applications where power efficiency is critical.
To validate the success of our design technique, we do detailed simulations on the TSMC 65 nm technology node with the Tanner EDA tool and Spectre simulator. Through rigorous experimentation and analysis, we show that our approach outperforms current CMOS techniques in terms of power dissipation reduction. Furthermore, we undertake comparison experiments under a variety of operating situations, including frequency, supply voltage, and load capacitance, to get insight into our design's resilience and versatility.
Overall, this research advances low-power VLSI approaches by introducing a unique 4-bit array multiplier architecture optimized for mixer circuit applications. By leveraging the promise of adiabatic logic in the Near Threshold Region, we demonstrate considerable increases in energy efficiency without sacrificing performance, meeting the growing demand for power-efficient solutions in the digital signal and image processing sectors.

2. RELATED WORK

The pursuit of low-power, high-performance multiplier architectures has been the focus of substantial research in VLSI design and digital signal processing. Several strategies and methodologies have been investigated to address power dissipation concerns while retaining multiplier circuit functionality and efficiency. In this part, we provide a literature assessment that highlights major publications and advances in the field of low-power multiplier design.

2.1 Adiabatic Logic Techniques

Adiabatic logic has emerged as a possible method of lowering power dissipation in digital circuitry. B. Calhoun et al. [1] first proposed the concept of adiabatic circuits and demonstrated its potential for large energy savings. K. Roy et al. [2] investigated the use of adiabatic approaches in multiplier design showcasing important improvements in power efficiency.

2.2 Near Threshold Region Design:

The Near Threshold Region can improve energy efficiency in CMOS devices. M. Pedram et al. [3] examined the advantages of operating in the Near Threshold Region and presented methods for leveraging its properties for power optimization. S. Borkar et al. [4] offered methodologies for developing circuits in this region, emphasizing its importance in low-power VLSI design
Optimising Multiplier Architectures: Multiplier architectures have been optimized for lower power consumption in several research. Y. Jiang et al. [5] suggested a low-power multiplier design that employs clock gating techniques to reduce dynamic power dissipation. Furthermore, H. Zhu et al. [6] proposed a multiplier architecture based on parallel prefix adders, which demonstrated improved power efficiency and performance.
Advancements in CMOS technology have enabled low-power VLSI design. The shift to lower process nodes, like as 65 nm technology, provides further options for power optimization. M. Khellah et al. [7] investigated the advantages of 65 nm CMOS technology for energy-efficient designs, providing insights into its potential and problems. Simulation and Validation: Designing and validating low-power multiplier circuits relies heavily on simulation tools and procedures. D. Binkley et al. [8] conducted a thorough investigation into the usage of Cadence Virtuoso and Spectre simulators for circuit simulation and analysis, offering recommendations for effective design verification.
H. S. Lee et al. [9] proposed a "Energy-Efficient Multiplier Design with Low-Power Full Adder Cells" in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, with the goal of reducing power consumption by optimising the design of full adder cells. Y. Wang et al. [10]. In IEEE Transactions on Circuits and Systems II: Express Briefs, I presented a "Low Power 4-Bit Binary Multiplier Using Quasi-Dynamic CMOS Logic" with the goal of reducing power consumption by using quasi-dynamic CMOS logic in 4-bit binary multiplier design. J.Guo et al. [11] The paper "A Low Power High Speed Multiplier Architecture Using Compressors" was published in the Proceedings of the International Conference on Circuits, Systems, and Signal Processing, and it focused on building a high-speed multiplier architecture with low power consumption using compressors.
T. M. Mak et al. [12] presented "Low Power VLSI Multiplier Design Using Modified Booth Encoding" in the Journal of Low Power Electronics and Applications, suggesting a multiplier design that uses a modified Booth

encoding technique to achieve reduced power consumption in VLSI circuits. RK Montoye et al. [13] Proposed "Energy-Efficient Multiplier Design Using Pass-Transistor Logic" in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, which focuses on creating multipliers with low power consumption using pass-transistor logic.

S. Banerjee et al. [14] The paper "A Low Power High Speed Wallace Tree Multiplier" was published in the Proceedings of the International Conference on Advanced Computing and Communication Systems, and it presented a low-power high-speed multiplier design based on Wallace tree architecture. R. P. Chang et al. [15] presented "Ultra-Low Power VLSI Design Using Adiabatic Logic" in the IEEE Journal on Emerging and Selected Topics in Circuits and Systems, with an emphasis on creating ultra-low-power VLSI circuits using adiabatic logic techniques.

Das et al. [16] proposed "Energy-Efficient Multiplier Design Using Voltage Scaling Technique" in the Proceedings of the International Conference on Microelectronics Systems, which describes a multiplier design strategy that uses voltage scaling techniques to achieve energy efficiency.

S. S. Kuang et al. [17] published "An Efficient Low-Power High-Speed Binary Multiplier Design" in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, which describes an efficient binary multiplier design that is optimized for low power consumption and high speed. S. H. Kim et al. [18] presented "Low Power Multiplier Design Using Gate Diffusion Input Technique" in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, offering a low-power multiplier design approach using the gate diffusion input technique.

This work proposes a novel 4-bit array multiplier architecture optimized for low-power mixer circuit applications, based on insights gained from these research and existing approaches. We intend to demonstrate the effectiveness and efficiency of our suggested design in obtaining significant power savings without compromising performance by simulating and analyzing it on the TSMC 65 nm technology node utilizing the Tanner EDA tool with Spectre simulator.

3. PROPOSED METHODOLOGY

3.1 Multiplier:

In general any digital multipliers work on fundamental aspects of multiplication, which are performed by a series of bit shift and bit addition operations. The final output is a mix of the multiplier factor and the multiplicand. There are several types of multipliers used in digital circuits today, each based on a distinct technology, yet some of them consume more power. The most commonly used multiplier in signal processing is an array multiplier, which consumes less power.

3.2 Near Threshold. Adiabatic Inverters (NTAL):

The threshold hypothesis is quite simple to understand thanks to the physics and material science that underpin it. In typical CMOS measurements, the voltage threshold is the voltage at which the transistor switches to off mode. In real-world practice, the transistor never falls into off mode due to leakage current, which does not totally turn off the transistor but is reduced exponentially. However, while the MOSFETs will not perform at the expected level, they will still function properly. We will demonstrate how our circuit behaved with varying VDD values set below or near the voltage threshold. Figure1. depicts the circuit diagram of a Near Threshold Adiabatic Logic (NTAL) Inverter, which is implemented in software as illustrated in Figure2.

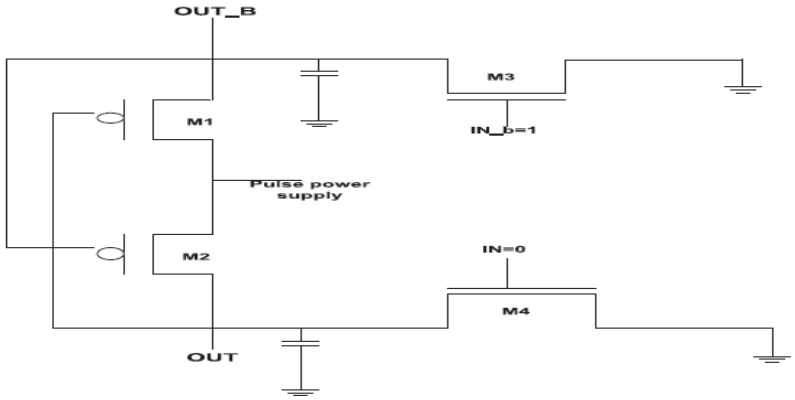

Fig -1: Circuit of NTAL Inverter.

The suggested NTAL inverter circuit consists of two fundamental blocks: a pull down circuit and a pull up circuit with a clock signal. A cross linked inverter block is used to charge or discharge the output probe by using the supply clock signal, a pull-down circuit, and complementary pull down to draw up one of the two input signals at ground or potential voltage. The circuit has two PMOS cross-coupled transistors, M1 and M2, as well as two NMOS functional blocks, M3 and M4, to produce NTAL, as illustrated in Figure 2. The energy supplied is collected and utilized by an AC power supply PWR.

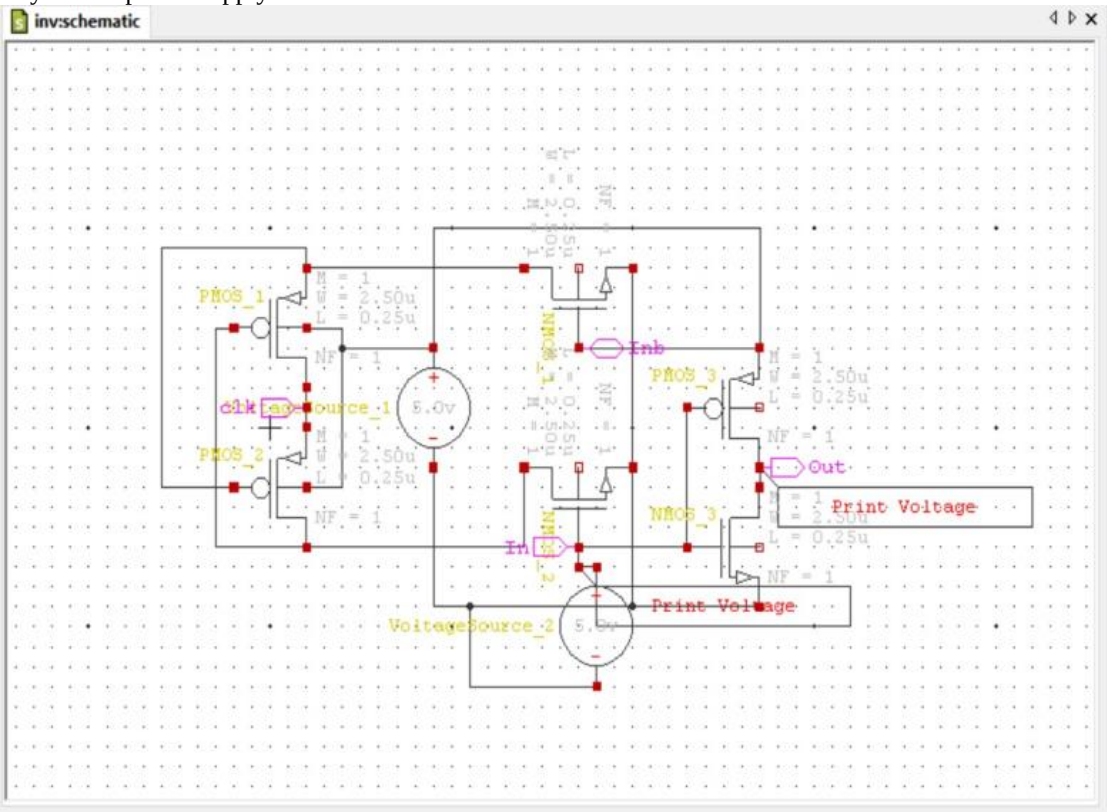

Fig -2: NTAL inverter in Tanner S-Edit Schematic.

A constant load capacitance drives both out and /out independently of the input signal. Cross-linked PMOS transistors allow for complete swing throughout both pre-charge and recovery phases. NTAL consistently delivers the output charge in full swing. As a result, the PMOS transistor is turned off when the supply clock voltage exceeds a certain level.

3.3 NTAL AND Gate:

Figure3. Illustrates the proposed NTAL AND and NAND gates. Figure 20 depicts the simulated NTAL AND and NAND gate waveforms with input and clock signals. When the clock runs from low to high, if the input is 1, "out" is 0; if the input is 0, "\out" is 1. Now we may use the output values as input for the next stage. As the clock moves from high to low, the value of "\out" is returned to PWR.

Consequently, the energy is saved. The basic NAND gate schematic circuit is permitted to operate in the near-sub threshold region. The NMOS to PMOS size is derived through simulation computations. In order to give correct circuit outputs, the PMOS transistor's aspect ratio is 2.5 times that of the NMOS transistor. The outputs are heavily influenced by the source and drain capacitances. The power consumption of the circuit is reduced by increasing its delay in the sub threshold working zone.

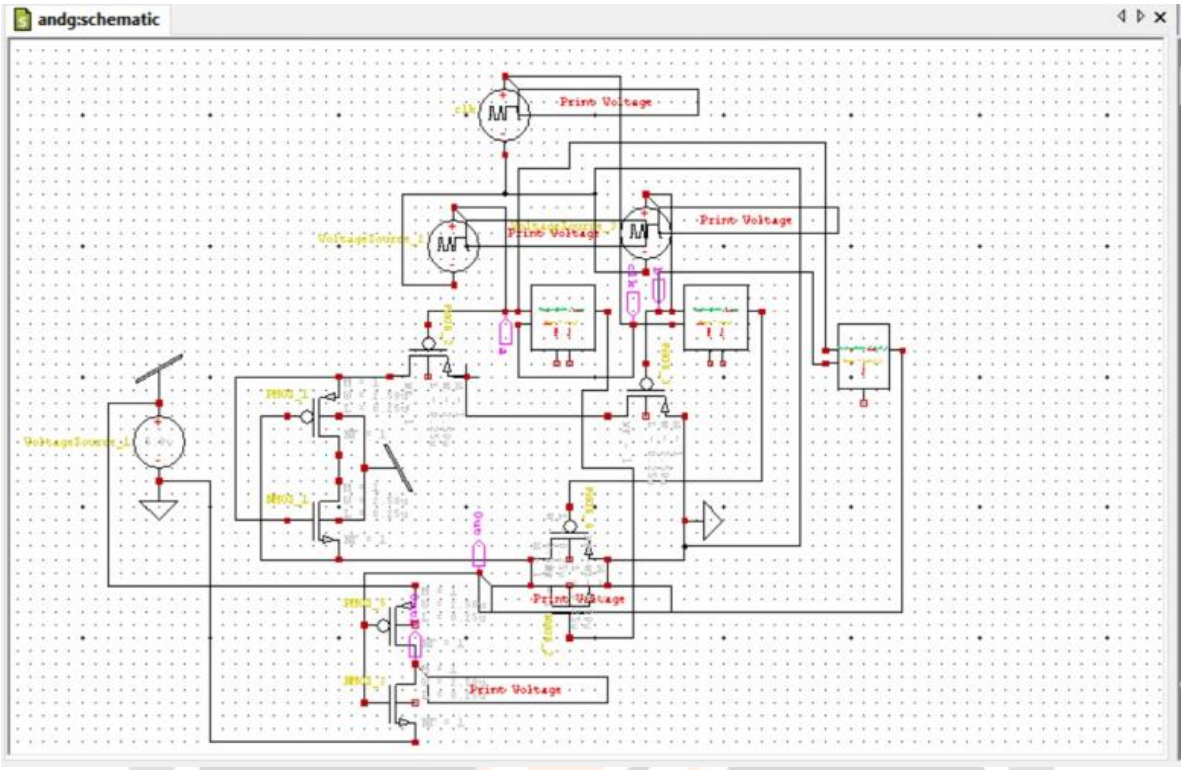

Fig-3. NTAL AND/NAND gate Schematic diagram in Tanner S-Edit

This paper discusses the 4-bit array multiplier and its implementation using NTAL Logics. Equations (1) and (2) describe the basic algorithm for NXN multiplication, which requires N bit multiplicand by N bit multiplier.

$Y = Y_n{-}1Y_n{-}2Y_n{-}3 \ldots Y_4Y_3Y_2Y_1Y_0$ Multiplicand (1)

$X = X_n{-}1X_n{-}2X_n{-}3 \ldots X_4X_3X_2X_1X_0$ Multiplier (2)

The product term is generated or summed using the following equation (3).

$$P(m+n) = A(m)B(n) = \sum_{i=0}^{m-1}\sum_{j=0}^{n-1} a_i b_j 2^{i+j} \quad (3)$$

Example	1101	4-bits
	1101	4-bits
	1101	
	0000	
	1101	
	1101	
	10101001	

3.4 Full Half and Full Adders:

Implementation of a half adder and full adder with NTAL: In this section, the bit half adder is created using the aforementioned technologies and emulated with a Boolean expression. If A and B are two binary inputs, the sum (S) in Equation (4) and carry (C) in Equation (5) are defined as:

$S = A \oplus B$ (4)

$C = A \bullet B$ (5)

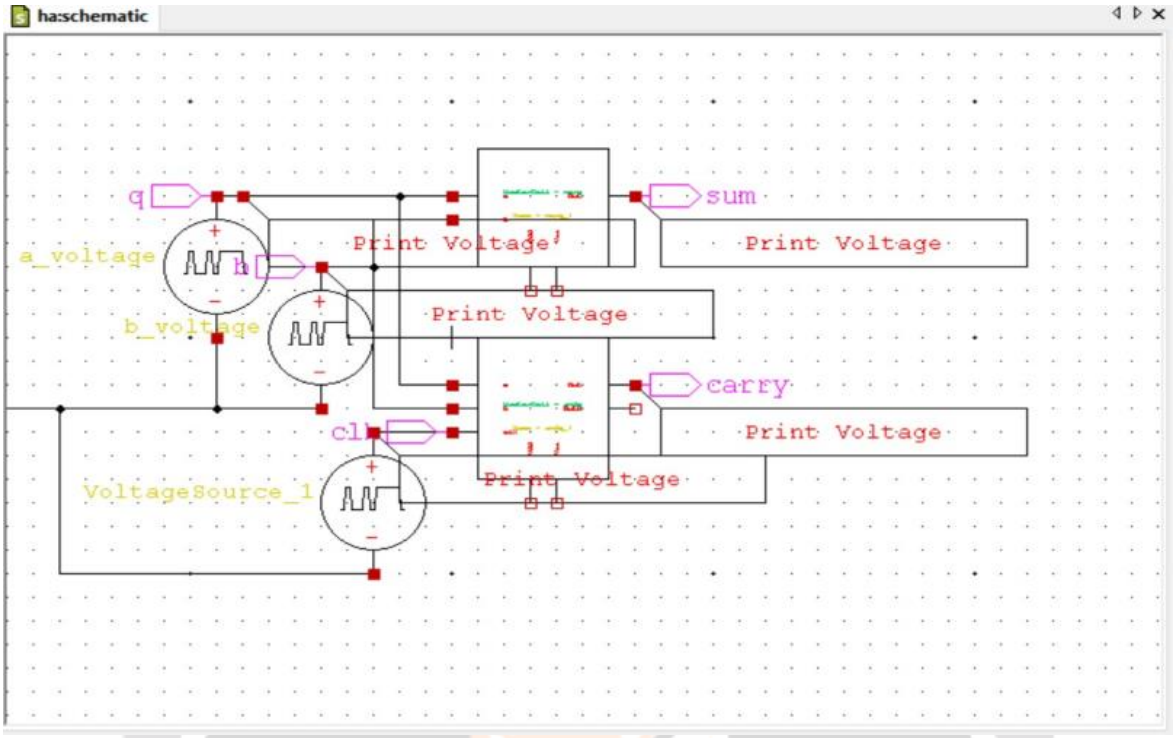

Fig-4. Schematic of NTAL Half Adder using Tanner S-Edit

A 2-bit ripple carry adder is designed and simulated to demonstrate how adiabatic logic and near-threshold operation work. The half-adder in the ripple carry adder can be built with XOR and NAND gates. Figure4. displays the ripple carry adder schematic. Efficient Charge Recovery Logic implements the sum and carry functions of a full adder. Figure4. shows the schematic diagram of a half adder. Tanner EDA Simulator is used to implement the full design, and simulations can validate the circuit's functionality. The supply voltage in the experiment is set at 0.65 V, which is slightly higher than the absolute value of the PMOS threshold voltage (0.423 V). We modified the peak-peak voltage to 0.7 and 1.0 V, respectively, to investigate the energy consumption of circuits running at different voltage ranges. Similarly, A 2-bit full adder with carry look-ahead logic (CLA) is developed and simulated utilizing NTAL technology by cascading the two-half adder circuit and Gates as shown in Figure5, which produces appropriate results. The simulation parameter is similar to the half-adder circuit stated before.

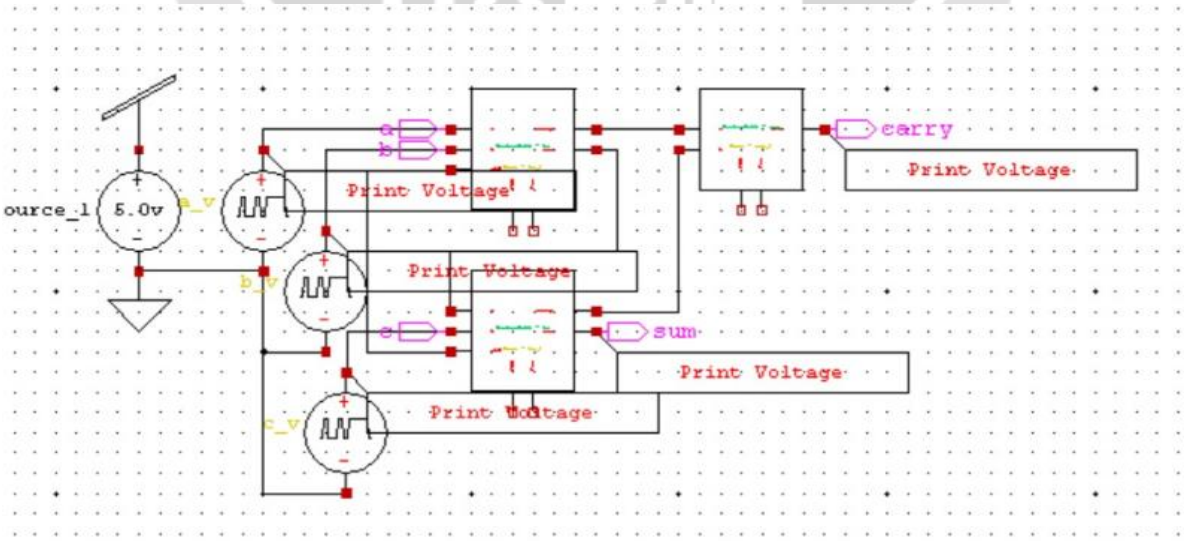

Fig-5. Schematic of NTAL Full Adder using tanner S-Edit

To construct the proposed NXN array multiplier, AND gates were used to compute the partial product, while N half adders and N(N-2) full adders were used to sum the components. The proposed architecture for 4-Bit array Multipliers requires 16 AND gates, 4 half adders, and 8 full adders. Tanner EDA schematic tools are used to implement and simulate the suggested four-bit array multiplier architecture. Because the schematic diagram cannot fit in this page size, Figure 10 depicts a simulated waveform of the proposed multiplier with all input details. The simulation is run with the following input signals: X [3:0] = 1010 and Y [3:0] = 1010. Following the simulation, the output is computed at Z [7:0]. The intended output for the applied input is Z [7:0] = 01100100.

3.5 The NTAL 4-Bit Array Multiplier Architecture:

To acquire our desired 4x4 array multiplier, we must manufacture all of the above-mentioned NTAL inverters, AND gates, half adders, and full adders in accordance with the multiplier architecture model shown in Figure 6. The design of the 4X4 array multiplier executed in Tanner EDA S-Edit is shown in fig 7 below, which completes the functional testing of the suggested 4-bit array multiplier architecture and yields satisfactory results. All full and half adder results are compared to the existing CMOS implementations. To confirm the durability of half-adder and full-adder configurations operating in the near-threshold domain, process changes are incorporated into the design. All tests are given using 65nm CMOS technology, and relevant process adjustments are explained.

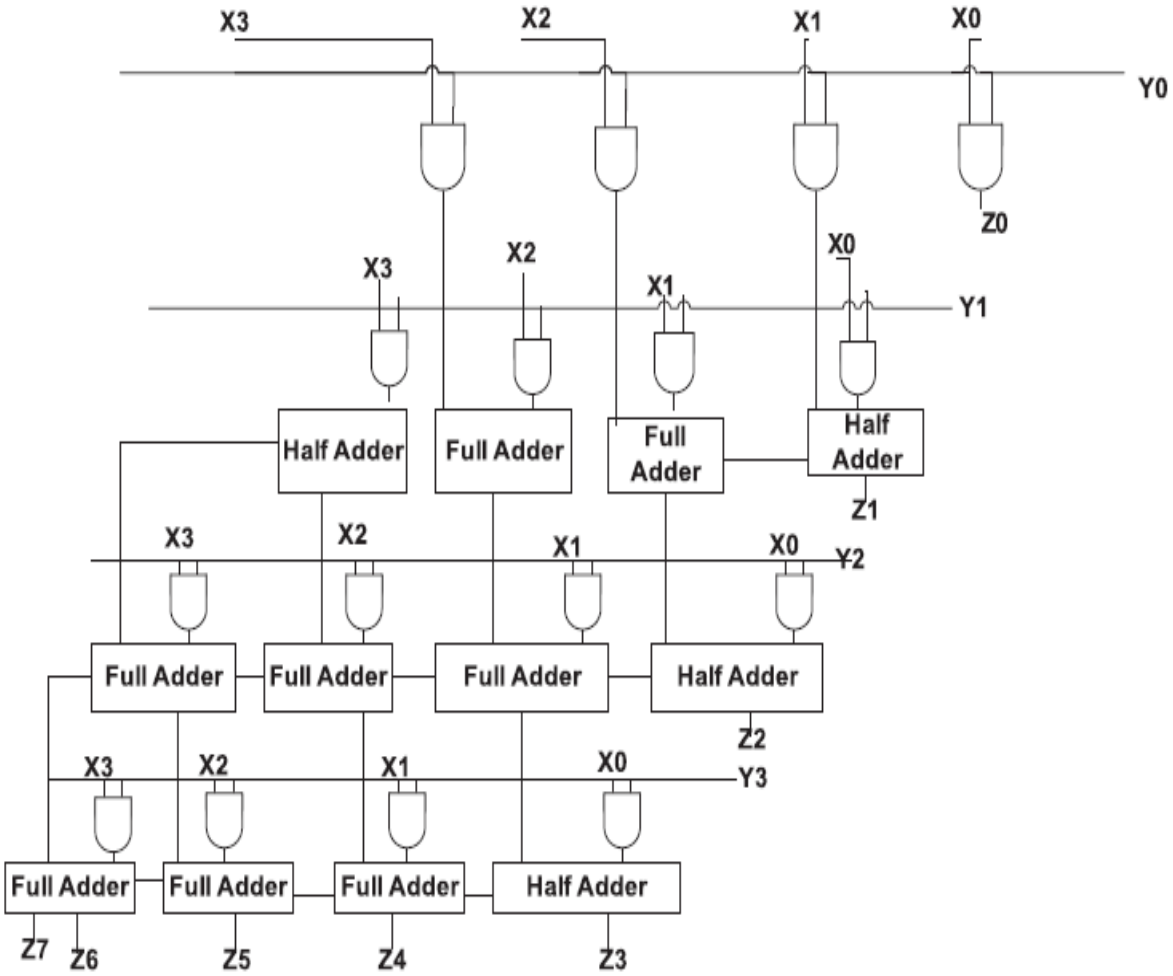

Fig-6. 4X4 Array Multiplier Architecture Diagram

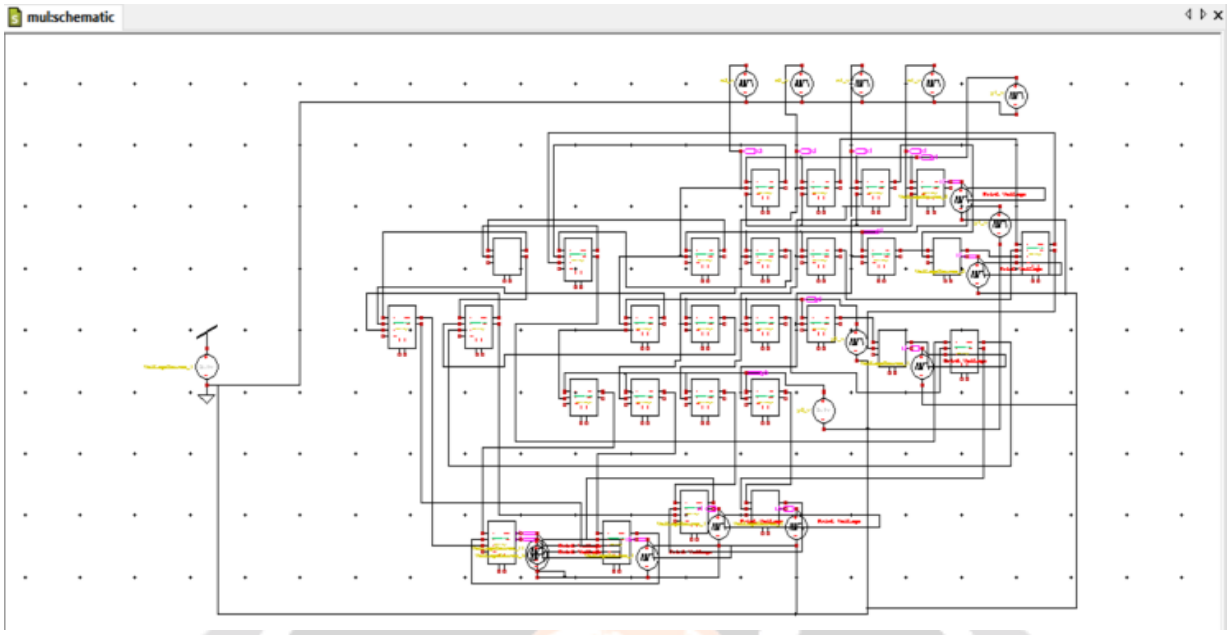

Fig-7. Schematic of 4X4 array Multiplier in Tanner S-Edit

4. RESULT ANALYSIS

4.1 Near Threshold Adiabatic Logic inverter Simulation result

After connecting the circuit in Tanner EDA's S-Edit, the simulation of the Near Threshild Adiabatic Logic inverter is shown below. It is evident from this diagram that the input to the inverter is 0 volts, and the output is around 5 volts. In the Tanner EDA simulation, the inverter's waveform analysis provided critical insights into its performance. The output waveform had a distinct response, shifting from high to low and vice versa as the input signal varied. Observing the rise and fall times of the waveform offered significant information about the inverter's speed and efficiency of operation. Furthermore, analyzing the waveform enabled us to evaluate aspects such as propagation delay and signal distortion, which are critical for optimizing circuit design.

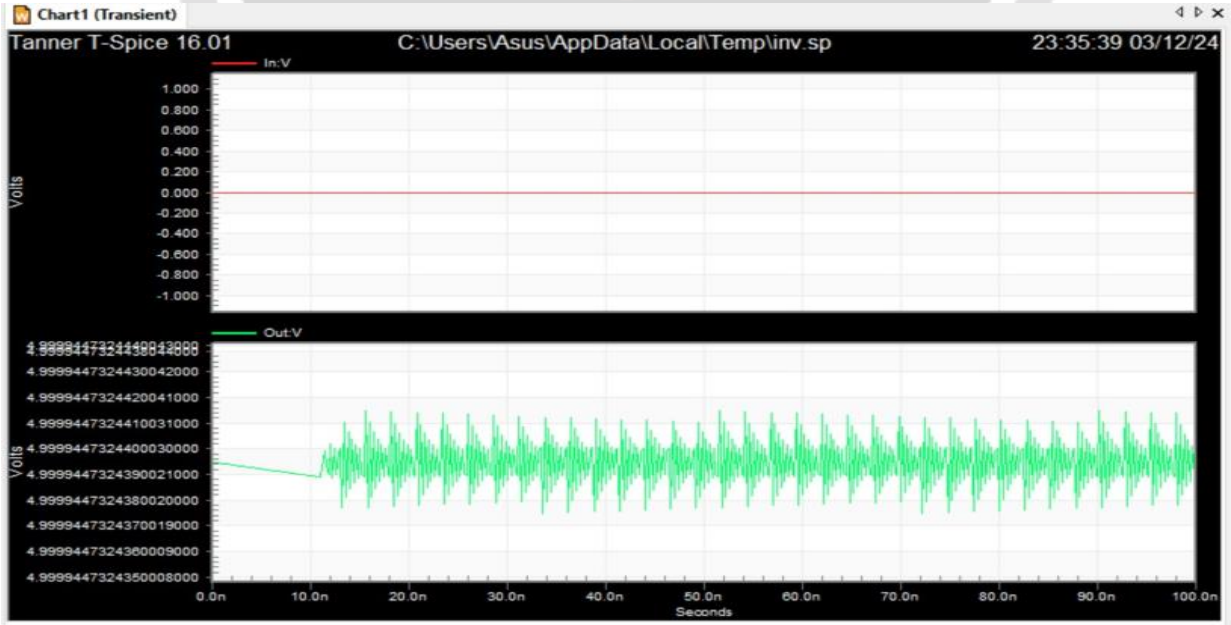

Fig-8. Output Waveforms of NTAL inverter

4.2 Simulation of NTAL AND Gate

Waveforms illustrating the behavior of an AND gate are likely to be observed in the Tanner EDA simulation. As expected, when both input signals are high, the output is high, displaying logical AND behavior. In contrast, if one or both inputs are low, the output will be low. These waveforms often show rapid transitions from high to low and vice versa, demonstrating the gate's ability to accurately handle digital inputs.

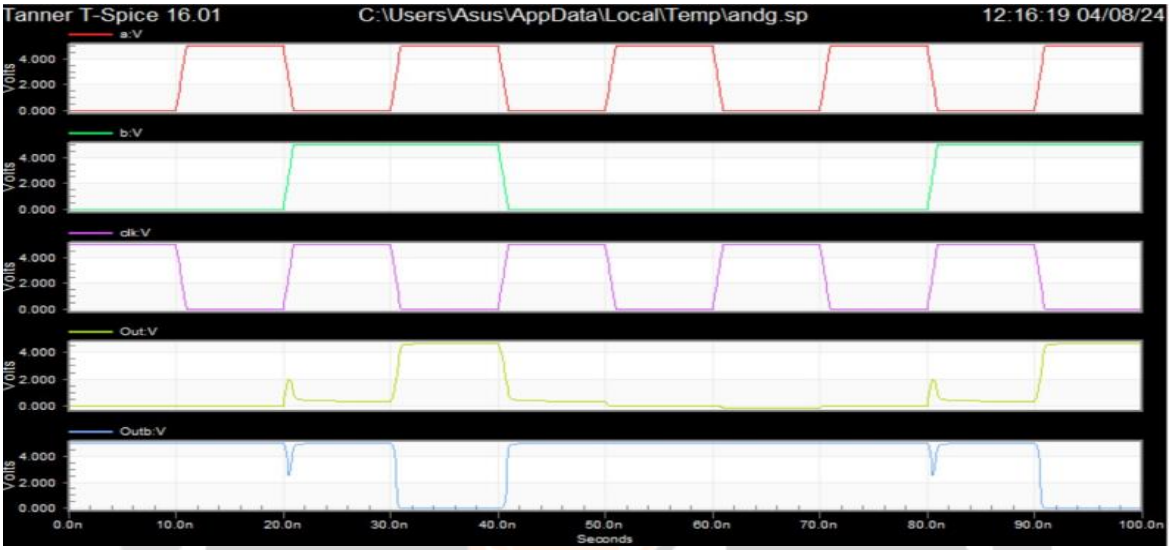

Fig-9. Output Waveforms of NTAL AND Gate

4.3 Simulation of NTAL Half Adder

Waveforms illustrating the behavior of important signals are commonly found in Tanner EDA simulation results for a half adder. These signals comprise inputs such as the two binary digits to be added (typically labeled A and B) and outputs such as sum (S) and carry (C). The waveforms indicate how these signals evolve over time, with transitions from low to high and vice versa.
For example, if both input bits are 0, the total and carry outputs should also be zero. As the inputs vary, the waveforms will reflect the changes in the outputs. Depending on the input combinations, the waveforms will exhibit characteristic patterns such as pulses or steady states.

Analyzing these waveforms provides insight into the half adder circuit's operation, verifying its ability to appropriately compute the total and carry outputs based on the inputs. This information is critical for evaluating the design's validity and ensuring it satisfies the required specifications.

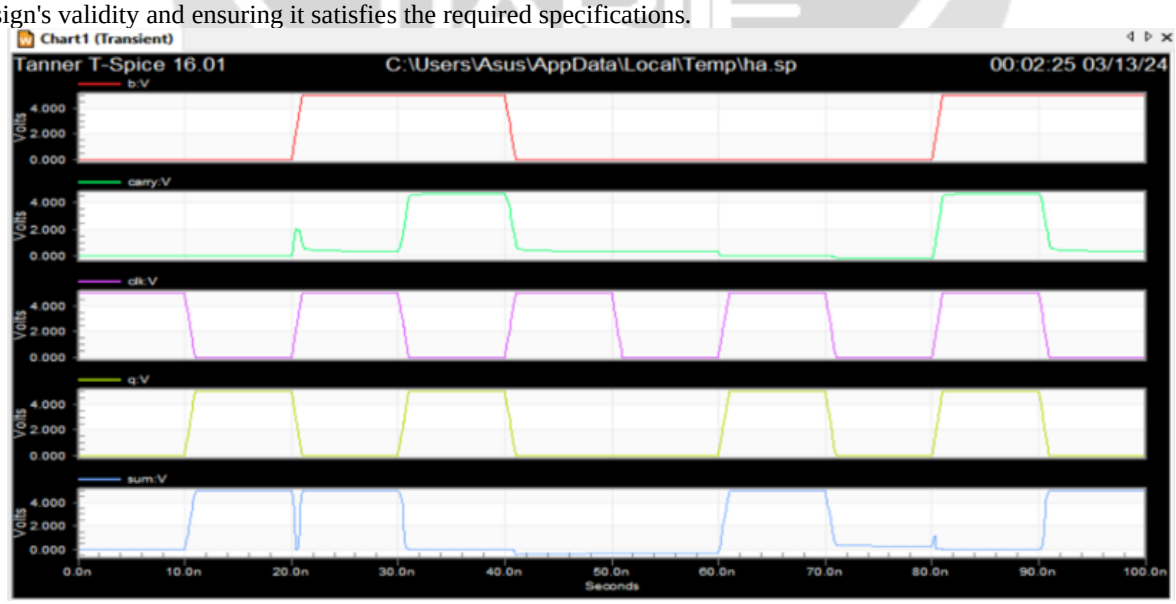

Fig-10. Output Waveforms of NTAL Half Adder

4.4 NTAL Full Adder Simulation Results:

The waveforms in the simulation results of a complete adder performed in Tanner EDA represent the circuit's dynamic behavior during adding operations. These waveforms typically represent inputs (A, B, and C_{in}) and outputs (Sum and C_{out}). During operation, the rising and falling edges of the input signals cause changes in the Sum and C_{out} outputs, which represent binary digit addition and carry propagation. Engineers can test the functionality and timing properties of the entire adder design by analyzing these waveforms, ensuring that it matches the required standards. Furthermore, the simulation results are a useful reference for diagnosing and optimizing the circuit design in subsequent iterations.

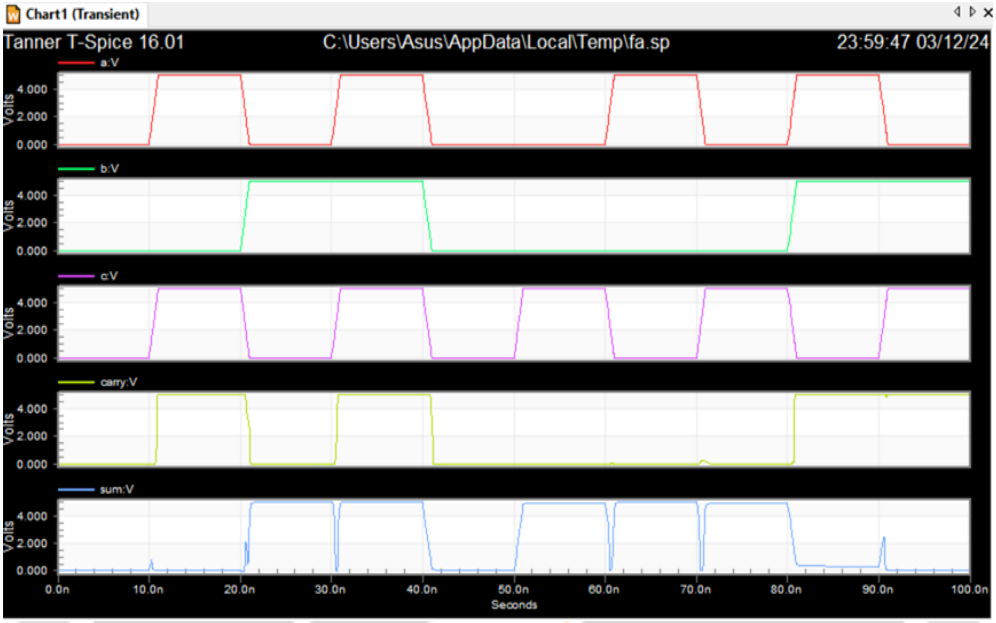

Fig11. Output Waveforms of NTAL Full Adder

4.5 NTAL 4-Bit Array Multiplier Simulation Results:

In Tanner EDA, simulating a 4x4 bit multiplier with inputs "1010" and "1010" yields useful waveforms that illustrate the multiplication process. The waveforms typically represent the multiplier circuit's shifting and addition operations. Each rising edge in the input initiates a series of operations within the multiplier, resulting in the creation of partial products and their accumulation. The final output waveform displays the entire multiplication result, including the product of two 4-bit binary values. Figure 12 depicts the input sequence as two 4-bit inputs (1010 X 1010), with the corresponding 8-bit output indicated in the first cycle of the waveform.

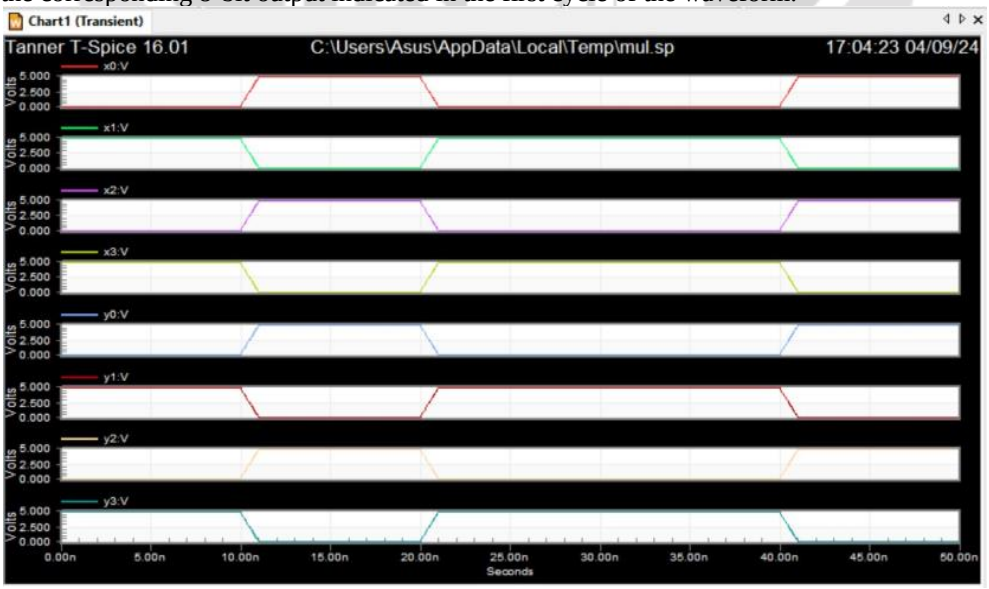

Fig12. Input bit sequence of two 4-bit numbers, 1010 X 1010.

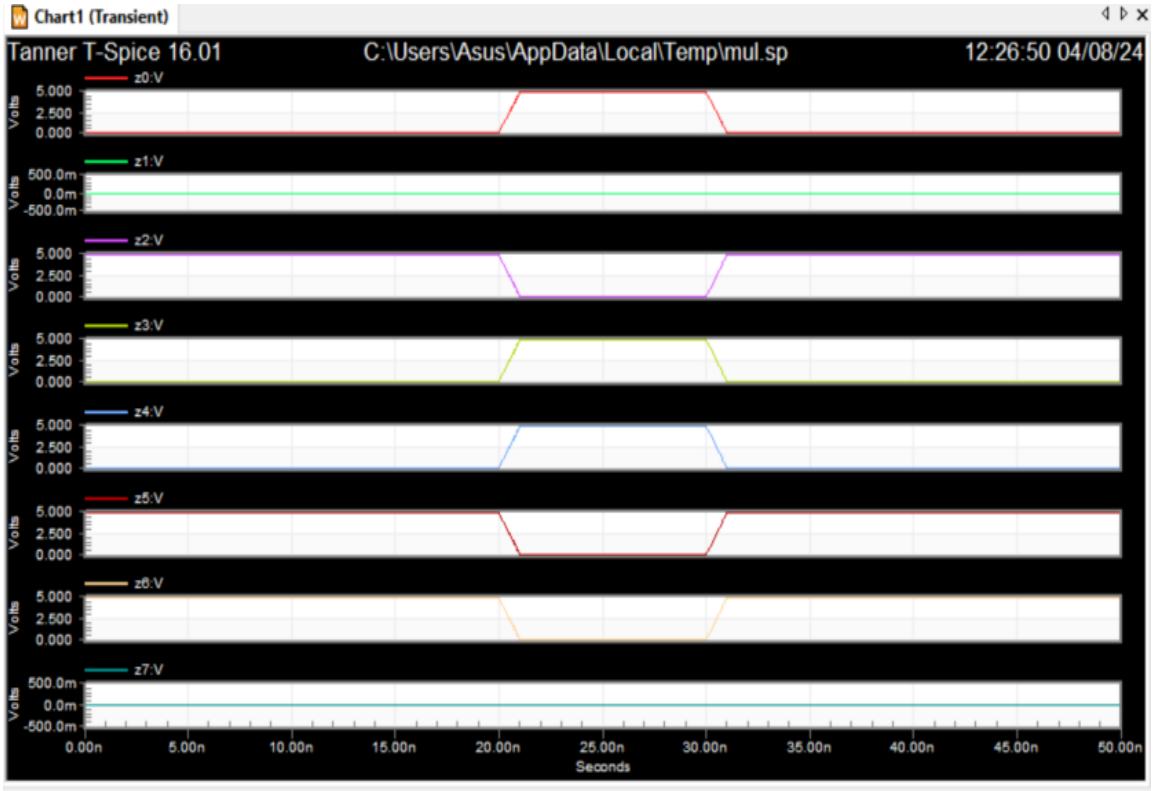

Fig13. 8-bit output of product term obtained 01100100

5. COMPARISIONS

Our proposed multiple results are thus compared to the CMOS 4-bit array Multiplier in terms of several parameters such as transmission clock frequency, supply voltage, and load capacitance.

5.1 Frequency Vs Power Dissipation:

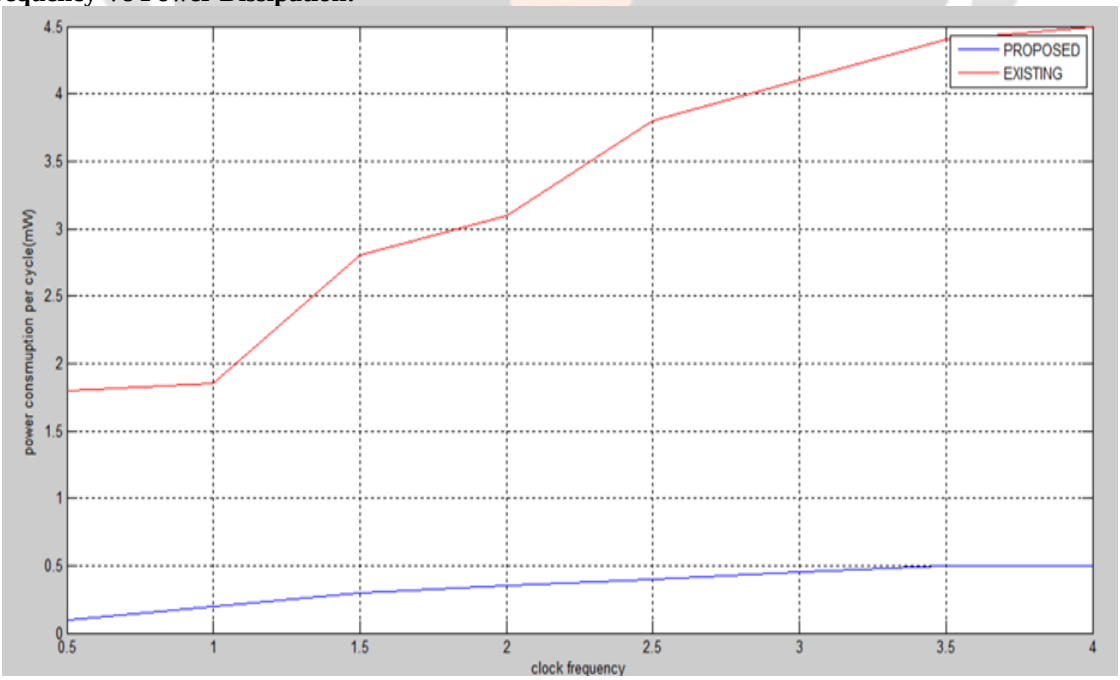

Fig-14. Representation of 4-bit array multiplier showing power dissipation with respect to frequency at VDD = 1.2 V and capacitance = 10 pf.

5.2 Supply Voltage Vs Power Dissipation:

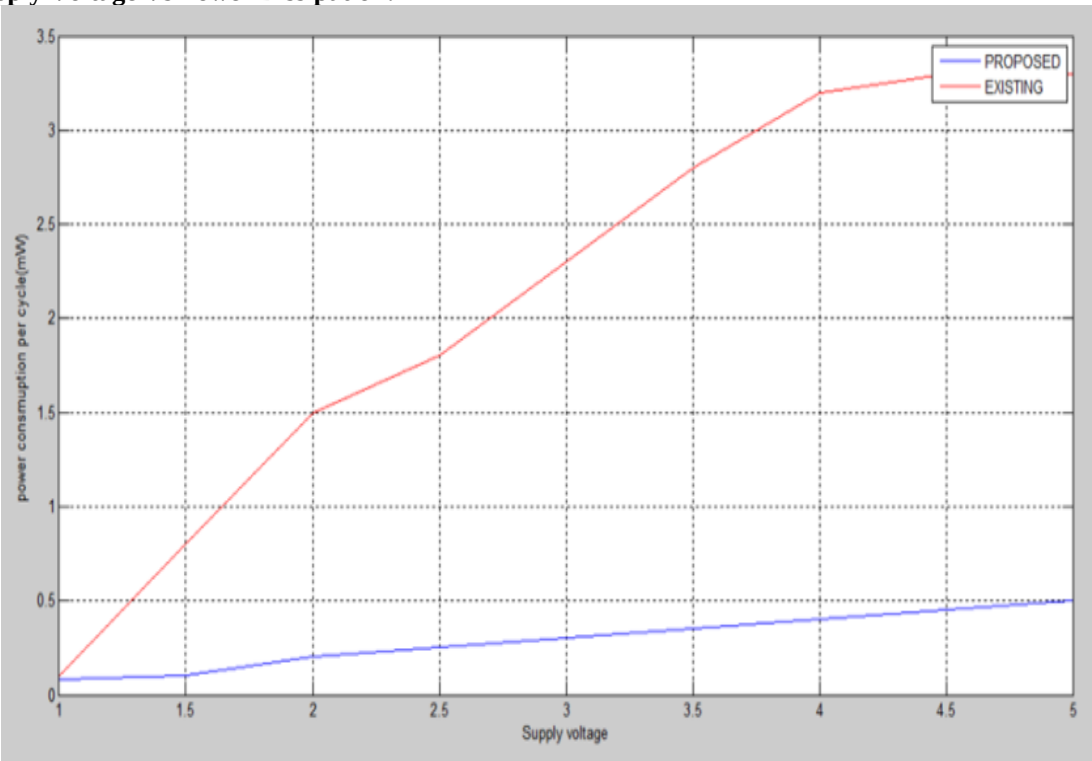

Fig-15. Representation of 4-bit array multiplier showing power dissipation with respect to Supply Voltage at Load capacitance = 10 pf and frequency = 4 GHz

5.3 Load Capacitance Vs Power Dissipation:

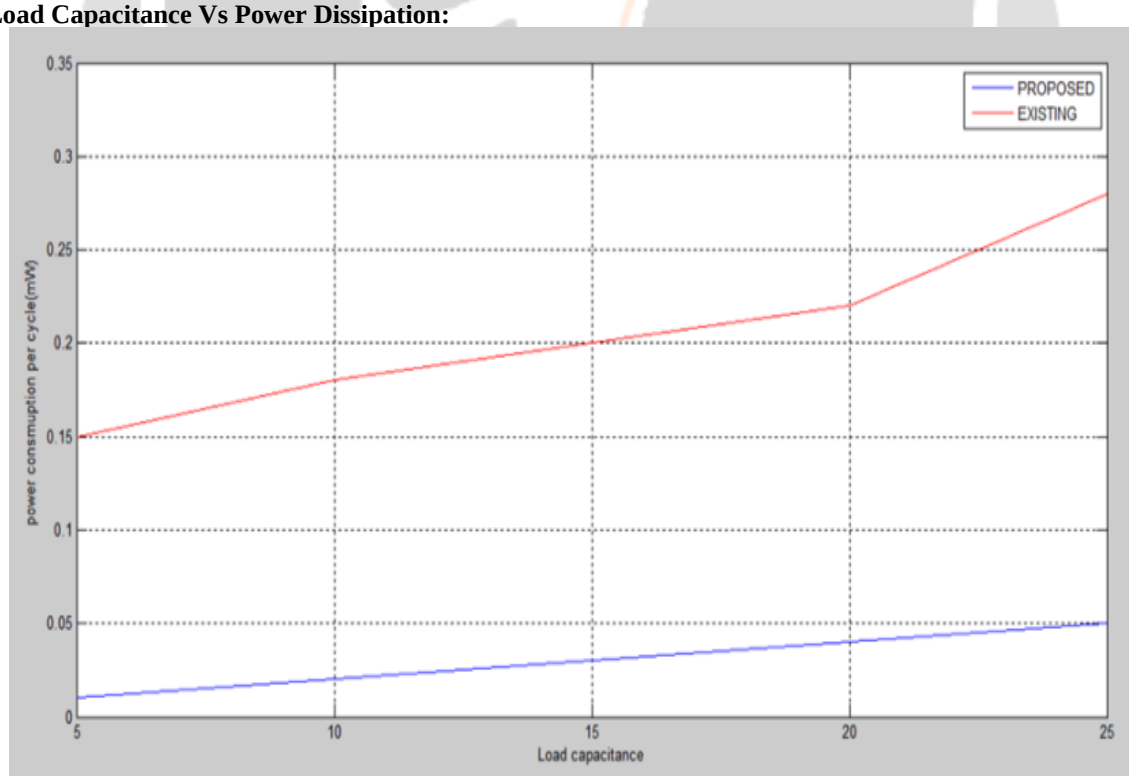

Fig-16. Representation of 4-bit array multiplier showing power dissipation with respect to load capacitance at VDD = 1.2 V and frequency = 4 GHz

Table -1. Observation of variation of power supply with respect to variation of frequency at Vdd = 1.2V and Cload = 10Pf

	Frequency	1 GHz	2 GHz	3 GHz	4 GHz
Proposed design	NTAL 4-Bit Array Multiplier	0.2 mW	0.35 mW	0.45 mW	0.5 mW
Ref. [10]	CMOS 4-Bit Array Multiplier	1.85 mW	3.1 mW	4.1 mW	4.5 mW

Table -2. Observation of variation of power supply with respect to variation of supply voltage at F = 4 GHz and Cload = 10Pf

	Supply Voltage	1 V	2 V	3 V	4 V	5 V
Proposed design	NTAL 4-Bit Array Multiplier	0.1 mW	0.2 mW	0.3 mW	0.4 mW	0.5 mW
Ref. [10]	CMOS 4-Bit Array Multiplier	0.1 mW	1.5 mW	2.3 mW	3.2 mW	3.3 mW

Table -3. Observation of variation of power supply with respect to variation of supply voltage at Vdd = 1.2V and F = 4 GHz

	Load capacitance	5 pF	10 pF	15 pF	20 pF	25 pF
Proposed design	NTAL 4-Bit Array Multiplier	0.0112 mW	0.0253 mW	0.0356 mW	0.0478 mW	0.0558 mW
Ref. [10]	CMOS 4-Bit Array Multiplier	0.153 mW	0.168 mW	0.213 mW	0.235 mW	0.285 mW

In terms of power dissipation, the NTAL design method outperforms the more typical CMOS design process for logic circuits, although it is more complex to execute. The AND gate, half adder, and full adder can be used to build a 4-bit array multiplier circuit (3p467890). The suggested circuit has a total power dissipation of 0.5 mW, which is significantly lower than a normal CMOS circuit (about 4.5 mW). This technology is suitable for applications where power dissipation is a major concern, as its performance is low. To prove this, comprehensive Tanner simulation is performed at 65 nm technology.

4. CONCLUSIONS

This research proposes and compares Near Threshold Adiabatic Logic (NTAL) technology to CMOS technology for the digital application circuit 4-bit array multiplier. After analyzing various adiabatic strategies, it was determined that the NTAL design method is most suited for digital signal solutions due to its low power execution. In terms of power dissipation, the NTAL design method outperforms the more typical CMOS design process for logic circuits, although it is more complex to execute. Scholasticate 3p467890 provides a 4-bit array multiplier circuit using an AND gate, half adder, and full adder. The suggested circuit has a total power dissipation of 0.5 mW, which is significantly lower than a normal CMOS circuit (about 4.5 mW). This approach is suitable for areas with high power dissipation, but its performance is limited. Extensive Tanner EDA simulation at 65 nm technology is used to prove this. This approach can also be applied to designing ALUs and processors for signal processing, communication, and wireless networking.

6. REFERENCES

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