Analysis and Design 10 bit of Current – Steering Digital to Analog Converter in CMOS Technology

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ABSTRACT

The pressure to reduce cost in mass market communication devices such as cable modems and digital set-top boxes has created a need for embedded high-speed high-resolution digital-to-Analog converters (DACs). This thesis discusses the different architectures of current- steering digital-to-Analog converter (CS-DAC). Reasons of selecting binary-weighted architecture are low complexity, small area and less power consumption in comparison of other architectures. 14-bit CS-DAC is implemented and performance parameters are checked.

Keyword : - *Binary Weighted, Thermometer, Segmented, Digital to Analog Conversion, Glitch;*

1. INTRODUCTION

The production of digital computing and signal processing in electronic systems is often described "The world is becoming more digital every day". Digital circuits exhibits lower sensitivity to noise and more robustness to supply and offer more extensive programmability as compare to Analog circuits. In order to interface digital processors with the Analog world, a high-speed and high-resolution Digital-to-Analog converter is needed.

The pressure to reduce cost in mass market communication devices such as cable modems and digital cable set-top boxes has created a need for embedded high-speed digital-to-Analog converters (DACs) and Analog-to-digital converters. DACs designed in CMOS technology are becoming more popular in high-speed communication, instrumentation and data acquisition system. For various applications such as video signal processing, audio signal processing, digital signal synthesis and both wired and wireless transmitters, high resolution display and high de nation television(HDTV), we need high speed and high resolution DACs. The current steering is a good applicant for this application. They are inherently faster and more linear because they can drive resistive load directly without the output voltage buffer.

1.1 Digital to Analog Interface

In signal processing systems, digital to Analog converters (DACs) are essential blocks. They are taken as the interfaces between the digital signal processors and the Analog world as shown in Figure 1. It should be noted that DACs can use either voltage or current as its Analog signal.

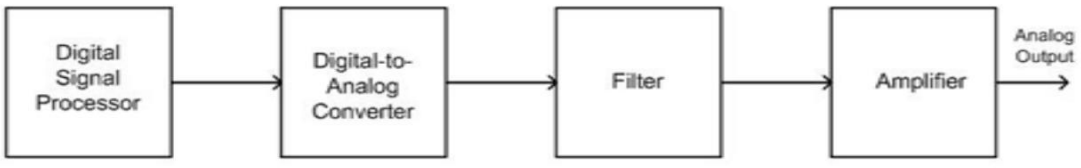

Fig 1Digital to Analog Interfaces

The function of DAC is to convert the digital input code to the continuous time Analog signal. The block diagram of transfer function of N-bit DAC is shown in Figure 2. The output of the DAC is a voltage that is some fraction of a reference voltage.

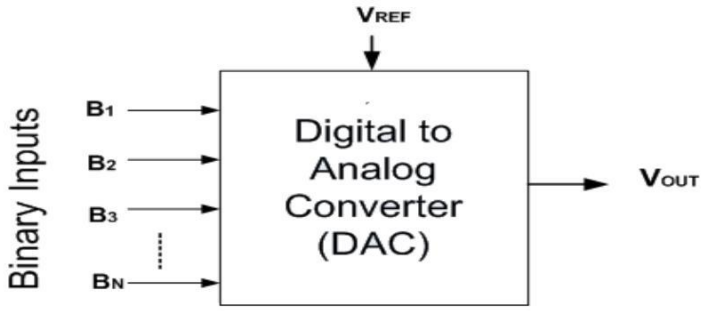

Fig 2 Block Diagram of a N – bit D/A Converter

Mathematically the output voltage V_{OUT} can be expressed by following formula:

$$V_{OUT} = V_{REF} \ (B_N 2^{-1} + B_{N-1} 2^{-2} + B_{N-2} 2^{-3} + \ldots \ldots + B_1 2^{-N})$$

Where, V_{REF} is reference voltage setting the output range of the DAC and the digital input words B_1, B_2 :::: B_N are the binary bits of either 0 or 1. The most significant bit (MSB) is BN and the least significant bit (LSB) is B1. Digital to Analog conversion can be regarded as a reference multiplication or division function.

2 CURRENT- STEERING ARCHITECTURES

Current steering architectures replicate a reference current source, the reference source is simply replicated in each branch of the DAC and each branch current is switched off or on based on the input code .In the binary version, the reference current is multiplied by power of 2^N, creating larger currents to represent higher magnitude digital signals. Current Steering DACs are low power and much faster compared to the other architectures such as resistor ladder or capacitor architectures because it does not require an output buffer.

The current steering architecture is suitable for high – speed and high resolution applications especially when special care is taken to improve the matching of the current sources. The basic principle of the -current steering DACs is to sum the current from the current sources according to the digital input. The current sources are connected parallel to each other. The current sources are connected to output node via MOS switches which are controlled by the input code. The output current of the DAC is proportional to the input code. To implement a high speed and high resolution current steering DAC we must pay more attention to choose a proper architecture which can achieve a reasonable power consumption, chip area and complexity with a balanced static and dynamic specifications. There are three different architectures in implementation of this array namely the binary, the thermometer code and the segmented architecture.

2.1 Binary Weighted Architecture

A Binary structure is the simplest one to realize a current steering D/A convertor. An N bit converter in shows in figure 3, N bit configuration which needs only N current sources. They are directly operated by the digital input codes and depending on the codes current flows either to the ground or to the output. This type of configuration is easy to implement and it is also better in term of area efficiency. However, this structure faces large glitch impulse because of the dynamic behavior and for improper synchronization of the switches. The advantage of this architecture is that it requires a relatively small area with a small number of transistors. This means that for an N-bit converter there are only N current sources and an equal amount of switches. One more advantage of this architecture is its simplicity.

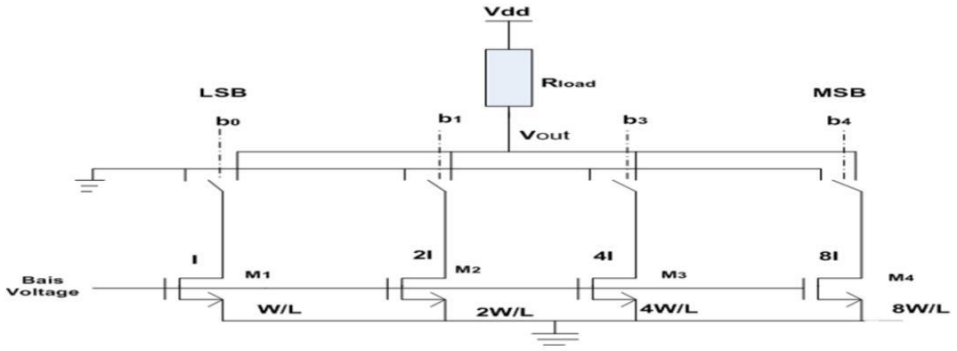

Fig 3 Binary Weighted DAC

2.2 Thermometer Architecture

Glitches are a major limitation in decoder and binary-weighted converters. When the digital input values changes, it is possible that some of the bit control signals may cause the switch controls to turn ON and/or OFF faster than other bits resulting in glitches in the Analog output signal values. In particular, if the MSB changes its value faster or slower than all other bits, it is possible to have glitches of almost half of V_{REF} . This problem can be alleviated by the use of thermometer code type of representation of the binary numbers. Although this coding scheme can result in potentially more circuit complexity, it has many advantages such as guaranteed monotonicity.

In thermometer code, when the transition is 0 to1 once it will remain ON through whole procedure. When the digital input increases by 1LSB, one additional current source is turned ON. Each current branch produces an equal amount of current thus for N bit converter, 2^N-1 current sources and switches are required which results in a larger area.

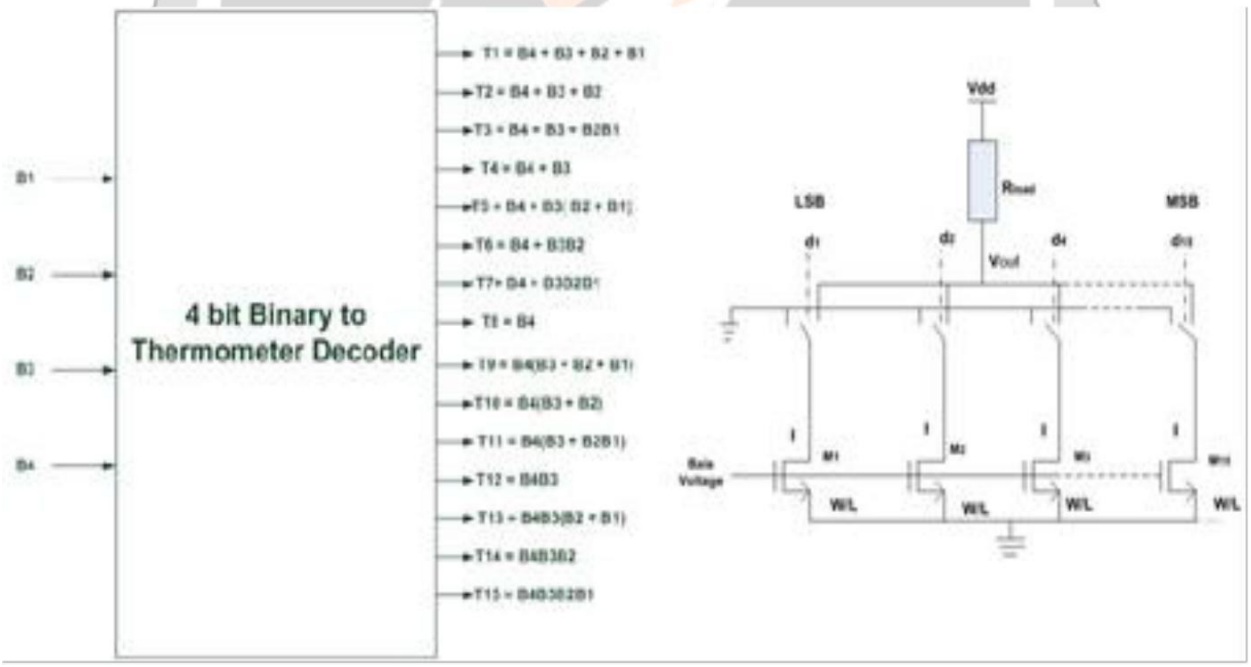

Fig 4 Thermometer weighted Current – Steering D/A converter

But it is having drawback of larger area than binary weighted architecture.

The advantage of this structure is that they provide guaranteed monotonicity, as a result the dynamic switching error gets reduced. No issue of imperfect synchronization occurs among switches and hence the glitch is also gets reduced significantly. The disadvantage of the thermometer coded approach is complex decoding logic, the large area requirement and high power consumption.

2.3 Segmented Architecture

The DAC is combined into two sub DACs one for most significant bits and the other for least significant bits. Thermometer coded gives minimum glitch and the binary weighted DACs using less area, so combination of both coding is called segmented coding. The full Binary weighted design means 0% segmentation and the full Thermometer code design means 100% segmentation. The Segmented DAC, which combines the thermometer-coded principle for the most significant bits and the binary-weighted principle for the least significant bits.

Partially segmented structure provides a good balance among power, area, and design complexity and as whole between static and dynamic performance of a DAC. The performance and area of the segmented DAC largely depends on the percentage of segmentation. Use of more number of bits in MSB unary DAC gives more linear results but the area is increased. On the other hand increasing the number of the bits in the LSB binary block decreases the total area but at the same time the performance is degraded.

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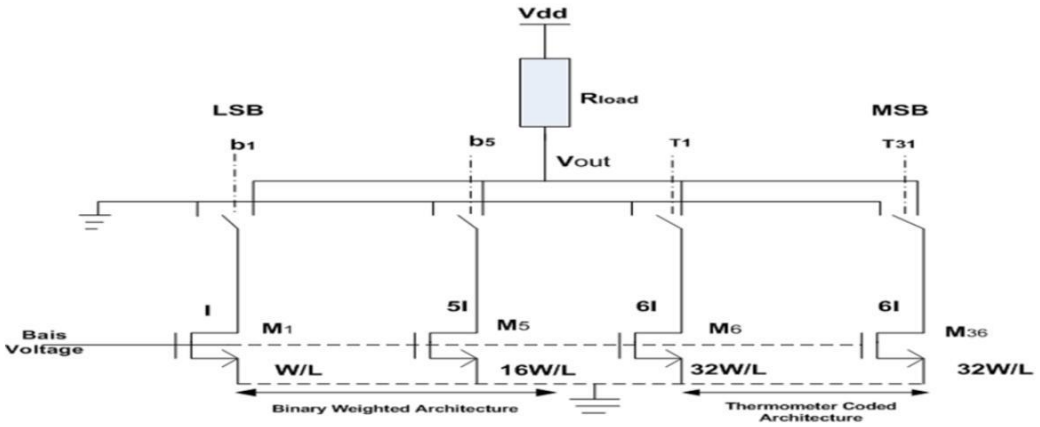

Fig 5 Segmented Architecture

For a given INL and DNL requirement, optimum segmentation for 10 bit DAC and are shown in figure 6. In a figure a fully binary weighted design is referred as 0% segmented whereas a fully thermometer design is referred to as 100% segmented. In figure 6 Line 4 represents the logarithmic area requirements for a DNL of 0.5 LSB as a function of segmentation. INL behavior is independent of segmentation and depends only on analog area. Line 2 represents the area requirement for INL of 1.0 LSB. Line 5 represents the digital area requirement as a function of segmentation. These three effects are put together in line 6 and are in bold curve. Line 6 represents the variation in total required area with segmentation foe an INL of 1.0 LSB and a DNL of 0.5 LSB. Any point on horizontal portion of line 6 can be taken for segmentation having minimum area. But if go beyond the corner optimum point, digital area gets increase. Therefore, optimum point represents the optimum segmentation, limited by the INL and DNL requirements For minimum area, the optimum value of segmentation calculated from graph is nearly between 60%-70%. So for 10 bit DAC the optimum segmentation is 6+4 and 7+3 to achieve optimum performance in terms of minimum area fixed INL and DNL.

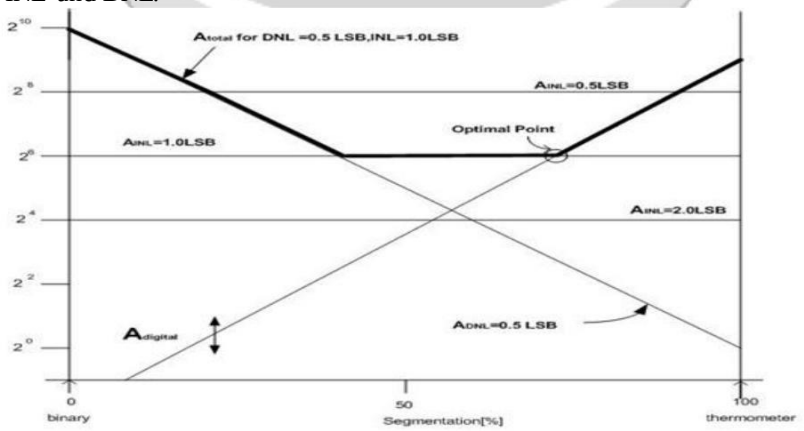

Fig 6 Normalized required area versus percentage of segmentation

3 DESIGN AND OPERATION OF CSDAC

The basic unit current cell consists of a single MOS transistor as a current source and two switching transistors. The switching transistors are directly exposed to the output terminal of the DAC i.e. the global output node where such a 2^N - 1current cells are connected. Hence this circuit topology is mainly subjected to errors which are voltage fluctuation of the output node of the current source due to improper timing of the switching OFF and ON of the switching transistor and charge feed through into the output terminal. The voltage at the output node of the current source should be constant. In reality, the switching causes a significant voltage variation. The cascade configuration is used to isolated the current transistor from the voltage fluctuation. The regulated cascode current mirror circuit is used as reference current source during the calibration period. Using the same bias current source, to basic reference current cells to control the mismatch between them.

Mmsc is main current source, I_b is current source which is 10 A. Msw's are two switching transistors and Mcs is a current source transistor, these are the main part of current steering DAC which is known as basic unit cell. For designing 10-bit current steering DAC the single cell is repeated 9 times. As we know voltage at the output node of the current source should be constant, but in reality it is not. Mco, Mpr and Mrc are regulated cascode transistors, is used to control the mismatch, and to isolate the current source transistor from voltage fluctuation. Sizing of the Mco and Mrc is different. Mmsc(W/L)=(10/1)µm

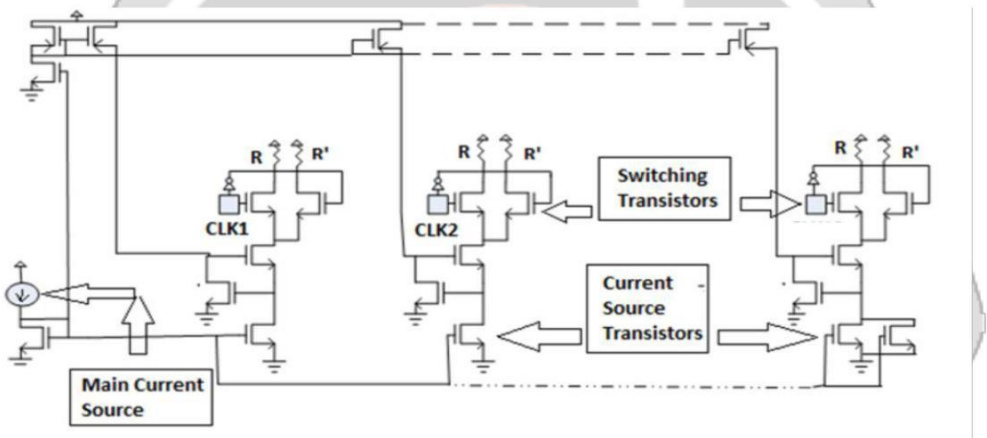

Fig 7 Design of Binary Weighted CS – DAC

Table 1 Sizing of Transistor

No. of Bit	Msw(W/L)	Mco(W/L)	Mcs(W/L)	Mpr(W/L)
1 – Bit	0.3/0.2	0.6/0.2	2.5/1	1.2/1
2 – Bit	0.3/0.2	1.2/0.2	5/1	2.5/1
3 – Bit	0.5/0.2	2.4/0.2	10/1	5/1
4 – Bit	1/0.2	4.8/0.2	20/1	10/1
5 – Bit	2/0.2	8/0.2	40/1	20/1
6 - Bit	4/0.2	16/0.2	80/1	40/1
7 – Bit	8/0.2	32/0.2	160/1	80/1
8 – Bit	16/0.2	64/0.2	320/1	160/1
9 – Bit	32/0.2	128/0.2	640/1	320/1
10 - Bit	64/0.2	256/0.2	1280/1	640/1

Calculation of R

$V_{OUT} = V_{DD} - IR$

$V_{OUT} = I_{LSB} * (2^N - 1) - IR$

$1.5 = (2.5\ \mu A) * (2^{10} - 1)\ R$

So, from the above equation we get the value R that is 0.587KΩ.

4 SIMULATION RESULT OF 10 BIT BINARY WEIGHTED DA

This section shows simulation results of 10 bit binary-weighted CS-DAC for two different cases. In one case DAC is implemented with ideal condition when no error is considered. Performance parameters are checked that are DNL and INL that are obtained from transient response. In other case according to polegram model error is introduced and transient response is taken and DNL and INL is obtained from transient response. Three different 10 bit segmented architectures are implemented and INL DNL and glitch energy of them is compared to each other and with INL, DNL and glitch energy of 10 bit binary weighted architecture.

4.1 10 bit Binary Weighted CS-DAC for Ideal case

This section includes transient response for ideal case when no error is taken in consider. Transient response is obtain to check the continues analog output of digital input and graphs that shows differential and integral nonlinearity obtain from the transient response.

4.1.1 Transient Response

Figure 8 shows the transient response of 10-bit CS-DAC for ideal case when no error is considered. Transient response is taken to measure the output voltage of all different combinations of input bits that is from 0000000000 to 1111111111. Y-axis denotes the output voltage and X-axis shows time (µs).

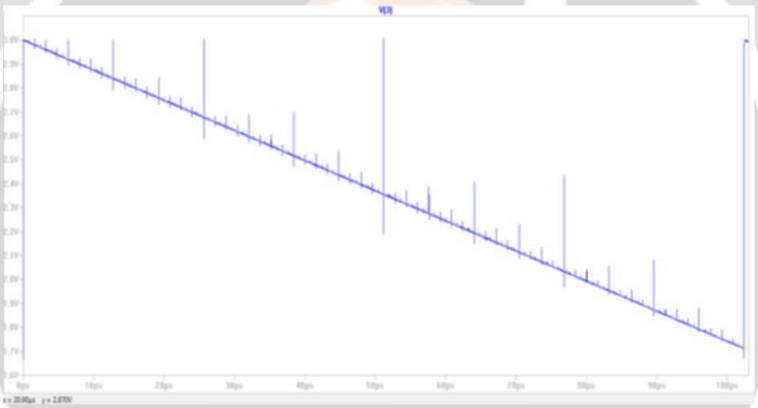

Fig 8 Transient response

4.1.2 Differential Nonlinearity and Integral Nonlinearity

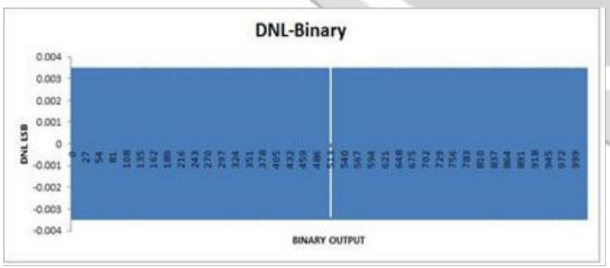

Fig 9 Differential Nonlinearity

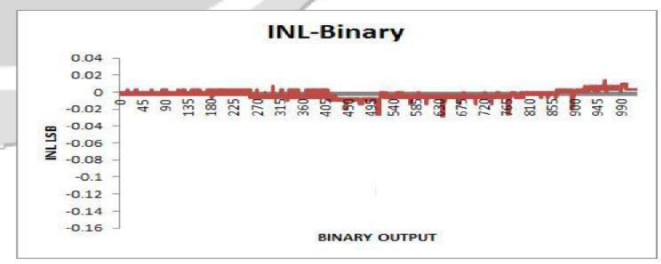

Fig 10 Integral Nonlinearity

4.2 5+5 Segmented Architecture of CS-DAC

Segmented architecture is designed using the combination of binary weighted architecture and thermometer coded architecture. LSB bits are designed using binary weighted architecture so for this combination 5 current source transistors are required. MSB bits are designed using thermometer architecture so for this combination 2^5-1 that is 31 current source transistors is required.

4.2.1 Transient Response

Figure 11 shows the transient response of 5+5 segmented architecture. Where 5 LSB bits are designed using Binary Weighted architecture and 5 MSB bits are designed using Thermometer Code architecture. X-axis shows time (µs) and Y-axis shows voltage.

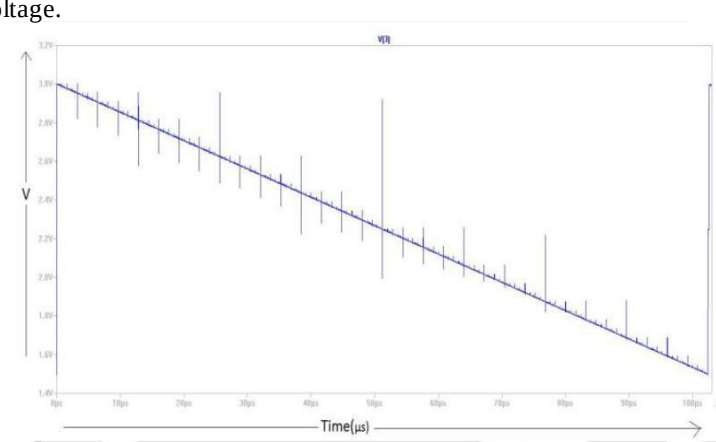

Fig 11 Transient Response of 5+5 segmented architecture

4.2.2 Differential Nonlinearity and Integral Nonlinearity

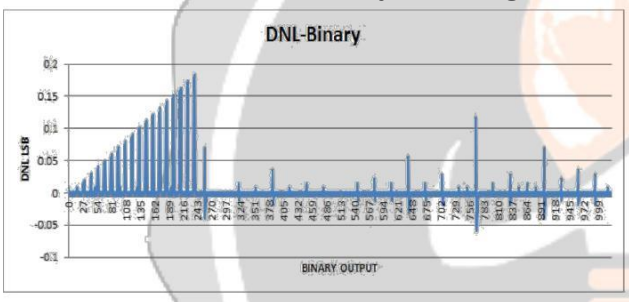

Fig 12 DNL

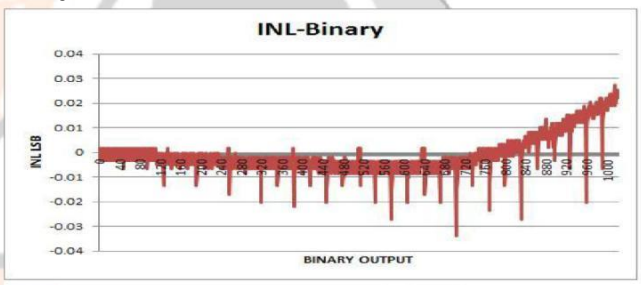

Fig 13 INL

4.3 6+4 Segmented Architecture of CS-DAC

Here LSB bits are designed using binary weighted architecture so for this combination 4 cur-rent source transistors are required. MSB bits are designed using thermometer architecture so for this combination 2^6-1 that is 63 current source transistors is required.

4.3.1 Transient Response

Figure 14 shows the transient response of 6+4 segmented architecture. Where 4 LSB bits are designed using Binary Weighted architecture and 6 MSB bits are designed using Thermometer Code architecture. X-axis shows time (µs) and Y-axis shows voltage.

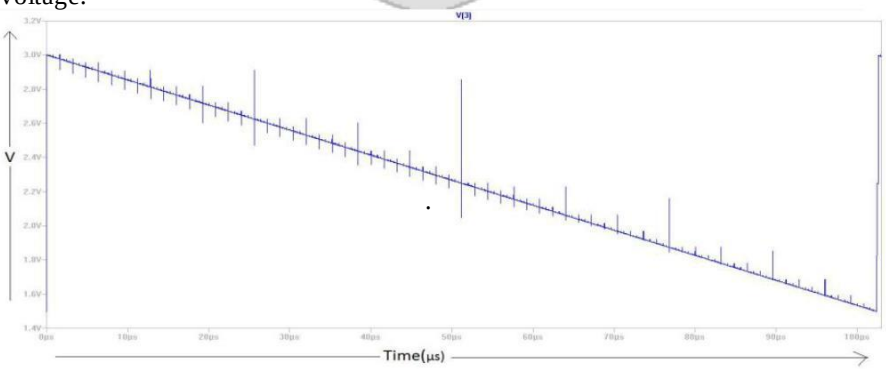

Fig 14 Transient Response of 6+4 segmented architecture

4.3.2 Differential Nonlinearity and Integral Nonlinearity

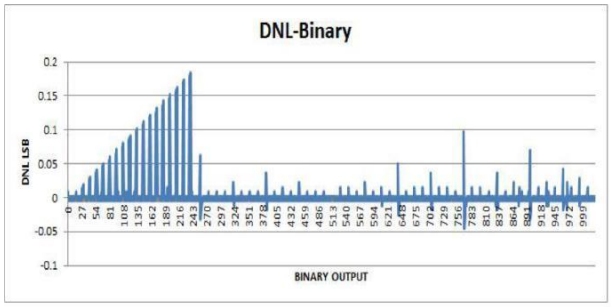

Fig 15 DNL

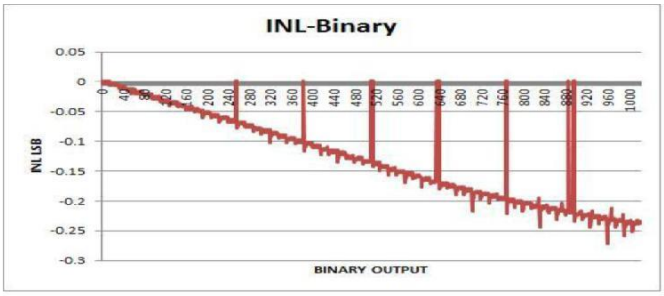

Fig 16 INL

4.4 7+3 Segmented Architecture of CS - DAC

In this architecture LSB bits are designed using binary weighted architecture so for this combination 3 current source transistors are required. MSB bits are designed using thermometer architecture so for this combination 2^7-1 that is 127 current source transistors are required. For this architecture binary to thermometer decoder will have the largest area.

4.4.1 Transient Response

Figure 17 shows the transient response of 7+3 segmented architecture. Where 3 LSB bits are designed using Binary Weighted architecture and 7 MSB bits are designed using Thermometer Code architecture. X-axis shows time(s) and Y-axis shows voltage.

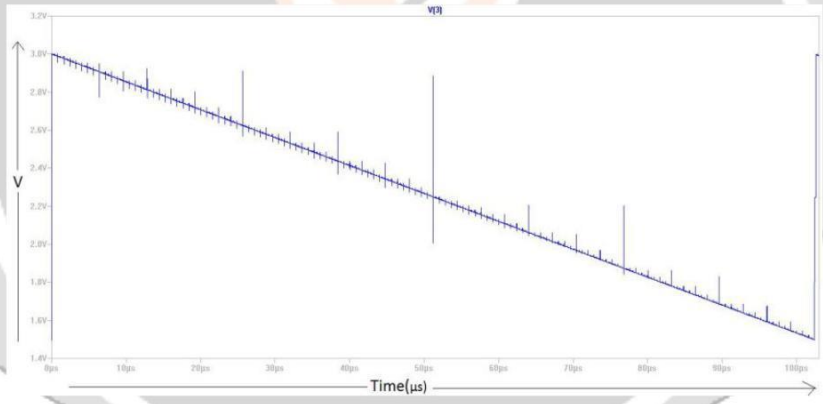

Fig 17 Transient Response of 7+3 Segmented

Architecture 4.4.2 Differential Nonlinearity and Integral Nonlinearity

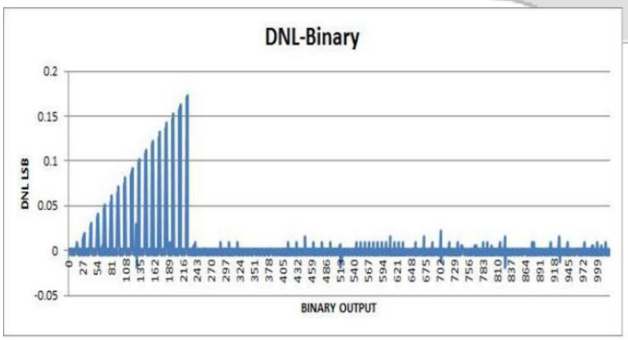

Fig 18 DNL

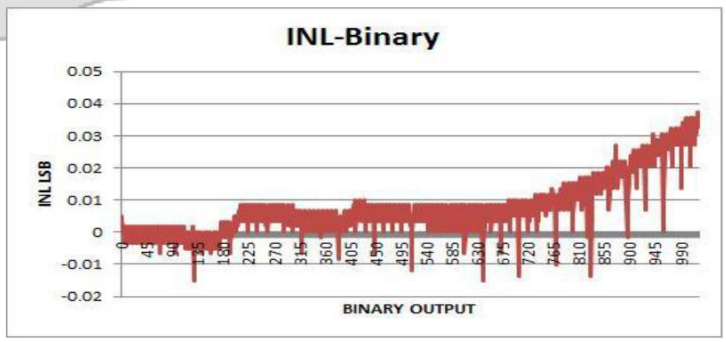

Fig 19 INL

Table 2 Comparison of 10 bit Architecture of CS-DAC

Parameters	Binary Weighted	Segmented			Reference		
		5+5	6+4	7+3	2015[1] (5+5)	2005[12] (6+4)	2010[7] (7+3)
INL(LSB)	0.003	0.03	0.24	0.03	0.44	0.4	0.3
DNL(LSB)	0.02	0.2	0.176	0.166	0.248	0.55	0.15
Glitch Energy (pVs)	632.48	457.98	270.67	120.05	-	-	-
Power (mW)	7.67	7.673	7.675	7.68	17.85	27.6525	49.5

Table 7.1 Comparison of 10 bit Architecture of CS-DAC

5. CONCLUSIONS

10 bit Binary weighted architecture is designed and it achieves DNL and INL for ideal condition of 0.003 LSB and 0.02LSB respectively. Designed three different segmented architectures of 10 bit CS-DAC that are 5+5 architecture, 6+4 architecture and 7+3 architecture. According to simulation results, optimum point of segmentation should be 60%-70% to improve performance parameters. Performance parameters of designed binary weighted and segmented architectures are found appropriate (compatible) when they are compared to references.

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