ANALYSIS OF MCML INVERTER

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ABSTRACT

The recent trend in the VLSI industry toward miniature designs, low power consumption, and increased growth of portable applications compels researchers to design circuit having high speed. MOS current-mode logic (MCML) technology is increasing because of its ability to dissipate less power, decrease in delay and so decrease in overall power delay product and used for high speed application than conventional CMOS techniques at high frequencies and high switching speed than Schmitt trigger, while providing an analog friendly and mixed signal environment.

It provides designers with an insight to the different tradeoffs involved in the design of MCML circuits to efficiently and systematically design MCML circuits. Circuit is implemented in 32nm MOS technology using HSPICE. The result illustrates that total delay improvement is achieved by using proposed system which helps the circuit to operate at high speed. This paper presents the analysis of design parameters of MCML inverters, which exhibits decrease in delay compared to CMOS and Schmitt trigger inverter circuits and compare them. It also discusses delay and power trade-offs associated with them.

Keyword : - *CMOS (Complementary Metal-Oxide Semiconductor), MCML (MOS Current Mode Logic), TPD (Total propagation delay), PDP (Power Delay Product), EDP (Energy Delay Product),VLSI(Very Large Scale Integration),tpdf(fall time propagation delay),tpdr(rise time propagation delay),C_L(load capacitor), HP(High Performance), LP(Low Power), PTM(Predictive Technology Model).*

1. INTRODUCTION

With the rapid increase in transmission speeds of communication systems, the demand for very high-speed low-power VLSI circuits ever increasing. Even though performance of CMOS technologies improves notably with scaling, conventional CMOS circuits cannot simultaneously satisfy the speed and power requirements of these applications. Moreover, conventional CMOS circuits generate significant supply noise, thus hindering the on-chip integration of sensitive analog and digital circuits[2].

MOS current mode logic (MCML) is a popular logic style for high-speed circuits. This type of logic was first implemented in bipolar technology and extended for application with MOS transistors. This logic style is promising for both reducing power consumption with the scaling of input voltage and for high Speed and providing an analog friendly environment. In addition to this its robustness further attracts to increase this style in high speed applications. This circuit conducts a very low tail current with the production of huge output swing. It has numerous advantages over conventional CMOS. MCML is widely used in high-speed applications, e.g., optical communication transceivers. MCML circuits are characterized by their low supply noise generation and high noise immunity, thus enabling the integration of analog and digital blocks on the same chip.

1.1 Overview Of MCML Inverter

MCML is MOS Current-Mode Logic (MCML) is an alternative logic designing style that provides true differential operation, low noise level generation and noise immunity. Which consists of three main parts: 1) the current source , 2) the differential pull-down network(PDN), 3) the load resistor (R), which can be implemented using resistors or active PMOS loads. MCML circuit depend on a current steering approach, Its PDN consists of source coupled NMOS transistor pairs. The constant current source generates the bias current I_{bias} while the load resistance R_L determines the output swing.

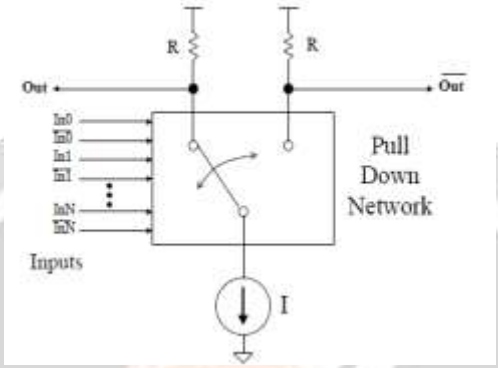

Fig.1. MCML Inverter

The optimum design of MCML gates involves minimizing a chosen quality metric such as energy-delay product or power-delay product. Since the delay of an MCML gate depends on the voltage swing ΔV and the bias current I_B[3]**.** The high output voltage is V_{DD}, while the low output is given by V_{DD}-ΔV, where ΔV is the voltage drop across R. Hence, MCML circuit experience a reduced voltage swing of ΔV. MCML circuits are characterized by: 1) high switching speeds, because of the reduced voltage swing. 2) constant power dissipation, because of the use of a constant current source. And 3) high noise immunity, because of the differential structure[1].

1.2 Overview of CMOS Inverter

In CMOS inverter, both p and n channel transistors are used. The circuit is fabricated on n type silicon substrate in which a p type well or tub is created by diffusion. The n channel transistor is created in the p well region. The p channel is made in the n substrate under an ion implanted layer called the p^+ layer. Similar to the depletion mode implantation is used for nMOS. When V_{in} (A) is equal to VDD, which is a logic 1, PMOS transistor is cut-off, and we can consider the n MOS transistor as a resistor, as it operates in the linear or triode region. When V_{in} is linked to ground, which is a logic 0, NMOS transistor is cut-off, and the PMOS transistor is operating in the triode region[4].

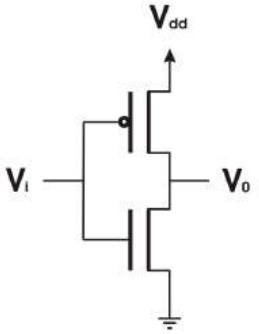

Fig.2. CMOS Inverter

1.3 Overview of Schmitt Trigger Inverter

In Schmitt trigger noise is being ignored by CMOS Schmitt Trigger inverter as the hysteresis offers a better noise margin and noise stable operation. It is designed by using less transistor count and a capacitor which results in less average power consumption with decrease in area. Delay is also decreased by using only one PMOS as because delay is more concentrated to PMOS due to less mobility of PMOS compare to NMOS. Transistors P1, P2, P3, N1, N2, and N3 in Figure are the I/O devices with the normal operation voltage of VDD. If the board voltage is equal to VDD, the gate-drain and gate-source voltages of transistors P1, P2, P3, N1, N2, and N3 in Figure will not exceed VDD. Thus, this circuit can be operated without suffering high-voltage gate-oxide overstress.[6]

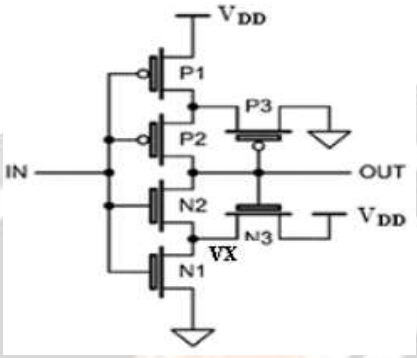

Fig.3. Schmitt Trigger

2. ANALYSIS AND DESIGN PARAMETERS

2.1 Analysis Of MCML Inverter

- Tpd (Total propagation delay) :- Measure the speed of output reaction to the input change.

$$tpd = \frac{(tpdr + tpdf)}{2}$$

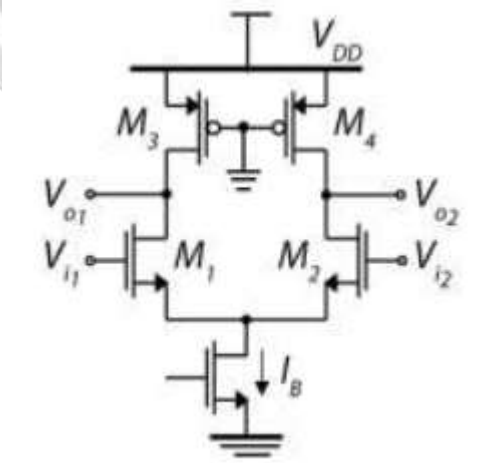

Fig.4. MCML Inverter

- PDP (Power Delay Product):- The PDP is the tool to assess overall performance of digital circuits and average

energy consumed per switching event.

$PDP = N^2 * C_L * \Delta V * V_{DD}$ …....[5]

• EDP(Energy Delay Product): It is the average energy consumed multiplied by the computation time required.

$$EDP = \frac{N^3 * CL^2 * \Delta V^2 * V_{DD}}{I} \quad \ldots\ldots [5]$$

2.2 Analysis of CMOS Inverter

• Tpd (Total propagation delay) :Measure the speed of output reaction to the input change.

tpd = (tpdr + tpdf)/2

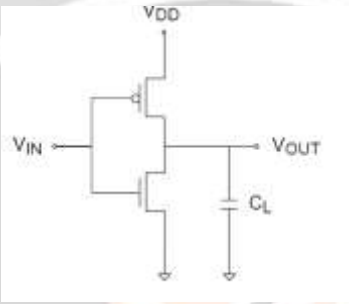

Fig.5. CMOS Inverter

• PDP(Power Delay Product) :- A power delay product is a fundamental parameter which is often used for measuring the quality and the performance of a CMOS process and gate design. As a physical quantity, the PDP can be interpreted as the average energy required for a gate to switch its output voltage from low to high and from high to low[4].

$PDP = C_{Load}.V_{DD}^2$

• EDP (Energy Delay Product): Note that calculating PDP with the generic definition of P_{avg} may result in a misleading interpretation that the amount of energy required per switching event is a function of the operating frequency. Thus the design engineers often use (EDP) for performance comparison, which is given by ;

$$EDP = (N^2.C_L^2.V_{DD}^2)/(\frac{\beta}{2}(V_{DD} - V_t^2) \quad \ldots [4]$$

3. RESULTS

All the simulations for analysis of various design parameters using Static CMOS, MCML and Schmitt trigger inverters have been performed at supply voltage 700mV. It can be observed that gate voltage of transistor (current source implemented using transistor) of MCML is scaled, the delay also decreases which is contrary to that of static CMOS logic inverter. This also leads to a decrease in PDP as the input voltage is scaled down contrary to CMOS and Schmitt trigger inverter. Thus CMOS and Schmitt trigger inverter shows a drastic increase in delay with decrease in supply voltage, whereas in case of MCML inverter the average delay still decreases. Therefore the total delay of MCML inverter is much lesser than CMOS and Schmitt trigger. So MCML topology finds applications where high speed is our primary concern. Various performance measures like Tpd, PDP and EDP compared to both and their tradeoff is observed.

Table-1:Result analysis for PTM HP MCML, CMOS and Schmitt trigger inverters

Parameters	Tpd	PDP	EDP
MCML Inverter	6.51E-12	4.68E-16	3.05E-27
CMOS Inverter	2.09E-11	1.45E-17	3.04E-28
Schmitt trigger Inverter	6.84E-11	2.74E-16	1.88E-26

From the result we can see that at 32nm technology node, MCML inverter shows significant improvement in Tpd, PDP and EDP performance as compared to both.

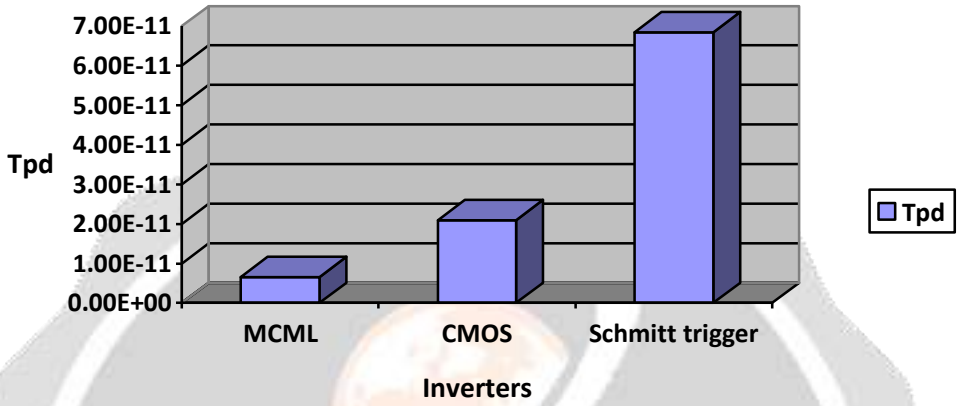

Chart -1(a): Tpd graph for MCML, CMOS and Schmitt trigger inverters.

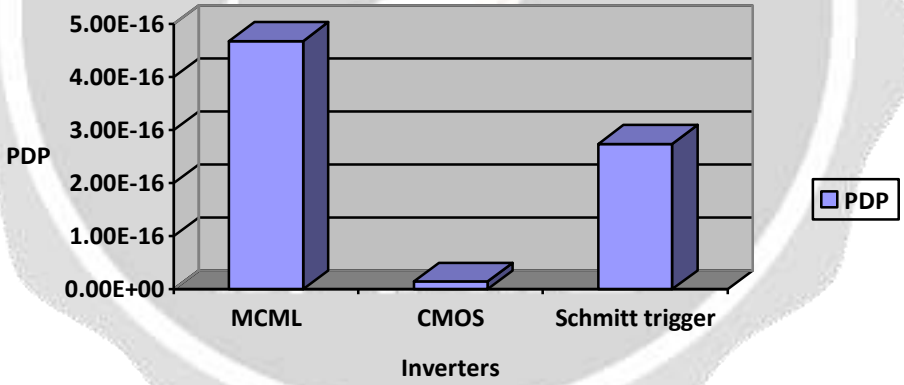

Chart -2(b): PDP graph for MCML, CMOS and Schmitt trigger inverters.

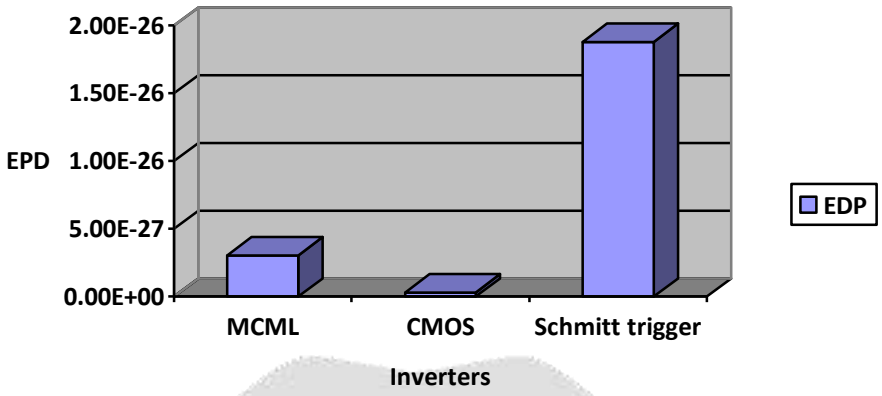

Chart -3(c): EDP graph for MCML, CMOS and Schmitt trigger inverters.

Table-2:Result analysis for PTM LP MCML, CMOS and Schmitt trigger inverters

Parameters	Tpd	PDP	EDP
MCML Inverter	5.85E-11	4.20E-16	2.46E-26
CMOS Inverter	9.81E-11	8.57E-17	8.41E-27
Schmitt trigger Inverter	5.66E-10	1.72E-15	9.76E-25

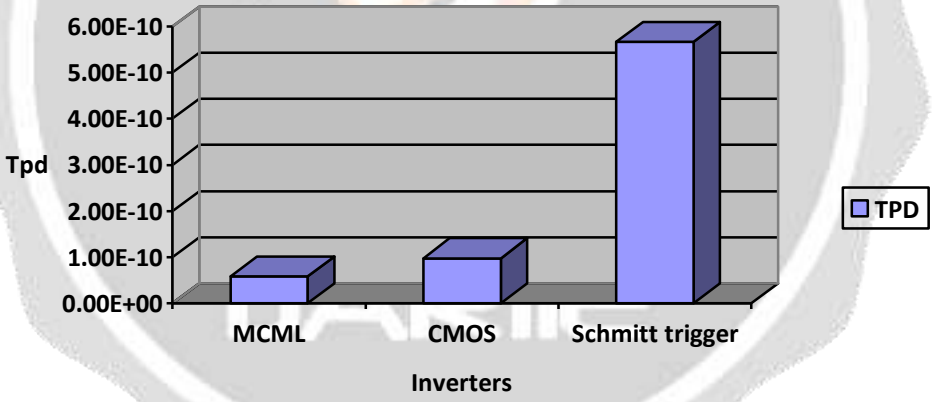

Chart -2(a): Tpd graph for MCML, CMOS and Schmitt trigger inverters.

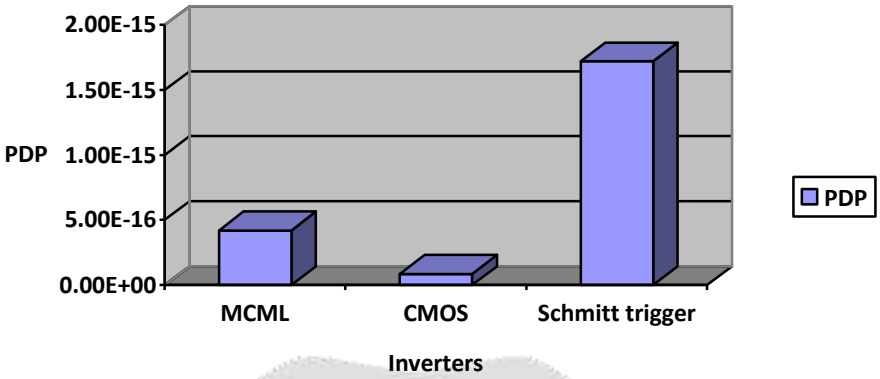

Chart -2(b): PDP graph for MCML, CMOS and Schmitt trigger inverters.

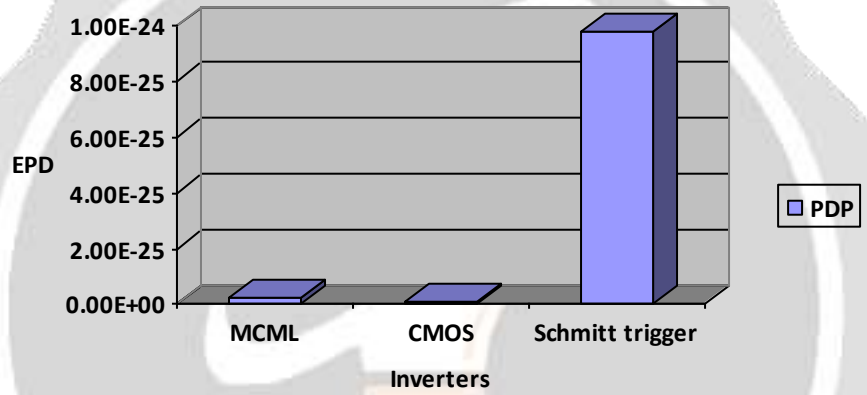

Chart -2(c): EDP graph for MCML, CMOS and Schmitt trigger inverters.

4. CONCLUSIONS

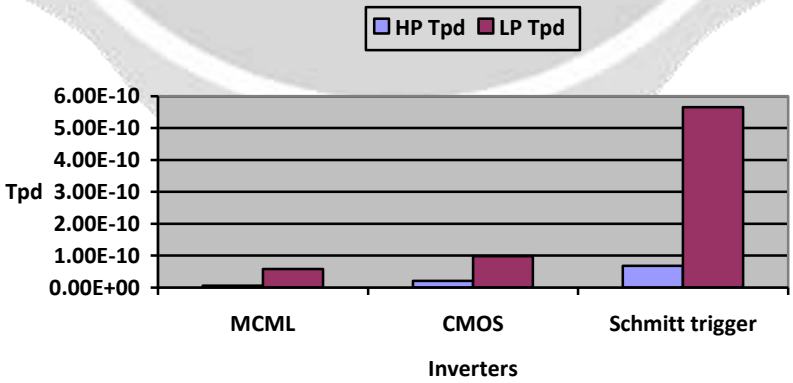

Chart -4(a): Tpd graph for HP and LP MCML, CMOS and Schmitt trigger inverters.

Above chart shows that HP inverters have much lesser delay than LP inverters, among which MCML inverter circuit has least delay as compared to that of the other inverters. Hence, MCML circuit is used for high speed applications.

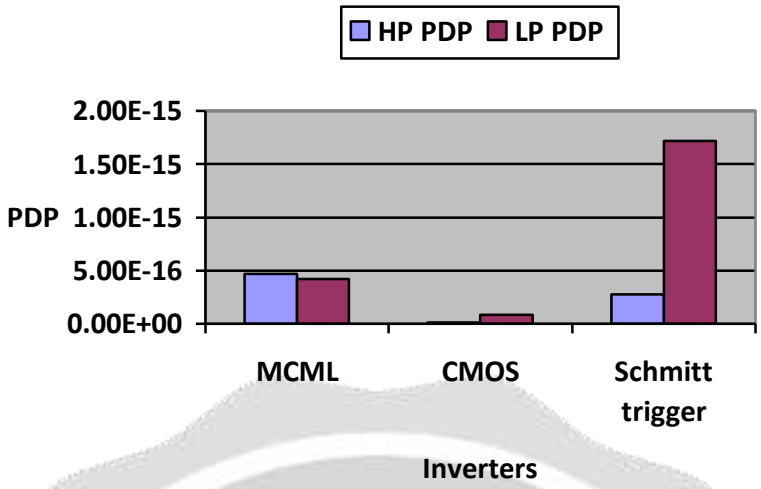

Chart -4(b): PDP graph for HP and LP MCML, CMOS and Schmitt trigger inverters.

In case of HP CMOS and Schmitt trigger inverters, power required is less than that of LP. Whereas in MCML circuit, power requirement is better in LP than in HP.

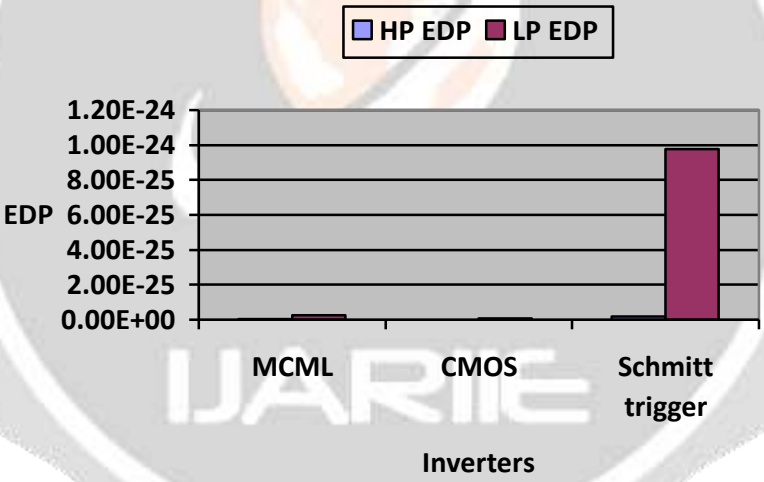

Chart -4(c): EDP graph for HP and LP MCML, CMOS and Schmitt trigger inverters.

Above chart shows that LP inverters have much larger EDP than HP inverters, among which Schmitt trigger inverter circuit has largest EDP as compared to that of the other inverters.

In this paper we described the performance parameters of MCML inverter along with CMOS and Schmitt Trigger inverters in HSPICE. It has been investigated that the delay in MCML inverter is very less as compared to that of CMOS and Schmitt trigger inverters, which helps to operate the MCML at high speed but with a bit increase in power. However, the MCML is a differential circuit which makes it robust in noise environment as compared to CMOS and Schmitt trigger inverter circuits due to current mode logic Hence there exhibits trade-off between power and delay in both HP and LP inverters.

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6. REFERENCES

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