DESIGE THREE CURRENT MIRROR OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Trang Le Thi Huyen[1], Anh Dang Thi Ngoc[1]

[1]Thai Nguyen University of Technology, Thai Nguyen city, Viet Nam

ABSTRACT

This article presents how to analyze and design an operational transconductance amplifier (OTA) circuit. The configuration chosen is three current mirror. The diagram-based design was used to find the DC bias conditions and the sizes. To demonstrate the proposed procedure, the schematic designed in 0.8 µm CMOS technology and simulated results compared the requirements. According to simulations, measurement results show good performance and proves the correctness of the proposed calculation steps.

Keyword: *OTA, Current mirror, Amplifier, IC design*

1. INTRODUCTION

The Operational Transconductance Amplifier (OTA) is an important circuit block in electronic circuits, used to convert voltage signals into current signals. It is also used in many applications in the telecommunications field, such as amplifiers, filters, and modulators. The Three Current Mirror configuration used to generate stable currents. It consists of three pairs of MOSFETs. This configuration has many advantages, including high stability, compact size, and stable perfomance.

The article is divided into 5 parts: (1) Introduction; (2) Design OTA; (3) Simulation results; (4) Conclusion; (5) Reference

2. DESIGE OTA

2.1 Schematic circuit

Three current mirror OTA uses three current mirrors as shown in Figure 1

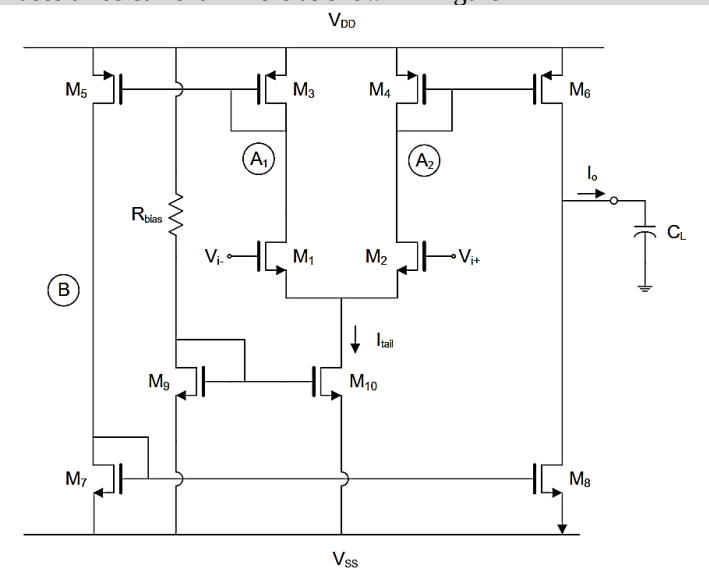

Fig - 1: Three current mirror OTA

Here, differential pair NMOS M1 and M2 is input differential amplifier. It is also the first stage of OTA. PMOS M3 and M6, M4 and M5, M9 and M10 pair are three current mirrors. M9 and M10 pair creates bias current for differential pair. Two pair rest are active load. The CS amplifier is second stage of OTA.

2.2 Design procedures

The table following is specifications of the OTA

Table -1: Specifications of the OTA

Specifications	Value
Gain	>40dB
Slew Rate	10V/μs
GB	>2MHz
Power (μW)	<10
ICMR+	2V
ICMR-	-1V
C_L	20pF

Model parameters for Mosfet using simple model based on 0.8μm process technology as follow:

Table -2: Model parameters for Mosfet

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		n-Channel	p-Channel	
V_{T0}	Threshold voltage ($V_{BS} = 0$)	0.7 ± 0.15	−0.7 ± 0.15	V
K'	Transconductance parameter (in saturation)	110.0 ± 10%	50.0 ± 10%	μA/V^2
γ	Bulk threshold parameter	0.4	0.57	V$^{1/2}$
λ	Channel length modulation parameter	0.04 (L = 1 μm) 0.01 (L = 2 μm)	0.05 (L = 1 μm) 0.01 (L = 2 μm)	V^{-1}
$2\|\phi_F\|$	Surface potential at strong inversion	0.7	0.8	V

Following are the suggested steps to design the circuit based on the given requirements.

Step 1: Find biased current from SR and C_L.

$$I_{10} = I_{TAIL} = SR \times C_L$$

Step 2: Detemind the size of M1 and M2

$$\left(\frac{W}{L}\right)_1 = \frac{g_{m1}^2}{2 \times K'_N \times I_1}$$

$$g_{m1} = GB \times C_L$$

$$I_1 = \frac{1}{2} I_{10}$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$

Step 3: Find size of M3 and M5 based on equation:

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_5 = \frac{I_{10}}{K'_P[V_{DD} - V_{in(\max)} - |V_{TO3}|_{\max} + V_{T1(\max)}]^2}$$

Step 4: Calculate size of M10 and M9 using:

$$\left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_{10} = \frac{2I_{10}}{K'_N\left[V_{DS10(sat)}\right]^2}$$

$$V_{DS10} = V_{in(\min)} - V_{SS} - \sqrt{\frac{I_{10}}{\beta_1}} - V_{T1(\max)}$$

Step 5: For M6, we rely on the gain of second stage which is easily determined by dividing the total gain by the gain of first stage. As follows:

$$A_{v1} = -\frac{g_{m1}}{g_{ds2} + g_{ds4}},\ A_{v2} = \frac{A_v}{A_{v1}}$$

$$\left(\frac{W}{L}\right)_6 = \frac{(A_{v2} I_{D6}(\lambda_N + \lambda_P))^2}{2K_p I_{D6}}$$

Step 6: Finally, find size of M7 and M8:

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_{10} \times \frac{I_6}{I_{10}}$$

Step 7: Check whether the power consumption is satisfactory or not

$$P_{diss} = (I_{10} + I_6 + I_5)(V_{DD} + |V_{SS}|)$$

Through step 1 to step 7 and the mosffet parameters in table 2, we have a table summarizing the size of the mosfetS:

Table -3: The size of mosfets

Transistor	Width(µm)	Length(µm)
M1 & M2	3	1
M3 & M5	100	1
M4 & M6	0.1	1
M7 & M8	107.5	1

M9 & M10	215	1

2.3 Simulation results

In this part, all results simulated on Pspice software will be presented after calculating the circuit parameters in previous part. Figure 2 is schematic circuit of OTA.

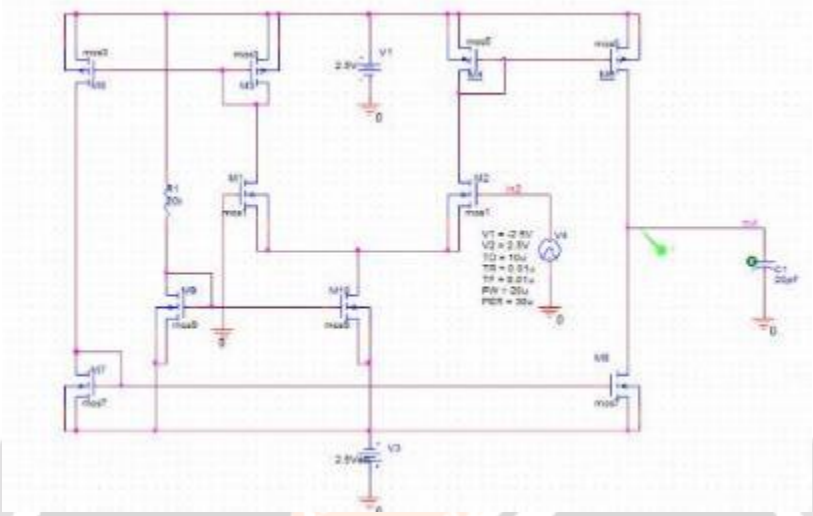

Fig - 2: Schematic of OTA

Transient response is shown in figure 3. Figure 4 is AC sweep response which show frequence response of the circuit. Mesuring Slew rate parameter is introduced in Figure 5 where input of circuit is square pulse.

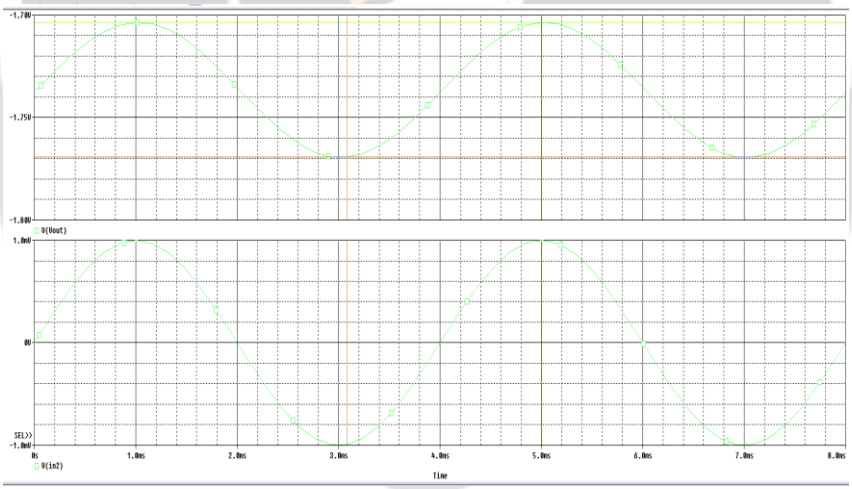

Fig - 3: Transient response of OTA

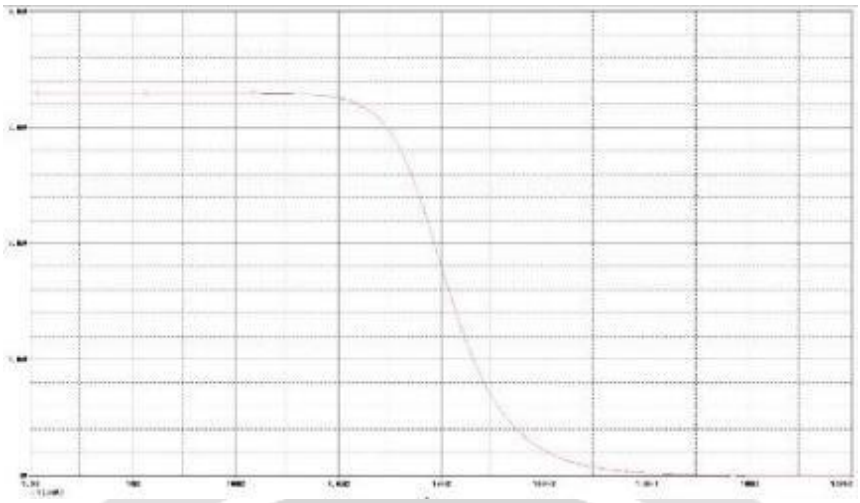

Fig - 4: Frequency response of OTA

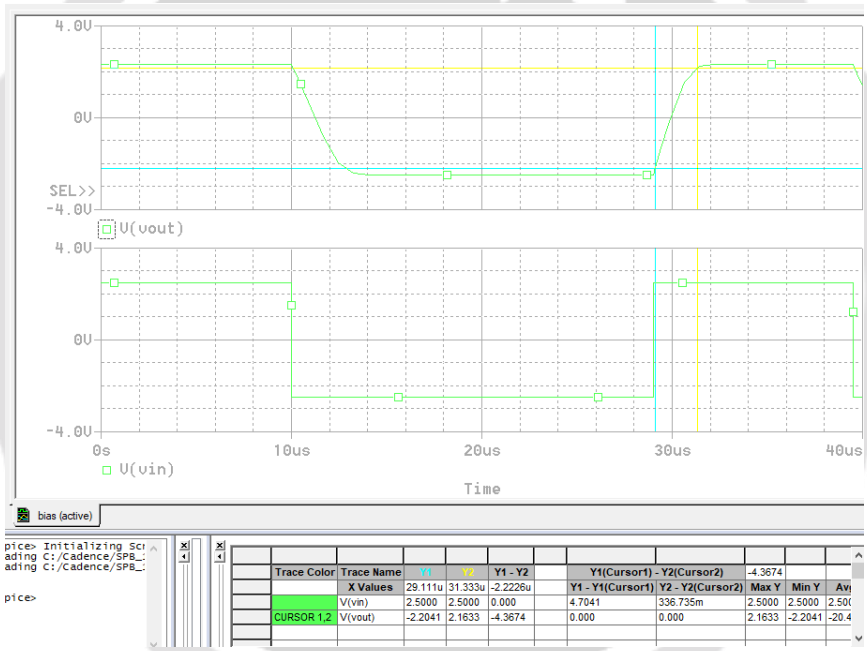

Fig - 5: Mesuring SR

Table 4 summarizes the main performance parameters compared to the itself value in given specifications:

Table -4: Summarizing OTA performance

Parameters	**Spec**	**Simulation results**
Av (V/V)	100	110
SR (V/**µ**S)	>10	18.14
GB (MHz)	>2	2.034 MHz
ICMR-	-1	-1
ICMR+	2	1.9

Simulation results show that the circuit meets the given requirements accurately. That shows the correctness of the proposed calculation steps.

3. CONCLUSIONS

This article introduces a simple method to design OTA circuits. From given specifications, the bias current and size of mosfets are detemined clearly. The simulation process is then conducted. Comparison between simulation results and requirements has shown that the initial design calculations are satisfactory.

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4. REFERENCES

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