DESIGN AND ANALYSIS OF FPGA BASED HIGH-RESOLUTION DIGITAL PULSE WIDTH MODULATORS TECHNIQUE FOR DC-DC CONVERTERS

Dr. K.Umadevi[1], Mr. R.Karthikeyan[2]
[1]*Head of Department EEE Sengunthar Engineering College,Tiruchengode,Tamilnadu,kindlyuma@gmail.com*

[2]*PG Scholar,ME-VLSIdesign,Sengunthar Engineering College,Tiruchengode,Tamilnadu thikar.dsn@gmail.com*

ABSTRACT

The Digital Pulse Width Modulation (DPWM) have become one basic building block in digital control architectures of any power converter.

The Digital pluse width modulation (DPWM) have become one basic buliding blosk in digital control architectures of any power converter. Hence it has become an integral part of all System on Chips.The Traditional Digital pulse width modulator implementation are based on counters and comparators which generate the power converter gating signals according to several predefined thresholds are based on counters and comparators which generate the power converter gating signals according to several predefined thresholds. For these designs, the minimum on-time step is equal to the counter clock period. DC-DC converters for proper system performance, by proposing differende design methods and control approach with growing tendency to using digital implementation over analog practices. Because of the rapid advancement in semiconductors and microprocessor industry, digital control grew in popularity among pulse width modulators converters and is taking over analog techniques due to the availability of fast speed microprocessors, flexibility, and immunity to noise and environmental variations. Furthermore, increased interest in Field Programmable Gate Arrays (FPGA) makes it a convenient design platform for digitally controlled converters. New digital control schemes, aiming to improve the steady-state and transient responses of a high switching frequency FPGA–based digitally controlled DC-DC converters. The target is to achieve enhanced performance in terms of tight regulation with minimum power consumption and high efficiency at steady–state, as well as shorter settling time with optimal over– and undershoots during transients. VHDL and Verilog are employed for the coding of the Digital Controller, synthesis has been done using Modelsim, and Behavioral and Timing simulation has been handled by ModelSim.

Keywords—*System on a chip, DC-DC Converters, Digital controller. Pulse-width modulation, Stability.*

I.INTRODUCTION

This research presents a new Digital Pulse Width Modulator (DPWM) architecture for Field Programmable Gate Array (FPGA) based systems. The design of the proposed Digital Pulse Width on counters and comparators which generate the power converter gating signals according to several predefined thresholds to overcome this problem, different solutions have been proposed depending Modulator architecture is based on fully utilizing the Digital Clock Manager (DCM) resources available on new FPGA boards. The Digital pulse width modulators (DPWM) have become one basic building block in digital control architectures of any power converter. Traditional DPWM implementations are based on whether the digital controller is implemented on a Digital Signal Processor (DSP), an Application Specific Integrated Circuit (ASIC), or a Field Programmable Gate Array (FPGA). In the case of DSPs, some of them incorporate High-Resolution pulse width modulators (HRPWM) peripherals. Modulators allowing a minimum time step that is a fraction of the system clock. Several FPGA-based solutions have also been proposed in the literature. One common The solution is to use a coarse resolution counter-based stage plus one or several on-chip Digital Clock Manager (DCM) blocks.

The Pulse Width Modulator signal is set at the beginning of the counter period, and it is reset after a given number of clock cycles plus a certain fraction of the clock period established by the Digital Clock Manager. Apart from, the circuits previously published for delaying the reset signal are not fully synchronous. The aim of this paper is to propose a fully synchronous high-resolution DPWM architecture in order to avoid the need of using excessively high clock frequencies, providing a more convenient final implementation. Our proposed architecture is a generalization of the circuit in and it can allow working the circuit at higher clock frequencies. The Digital Clock Manager is a clock management system that enables the following features: input clock frequency duplication, multiplication, and division in addition to generating. Through analysis and

examination of the Digital Clock Manager operation, it can be determined that, in order to take full advantage of the Digital Clock Manager modules, the same phase shifts are better utilized if generated with different ON–time/OFF–time relationship other than the corrected default duty cycle. Another attractive feature of Digital Clock Manager Blocks is the ability to cascade them; one Digital Clock Manager Module feeds the next to further increase the resolution while using available power–optimized FPGA resources.

The design of the proposed DPWM is basically a segmentation of the available power optimized Digital Clock Manager blocks to increase the effective resolution of the system. Furthermore, this architecture will also add a window–mask signal which limits the Digital Clock Manager operation to only a portion of the switching period in order to further decrease power dissipation. The digital modulator technique allows for higher Digital Pulse Width Modulator resolution with lower power consumption which was the primary barrier to high switching frequency operation.

The presented technique relies on power– optimized resources already existing on new FPGAs, and benefits from the phase shifting properties of the Digital Clock Manager blocks which help in simplifying the duty cycle generation. The output voltage of a DC-DC converter relies on the switching control circuit which is fundamentally an FPGA Digital controller-PWM. The architecture can be applied to achieve different numbers of bits for the Digital Pulse Width Modulator resolution designed for different DC-DC applications, by determining how many Digital Clock Manager Modules will be cascaded in the design. The proposed architecture shifts the ramp signal by a value which is a proportional function of the error signal to compensate for the difference, (deviation of the output voltage from the desired reference value) and help the system reach the steady–state faster than the case where the compensator works alone. Switching frequency PWM techniques and the related random counterparts are investigated.

DYNAMIC DIGITAL CONTROL TECHNIQUE FOR IMPROVED TRANSIENT RESPONSE

A new digital control scheme aiming to improve the transient response and efficiency of an FPGA–based digitally controlled DC-DC converters in terms of shorter settling time with optimal over–and undershoots is also presented in this document. The approach enhances the dynamic response by dynamically controlling the ramp of the Digital Pulse Width Modulator (DPWM) unit through applying a linear and nonlinear shift to the conventional ramp–based Digital Pulse Width Modulator[25-31]. This will help the compensator reach the steady-state value faster. The dynamic ramp shift design method presented in this research utilizes an existing system digital controller and does not require any additional circuitry. During transients, the system diverges away from the desired steady–state range, and thus the power stage relies on the compensator to minimize the deviation and return to the wanted steady–state[11]. The longer it takes for the compensator to reach the steady–state, the worse the transient response becomes. The idea of adjusting the offset value of the Digital Pulse Width Modulator ramp was investigated in an attempt to achieve a better dynamics response through reducing the time required by the compensator to reach back to the steady–state during a transient condition. The Pulse Width Modulator shifting will only occur during transients for the reason that the error (which Basically compromises the shift value) is almost zero during steady–state. While during transients, the positive or negative value of the error will shift the ramp downwards or upwards.

II. LITERATURE REVIEW

Pulse Width Modulator (DPWM) with a fixed slope is dynamically and linearly shifted upwards or downwards by a value proportional to the error signal. The shift is done through applying a positive or negative offset (shift) value depending on the direction of the transient. This control approach aims to improve the transient response and efficiency of an FPGA–based digitally controlled DC-DC converters in terms of shorter settling time with optimal over and undershoots.

The dynamic Ramp Shift design method presented in this work is a linear DC shift control achieving a better dynamics response through reducing the time required by the compensator to reach back to the steady state during a transient condition. Moreover, it utilizes an existing system digital controller and does not require any additional circuitry. This shifting will only occur during transients for the reason that the error (which basically formulates the shift value) is almost zero during steady state, while during transients; the positive or negative value of the error will shift the ramp downwards or upwards. The digital technique is validated by computer simulation.

Experimental result of a prototype on a Modelsim FPGA platform verifies the concept. Improving the steady-state and dynamic behaviors of DC-DC converters is a quest that has not ceased to be the focus of design engineers and researchers whether in the analog or the digital control domains. Robust closed loop compensator design readily achieves a well-regulated performance at a fixed operating point but unexpected and fast load changes occur causing the whole system deviate into a transient mode away from the desired steady–state condition.

Under load changes, the difference in the energy balance must be handled, and since the power stage cannot catch up with the fast load change effectively, due to the large filter inductance required to decrease the output current ripple, the energy imbalance will be accounted for by the bulk filtering capacitors until the power stage is capable of delivering the energy needed at

the load side[16-23]. The time it takes the power stage to establish a steady state energy balance during the transient can result in out of tolerance output voltage which can lead to thermal stresses as well as system failure and degraded reliability.

III.PROPOSED ARCHITECTURE

Fig.1 Proposed PWM Architecture below shows the digital control in power electronics has led to an increasing use of digital pulse width modulators (DPWM). However, the clock frequency requirements may exceed reasonable limits when the power converter switching frequency is increased while using classical DPWM architectures. The synchronous design to increase the resolution of DPWM implemented on Field Programmable Gate Arrays (FPGA). The proposed circuit utilizes the Phase Shift (PS) functional unit of the on-chip Digital Clock Manager (DCM) blocks available on modern FPGAs, operating in fixed mode. This solution has been implemented, tested and compared to other implementations.

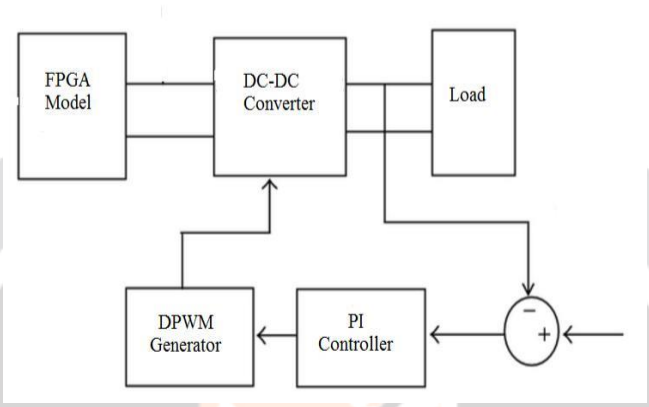

Fig.1 Proposed PWM Architecture

A. FPGA

Fig.2 DC- DC Bulk Converter shown underneath An FPGA is a device that contains a matrix of reconfigurable gate array logic circ uitry. When an FPGA is configured, the internal circuitry is connected in a way that creates a hardware implementation of the software application. Unlike processors, FPGAs use dedicated hardware for processing logic and do not have an operating system. FPGAs are truly parallel in nature so different processing operations do not have to compete for the same resources. As a result, the performance of one part of the application is not affected when additional processing is added. Also, multiple control loops can run on a single FPGA device at different rates. FPGA-based control systems can enforce critical interlock logic and can be designed to prevent I/O forcing by an operator. However, unlike hard-wired printed circuit board (PCB) designs which have fixed hardware resources, FPGA-based systems can literally rewire their internal circuitry to allow reconfiguration after the control system is deployed to the field. FPGA devices deliver the performance and reliability of dedicated hardware circuitry.

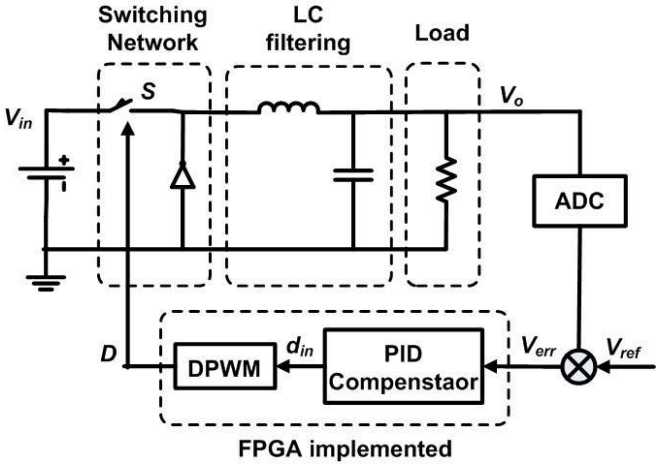

Fig.2 DC- DC Bulk Converter

Flexibility:

The control law is digitally implemented by writing a software code which makes it easily modified and promptly reprogrammed without requiring hardware modification. This is unlike the onboard discrete components (resistors and capacitors) needed to implement the control law via analog techniques.

Reliability:

Digital control realm is a component–free environment with the exception of a power–efficient, compactly integrated, fast and highly reliable microprocessor. This is in sharp contrast to the many analog components (resistors and capacitors) and power amplifiers required to implement the control law in the analog field. Fewer components with tighter integration means failure probabilities are reduced, which makes it nearly immune to temperature, and environmental variations, increasing the reliability of digital controlled systems.

Expandability:

Digital control techniques can be easily expanded to include sophisticated in addition to nonlinear control algorithms by simply expressing the architecture in software code rather than building the circuit using hardware components. These complicated control techniques are difficult to be implemented in the analog PWM switch mode power supplies. However, non–linear control techniques, which are easily expressed in digital control, proven, to achieve enhanced steady state regulation as well as the dynamic behavior of DC-DC converters. On the other hand, digital control falls short compared to the infinite–resolution and sampling–free analog control. One of the setbacks of digital control is the resolution of the two main building blocks of the digital loop: the Analog to Digital Converter (ADC) and the Digital Pulse Width Modulator (DPWM).While the conventional analog control is ideally assumed to have infinite resolution, the resolution of the two digital blocks decides the accuracy by which the duty cycle is determined.

B. DC-DC CONVERTERS

The switching power supplies offer higher efficiency than traditional linear power supplies. They can step-up, step-down, and invert. Some designs can isolate output voltage from the input. This article outlines the different types of switching regulators used in DC-DC conversion. It also reviews and compares the various control techniques forthese converters studied challenges; accuracy and delay should be addressed.

A circuit is aschematic for a digitally controlled DC-DC converter. The digital loop starts at the Analog to Digital Converter (ADC) where the sensed output voltage is first digitized and is next compared to the desired reference value, in deciding the accuracy and the overall performance of the converter. Consequently, a well designed PID compensator and high-resolution DPWM architecture are essential to achieving a tightly regulated converter output. Thus, research has been dedicated to increasing the accuracy of the system by increasing the DPWM resolution without increasing power loss and deteriorating efficiencyspecifically at high switching frequencies.

Therefore, individual fuel cells are typically combined in series into a fuel cell stack. A typical fuel cell stack may consist of hundreds of fuel cells. Fuel cells are classified primarily by the kind of electrolyte they employ. This determines the kind of chemical reactions that take place in the cell, the kind of catalysts required, the temperature range in which the cell operates, the fuel required, and other factors.

In other words, a more accurate performance entails high- resolution DPWM. High-resolution DPWM is required for the following reasons to mention a few:

- Avoiding limit cycling which will be explained in the following section.
- DPWM resolution is proportional to the switching frequency;
- The higher the resolution, the higher the cost and the higher the sampling frequency required which can prove to be impractical in terms of the needed oscillator, particularly at the high switching frequency.

ADC Resolution

Fig.3 Output Voltage Quantization and ADC Resolution describe in order to fully leverage the advantages of digital control, the two previously mentioned well–known and thoroughly–studied challenges; accuracy and delay should be addressed Research has focused on decreasing the delay and increasing the accuracy of both the ADC and DPWM. Significant effort has been devoted to analyzing the ADC resolution.

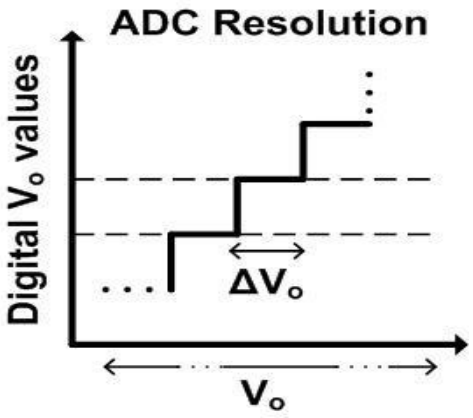

Fig.3 Output Voltage Quantization and ADC Resolution

Limit Cycle Oscillation

Fig.4 Limit Cycle Oscillation explain the V_{ref}, the resulting error signal, $V_{er}a$, is subsequently minimized through the action of the PID compensator which generates a duty cycle command (d_{in}), trying to maintain a near zero error signal and enhance the dynamic performance of the overall system. The output of the compensator is a digital representation of the duty cycle, (d_{in}) represented in discrete format from the Most to Least Significant Bit (MSB to LSB) as d [MSB, LSB]. The compensator is followed by theDPWM which translates the discrete duty cycle command of the compensator into an analog Pulse Width Modulated driving signal (D), controlling the ON–time of the main switch. Consequently, a well designed PID compensator and high-resolution DPWM architecture are essential to achieving a tightly regulated converter output. The least significant bit (LSB) of the DPWM determines the minimum change in the duty cycle. Thus the resolution of the DPWM is very critical.

Due to the limited resolution of any digital system, only limited discrete values of the duty cycle are obtained, which consequently means that, only, discrete values, of the, output, voltage ,can be achieved at, the, load side. If the, desired, output, voltage, which guarantees a zero error signal, is not mapped to exactly one of the available discrete values, then the, feedback loop, will continually alternate between at least two available values of the duty cycle. This kind of fluctuation is referred to as limit cycle oscillation. The main guideline to avoid the undesired limit cycle oscillations is to guarantee the mapping between minimum variations of the output voltage to a discrete duty cycle value that maintains a zero error signal.

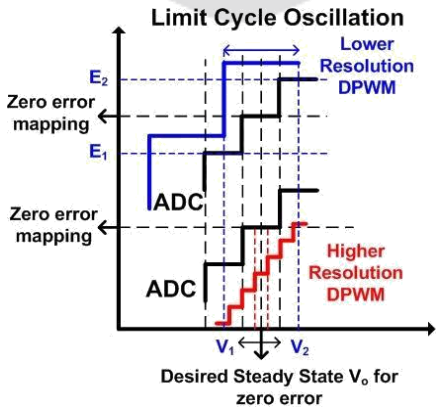

Fig.4 Limit Cycle Oscillation

IV. SIMULATION RESULTS

Fig.5 PWM output for 25% duty cycle and Fig.6 PWM output for variable duty cycle elucidate ModelSim PE, our entry-level simulator, offers VHDL, Verilog, or mixed-language simulation. Coupled with the most popular HDL debugging capabilities in the industry, ModelSim PE is known for delivering high performance, ease of use, and outstanding product support. Model Technology's award-winning Single Kernel Simulation (SKS) technology enables transparent mixing of VHDL and Verilog in one design.

ModelSim's architecture allows platform independent compile with the outstanding performance of the native compiled code. An easy-to-use graphical user interface enables you to quickly identify and debug problems, aided by dynamically updated windows. For example, selecting a design region in the Structure window automatically updates the Source, Signals, Process, and Variables windows. These cross-linked ModelSim windows create a powerful easy-to-use debug environment. Once a problem is found, you can edit, recompile, and re-simulate without leaving the simulator. ModelSim PE fully supports the VHDL and Verilog language standards. ModelSim PE also supports all ASIC and FPGA libraries, ensuring accurate timing simulations.

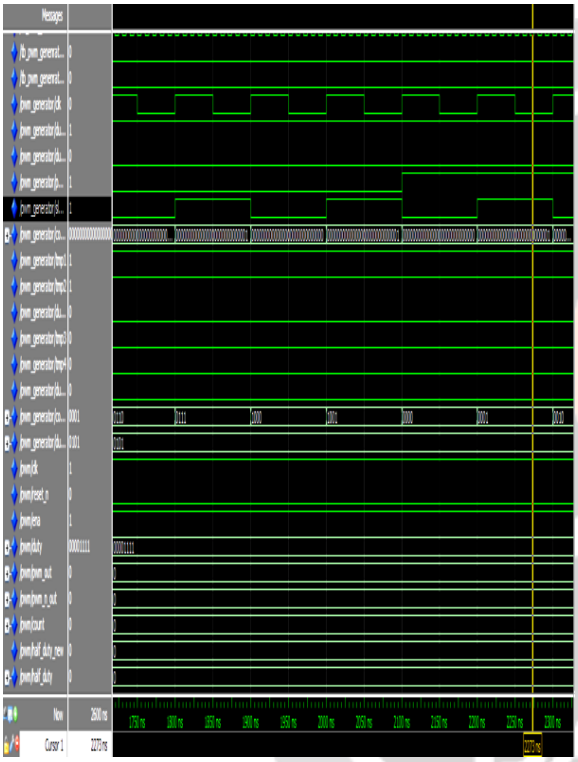

Fig.5 PWM output for 25% duty cycle

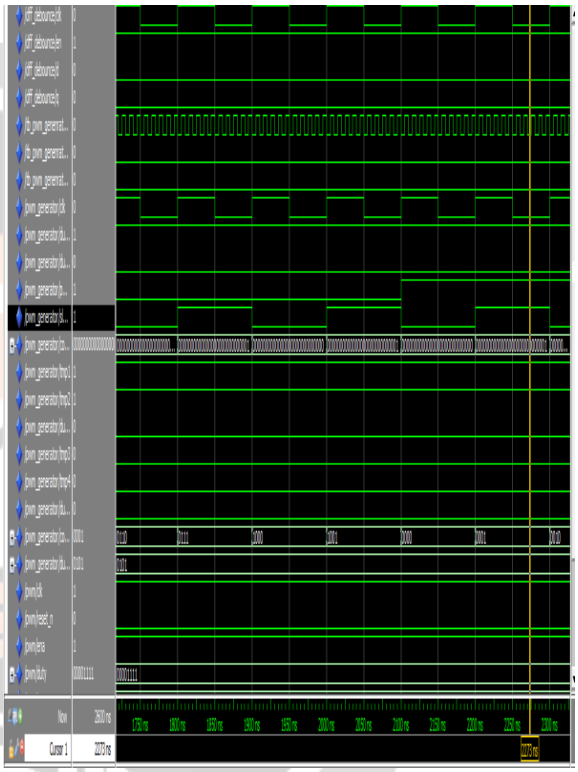

Fig.6 PWM output for variable duty cycle

TABLE - I CLASSIFICATION OF PWM TECHNIQUES

PWM switching technique	Case
Diagonal PWM switching (Ql, Q4 on/off simultaneously and Q2. Q3 on/off simultaneously)	Case1: without random, with random
QI, Q2 with 25% duty cycle and Q3. Q4 with PWM control (Not complementary switching)	Case2: without random, with random
Ql, Q2 with 100 % duty cycle and Q3, Q4 with PWM (Complementary switching) control	Case2: without random, with random

V. CONCLUSION

The DPWM can be implemented on FGPAs using the fine fixed phase shifting DCM capability. Unlike other high-resolution architectures proposed in the literature, the maximum clock frequency is determined by DCM instead of the multiphase circuit. An obtain working at the maximum clock frequency specified for the DCMs, showing the feasibility. This chapter proposes a new DPWM architecture design to operate high switching frequencies. The dynamic clock -adjusted digital ramp is presented as an improved version of the counter - comparator, it benefits from the best linearity and simplest architecture offers by the conventional counter-comparator DPWM nevertheless it adjusts the clock and thus the resolution in order to lower power consumption which was originally the barrier it the high switching operation. It is a direct emulation of the conventional ramp PWM signal expect for constant resolution the proposed dynamic clock -adjusted digital ramp utilizes fast clock and thus high resolution in the steady-state region and a slower clock with lower resolution outside that region. The anticipated saving in the power consumption due to slower clock oscillator will make the use of the simple architecture counter - comparator DPWM suitable for high switching operations. In additional to improve the response due to using a slower ADC outside the steady - state region.

VI. REFERENCES

[1] G. Foo and M. F. Rahman, "Sensorless direct torque and flux-controlled IPM synchronous motor drive at very low speed withthout signal injection," IEEE Trans. Ind. Electron., Trans. Ind. Electron., vol. 54, no. 1, pp. 660–670, Feb. 2007.vol. 57, no. 1, pp. 395–403, Jan. 2010.

[2] R.Seyezhai, "Design Consideration of Interleaved Boost Converter for Fuel Cell Systems", International Journal of Advanced Engineering Sciences and Technologies, Vol No. 7, Issue. No. 2, pp. 323 - 329.

[3] R. Seyezhai and B.L.Mathur. 2011, "Design and Implementation of Fuel Cell-based Interleaved Boost Converter", International Conference on Renewable Energy,ICRE 2011 Jan 17-21, 2011, University of Rajasthan, Jaipur.

[4] Shin, H.B; Park, J.G; Chung, S.K; Lee, .H.W; and Lipo,T.A. "Generalized Steady-State Analysis of Multiphase Interleaved Boost Converter with Coupled Inductors", in Proc.IEE Electronics Power Application, Vol. 152, No. 3, pp. 584-594, 2005.

[5] J.S.Anu Rahavi, T.Kanagapriya, R.Seyezhai "Design and Analysis of Interleaved Boost Converter for Renewable Energy Source", International Conference on Computing, Electronics and Electrical Technologies (ICCEET) 2012.

[6] S. De Breucker, K. Engelen, P. Tant, J. Driesen, "Adaptive Control Scheme for a Practical Bidirectional DC-DC Converter with an 80 kHz Switching and a 10 kHz Sampling Frequency", IEEE Trans on Ind. Electronics, Vol. 56, No. 6,June 2009

[7] P. S. Chen and Y. S. Lai, "Effective EMI filter design method for three-phase inverter based upon software noise method for three-phase inverter based upon software noiseseparation," IEEE Trans. Power Electron., vol. 25, no. 11, pp. 2797–2806, Jun. 2010.

[8] Y. S. Lai and P. S. Chen, "New EMI filter design method for single-phase power converter using software-based noise separation method," in Proc. IEEE Ind. Appl. Annu. Meeting, Sep. 2007, pp. 2282–2288.

[9] D. Jiang, R. Lai, F. Wang, F. Luo, S. Wang, and D. Boroyevich, "Study of conducted EMI reduction for three-phase active front-end rectifier," IEEE. Trans. Power Electron., vol. 26, no. 12, pp. 3823–3831, Dec. 2011.

[10] H.Kham, E. H. Milani, andK. E. K.Drissi,"Discontinuous random space vector modulation for electric drives: A digital approach," IEEE Trans. vol. 27, no. 12, pp.54, no. 2, pp. 1243–1245, Apr. 2007.

[11] J. Y. Chai, Y. C. Chang, and C. M. Liaw, "On the switched-reluctance motor drive with three-phase single-switch switch-mode rectifier frontend," IEEE Trans. Power Electron., vol.25, no. 5, pp. 1135–1148, May 2010.

[12] G. M. Dousoky and M. Shoyama, "Considerations for digital controllers targeted at conduced-noise spectrum-spreading in DC-DC converters," in Proc. Int. Power Electron. Conf., 2010, pp. 920– 926.

[13] A. Mirecki, X. Roboam, and F. Richardeau, "Architecture complexity and energy efficiency of small wind turbines," IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 660–670, Feb. 2007.

[14] K. T. Chau, C. C. Chan, and C. Liu, "Overview of permanent magnet brushless drives for electric and hybrid electric vehicles,"IEEE Trans. Ind. Electron., vol. 55, no. 6, pp. 2246–2257, Jun. 2008.

[15] L. Parsa and H. Lei, "Interior permanent magnet motors with reduced torque pulsation," IEEE Trans. Ind. Electron., vol. 55, no. 2,Issue. No. 2, pp. 323 - 329. pp. 602–609, Feb. 2008.

[16] M. G. Egan, D. L. O'Sullivan, J. G. Hayes, M. J.Willers, and C.. P. Henze, "Power-factor-corrected single-stage inductive charger for electric vehicle batteries," IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 1217–1226, Apr. 2007.

[17] G. O. Cimuca, C. Saudemont, B. Robyns, and M. M.Radulescu, "Control and performance evaluation of a flywheel energy-storage system associated to a variable-speed wind generator," IEEE Trans. Ind. Electron., vol. 53, no. 4, pp. 1074–1085, Aug. 2006.

[18] Y.-S. Kung, "Design and implementation of a high-performance PMLSM drives using DSP chip," IEEE Trans. IndElectron., vol. 55, no. 3, pp. 1341–1351, Mar. 2008.

[19] L. Harnefors and M. Hinkkanen, "Complete stability of reduced-order and full-order observers for sensorless drives," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1319–1329, Mar. 2008.

[20] L. Harnefors, "Globally stable speed adaptive observers for sensor less induction motor drives," IEEE Trans. Ind. Electron., vol.54, no. 2, pp. 1243–1245, Apr. 2007

[21] C. Xia, Z. Li, and T. Shi, "A control strategy for four-switch three-phase brushless dc motor using a single current sensor," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2058–2066, Jun. 2009.

[22] C. W. Hung, C. T. Lin, C. W. Liu, and J. Y. Yen, "Variable- sampling controller for brushless dc motor drives with low-resolution position sensors," IEEE Trans. Ind. Electron., vol. 54, no.5, pp. 2846–2852, Oct. 2007.

[23] S. M. N. Hasan, I. Husain, R. J. Veillette, and J. E. Carletta, "A PM brushless DC starter/generator system for a series-parallel 2 × 2 hybrid electric vehicle," in Conf. Rec. 42nd IEEE IAS Annu. Meeting, 2007, pp. 1686–1693.

[24] P. Bajec, B. Pevec, D. Voncina, D. Miljavec, and J. Nastran,"Extending the low-speed operation range of PM generator in automotive applications using novel ac– dc converter control," IEEE Trans. Ind. Electron., vol. 52, no. 2, pp. 436–443, Apr. 2005.

[25] T. Sakurai, H. Funato, and S. Ogasawara, "Fundamental characteristics of a test facility for micro-hydroelectric power generation system," in Proc. IEEE 6th IPEMC, May 2009, pp. 2612–2617.

[26] G. Foo and M. F. Rahman, "Sensorless sliding MTPA control of an IPM synchronous motor drive using asliding-mode observer and HF signal injection," IEEE Trans.Ind. Electron., vol. 57, no. 4, pp. 1270– 1278, Apr. 2010.