DESIGN AND IMPLEMENTATION OF LOW POWER DYNAMIC LATCH COMPARATOR

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In this article we composed a low power comparator for a use of low power simple to advanced converters. In advanced correspondence and sign preparing frameworks, ADC's assume a noteworthy part. To show signs of improvement execution of ADC's we outlined low power utilization comparator. The proposed comparator has a best execution than past best outlines. It is outlined in Cadence 180nm CMOS process and 90nm CMOS process with supply voltages from 0.8V to 1.8V. This outline works with up to clock recurrence of 900MHz and information recurrence of 10Hz to 5GHz.

Keyword: - Analog to Digital Converter. *CMOS process, low power comparator*

1. Introduction

Designing of comparator with low power and high speed is a difficult challenge for low power applications. Mostly comparators are used in analog to digital converters. Comparator is also called as one bit analog to digital converter. Because comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. A comparator is made up of specialized differential amplifier. These are mostly used in devices which measures and convert analog signal into digital form such as ADC's (analog to digital converters), as well as relaxation oscillators. The rest of the paper is organized as follows. In section 2 we explain some of the existing dynamic latch comparators. Section 3 explains the proposed method to reduce the average power and static power. Section 4 contains the simulation results for the proposed method.

2. Conventional double tail dynamic latch comparator

The Fig 1 shows the conventional double tail dynamic (clocked) latch comparator. It is similar to the basic comparator. In this comparator, transistors MC1 and MC2 are added with parallel to transistors M3 and M4 respectively.

This comparator has one disadvantage of high static power consumption. During decision phase, when Vin+ > Vin-, transistors M1, MC1 and Mtail turns ON. At this condition, VDD connects to GND which causes static power consumption. To overcome this problem, we added few transistors and proposed new comparator which gives best performance than other previous best design.

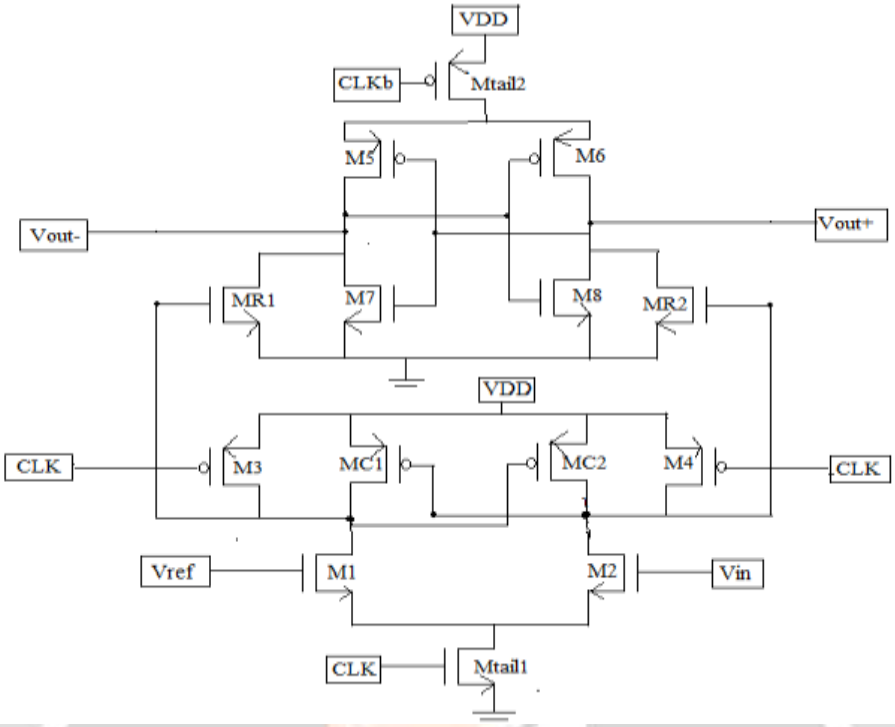

Fig -1: Conventional double tail dynamic latch comparator

3. Proposes dynamic latch comparator

Now we are presenting a low power consumption dynamic latch comparator. The operation of this comparator is similar to the conventional dynamic latch comparator. But this comparator consumes less average power and static power. Fig 2 shows the design of proposed dynamic latch comparator. Working of this comparator is shown in block diagram below.

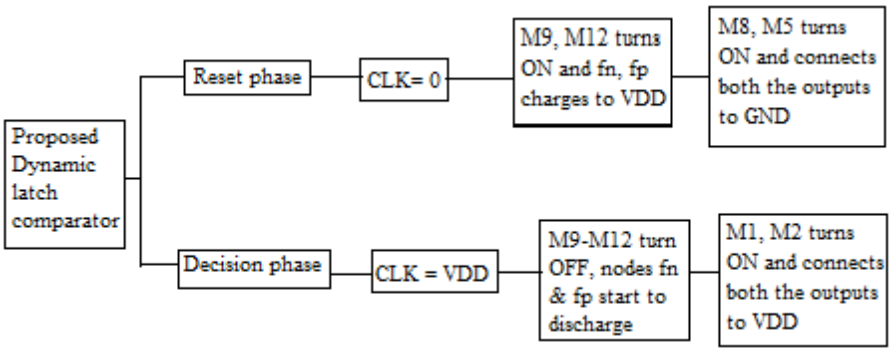

Fig- 2: Block diagram 1

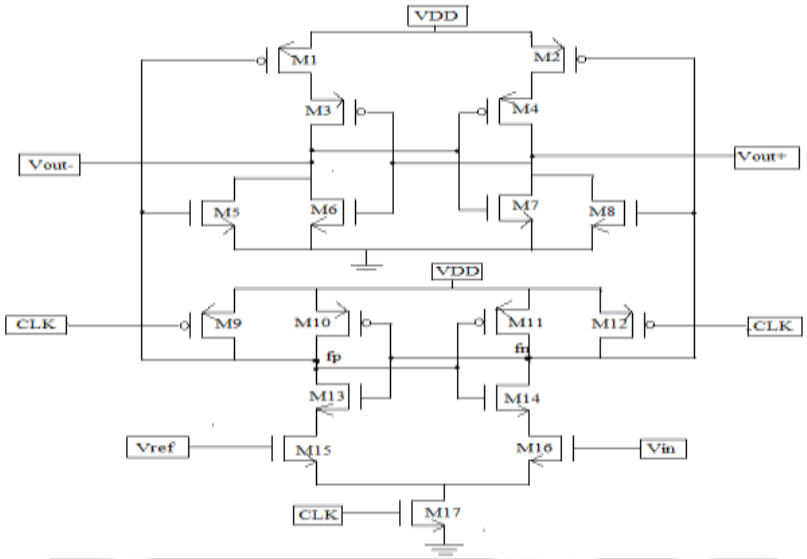

Fig -3: Proposed dynamic latch comparator

3.1 Simulation results

The simulation of the proposed comparator and existing comparator designs have been performed using Cadence tool and operations are performed using 180nm and 90nm technology. In order to compare other existing designs with our proposed design, we have taken some parameters like average and static power, propagation delay, PDP (power delay product), etc. The outputs are taken with 125MHz of clock frequency and 300MHz of input signal frequency.

3.2 CONVENTIONAL DYNAMIC LATCH COMPARATOR:

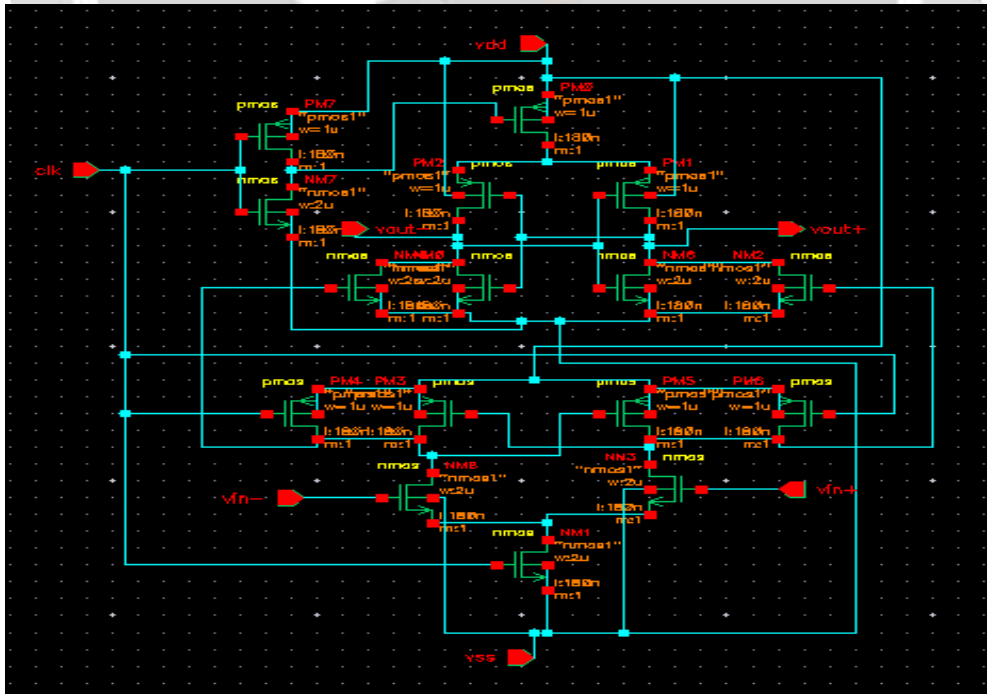

Fig -4: Schematic diagram

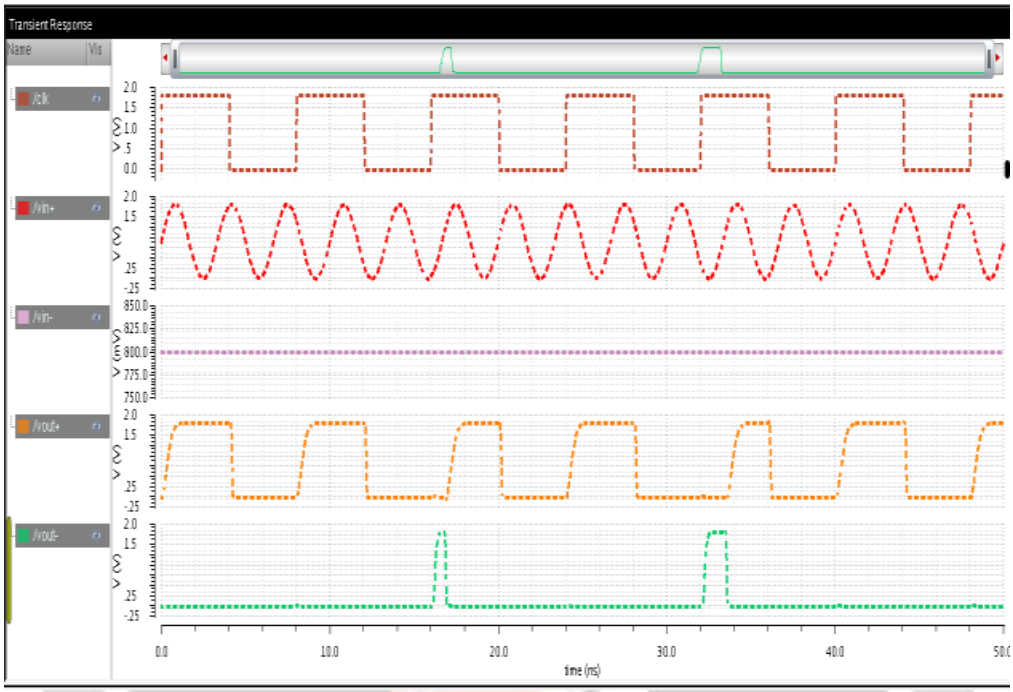

Fig -5: Schematic diagram

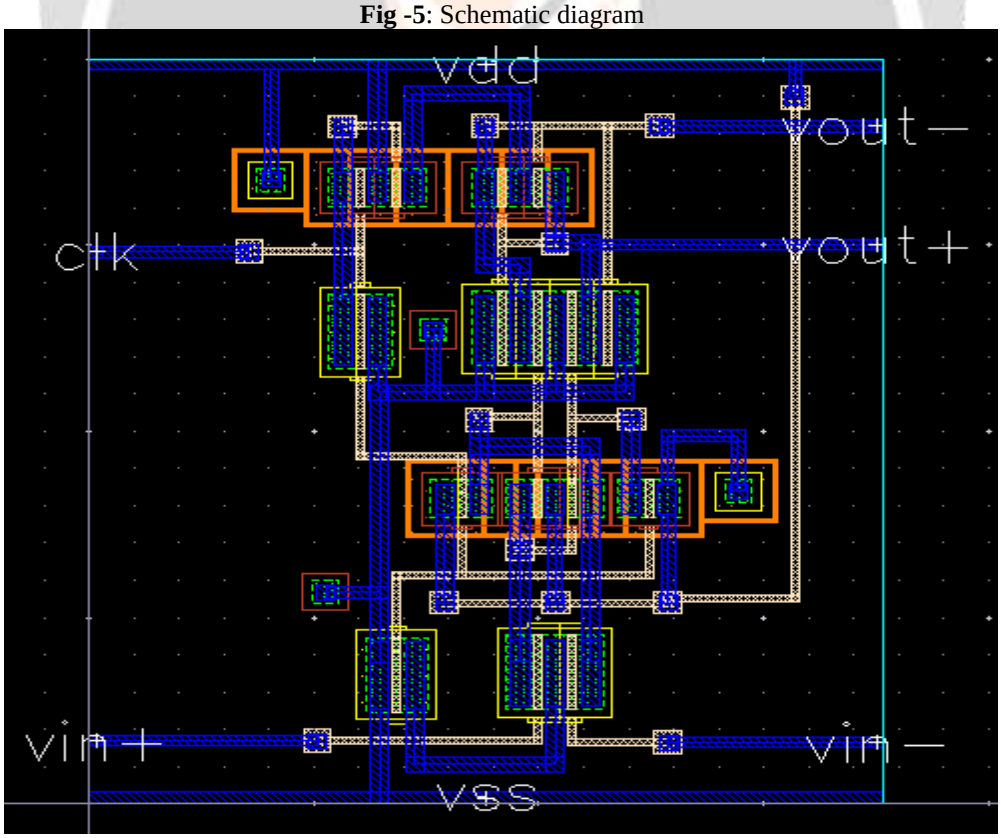

Fig -6: Layout diagram

3.3 PROPOSED DYNAMIC LATCH COMPARATOR:

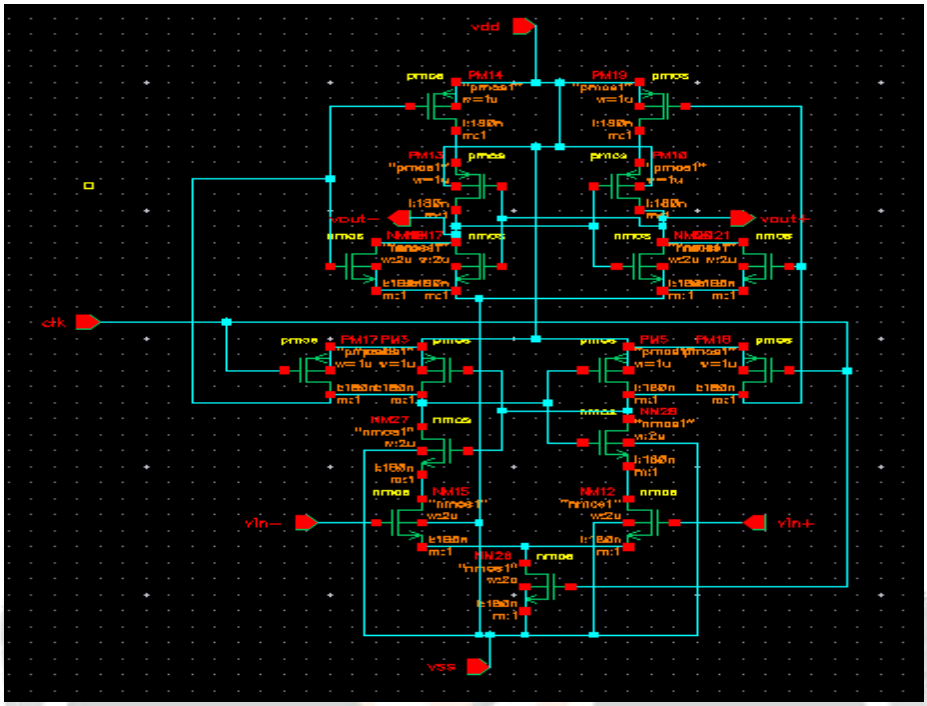

Fig -7: Schematic diagram

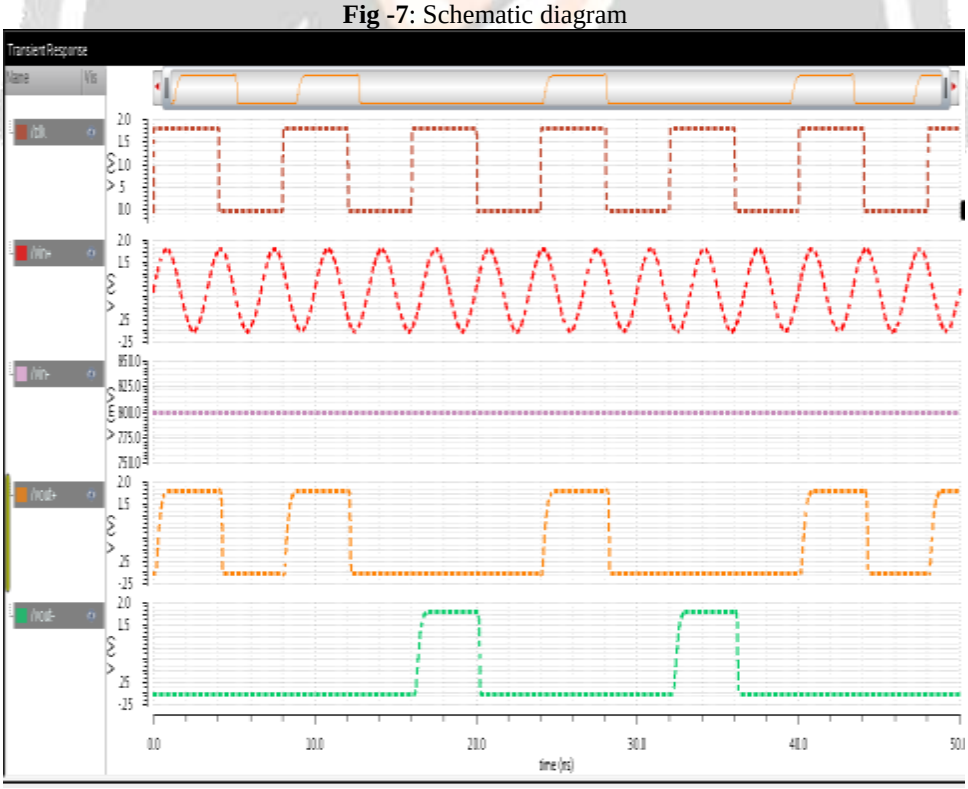

Fig -8: Output Waveform

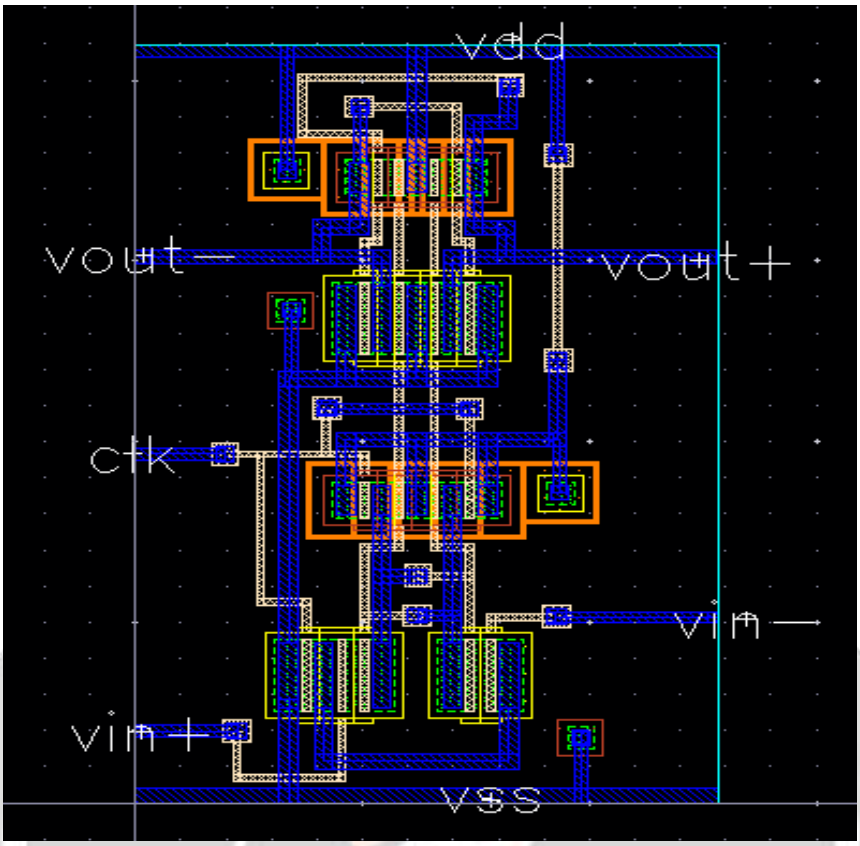

Fig -9: Layout diagram

Table 1. Performance comparison in 180nm (pre-layout).

Design specification	Conventional comparator	Comparator[1]	Comparator[2]	Proposed comparator
Average power(w)	150.0E-6	28.63E-6	31.56E-6	24.71E-6
Propagation delay(s)	1.267E-9	1.356E-9	1.335E-9	1.328E-9
PDP_{avg}(J)	0.19E-12	0.038E-12	0.041E-12	0.032E-12
Static power(w)	45.95E-12	50.94E-12	50.80E-12	28.91E-12
PDP_{static}(J)	0.058E-18	0.069E-18	0.067E-18	0.038E-18
No of transistors	16	14	18	17

Table 2. Performance comparison in 180nm (post-layout).

Design specification	Conventional comparator	Comparator[1]	Comparator[2]	Proposed comparator
Average power(w)	150.0E-6	31.27E-6	32.53E-6	24.78E-6
Propagation delay(s)	1.254E-9	1.343E-9	1.343E-9	1.327E-9
PDP_{avg}(J)	0.188E-12	0.0419E-12	0.0431E-12	0.032E-12
No of transistors	16	14	18	17

Table 3.Comparison of proposed comparator with different input voltages.

Design specification	0.8v	1v	1.2v	1.4v	1.6v
Average power(w)	3.74E-6	6.64E-6	10.54 E-6	14.54 E-6	19.24 E-6
Propagation delay(s)	1.56E-9	2.39E-9	2.693 E-9	1.182 E-9	1.278 E-9
PDP_{avg}(J)	0.0064E-12	0.0101E-12	0.015 E-12	0.0204E-12	0.026 E-12
Static power(w)	9.945 E-12	13.18 E-12	16.68 E-12	20.46 E-12	24.53 E-12
PDP_{static}(J)	0.014 E-18	0.018 E-18	0.023 E-18	0.028 E-18	0.033 E-18

Table 4. Performance comparison in 90nm.

Design specification	Conventional comparator	Comparator[1]	Comparator[2]	Proposed comparator
Average power(w)	5.968 E-6	750.7E-9	883.0 E-9	643.3 E-9

4. CONCLUSIONS

In this paper, a comprehensive analysis of power and delay for clocked dynamic comparators were done. Based on the analysis, a new dynamic comparator with low voltage, low power capability was proposed to improve the performance of comparator, mainly concerned in power consumption. Pre layout simulation results in 180nm and 90nm CMOS technology confirm that the power consumption of the proposed comparator is reduced to a great extent in comparison with all other dynamic comparators. And also the operational frequency of the proposed dynamic latch comparator is from 10Hz to 900MH.

5. REFERENCES

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