DESIGN AND IMPLEMENTATION OF UNIVERSAL GATE USING DG-FinFET 32NM TECHNOLOGY

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ABSTRACT

In this paper we have chosen the short gate [SG] FinFET device and explored the advantages over conventional single gate CMOS devices. We have designed the universal gates using both CMOS and FinFET and compared the result.

The main advantages of FinFET is lower leakage current and higher scaling factor when compared to CMOS technology. We have used 32nm technology for both the devices. Although there are many configuration in FinFET, we have selected Short Gate configuration as it has higher performance [2]. In this paper we have analysed the transient response and power consumption of the circuit. We have used LT-Spice tool to evaluate the performance of both the technology.

Key Word: *CMOS, FinFET, Double Gate, Transient Response*

I. INTRODUCTION

As the technology is advancing day by day, the density of transistor on a single wafer chip has increased and also frequency of operation. This leads to increase in consumption of power of battery operated device. As the density are increasing, the leakage current in these SoCs has increased. The main challenge is to reduce the power consumption and increase the speed. The FinFET have been proposed as alternate to meet these challenges posed by continuous scaling devices.

II. FINFET TECHNOLOGY

Former TSMC CTO and Berkeley professor Chenming Hu and his team presented the concept of FinFET in 1999 and UTB-SOI (FD SOI) in 2000. The main principle behind both the structures is a thin body, so the gate capacitance is closer to whole channel. The body is very thin, around 10nm or less. So, there is no leakage path which is far from the gate. The gate can effectively control the leakage. The basic structure of FinFET which they proposed would be a channel controlled by more than one side of channel. One of the Double-Gate Structures is shown in Figure 1.

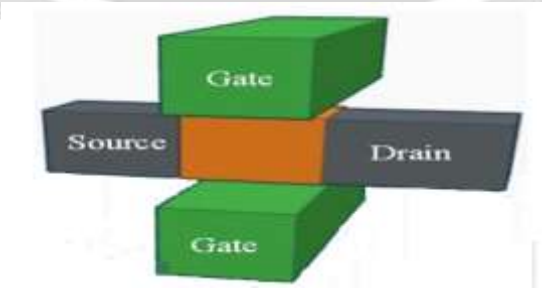

Figure 1. Double Gate Structure

III. FINFET CIRCUIT DESIGN

NAND Gate:
NAND gate is the combination of AND gate and NOT gate. It has the capability to perform the operations of logic gates such as OR, AND gate and NOT gate. The outputs of AND gate and NAND gates are inverse to each other.

From the truth table, it can be observed that NAND gate output will be high if any of its input is at low state. It will become LOW if both the inputs are HIGH. [7]

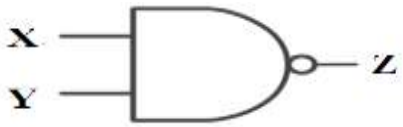

Fig.2 Logic Symbol

Inputs		Outputs
X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

Fig.3 Truth Table

NOR GATE:
The term NOR is a contraction of NOT-OR and it perform an OR function with an inverted output. A standard logic symbol for two-input NOR gate is shown in the fig4 and fig 5 respectively.

Similar to NAND gate, the NOR gate is a universal gate i.e NOR gate can be used to construct basic logic gates.

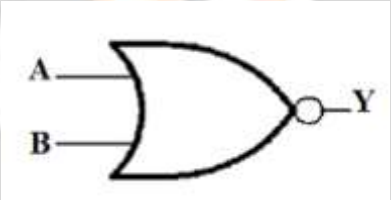

Fig.4 Logic Symbol

inputs		output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Fig.5 Truth Table

CMOS NAND GATE
The logical operation of the circuit can be verified by working in reverse. Consider the series connected nFETs MnA and MnB. If both $V_{in,a}$ and $V_{in,b}$ are high, then these transistors are active and conduct current while both pFETs are in cut off. This provides a strong conduction path to ground and gives an output voltage of V_{OL}=0v. However, if either A or B is low (either individually or at the same time) then there is no path to ground; in this case, at least one p-channel device is conducting to the power supply, giving a value of $V_{OH}=V_{DD.}$

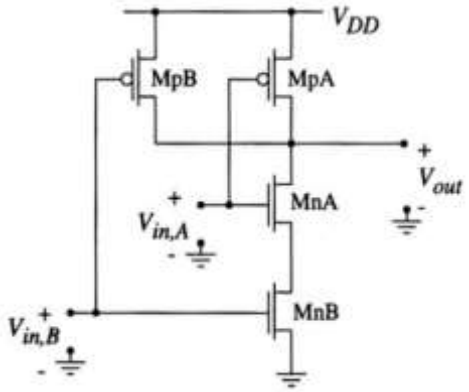

Fig.6 Logic Circuit

$V_{in,A}$	$V_{in,B}$	V_{out}
0v	0v	V_{DD}
0v	V_{DD}	V_{DD}
V_{DD}	0v	V_{DD}
V_{DD}	V_{DD}	0v

Fig.7 Truth Table

CMOS NOR GATE

A CMOS NOR2 gate can be built by using two complementary pairs as shown in Figure 5.16(a). Input *A* is connected to MnA and MpA, while *B* controls MnB and MpB. Note that the nFETs are connected in parallel, while the pFETs form a series chain. To understand the operation of the gate, we examine the conduction states of the transistors for different input voltages $V_{in,A}$ and $V_{in,B}$. If $V_{in,A}$=VDD then MnA is ON and MpA is OFF; since MnA provides a conducting path from the ground to the output, V_{out} = 0v. Setting $V_{in,B}$=V_{DD} turns MnB ON and MpB OFF and also results in V_{out} = 0v. And, if both $V_{in,A}$ and $V_{in,B}$ are high, then both nFETs are ON and the output voltage is V_{out}= 0v.The only input combination that results in V_{out}=V_{DD} is when $V_{in,A}$ = 0v = $V_{in,B}$, since both pFETs are ON while both nFETs are OFF. As verified by the truth table in Figure 5.16(b), this gives exactly the NOR2 operation.

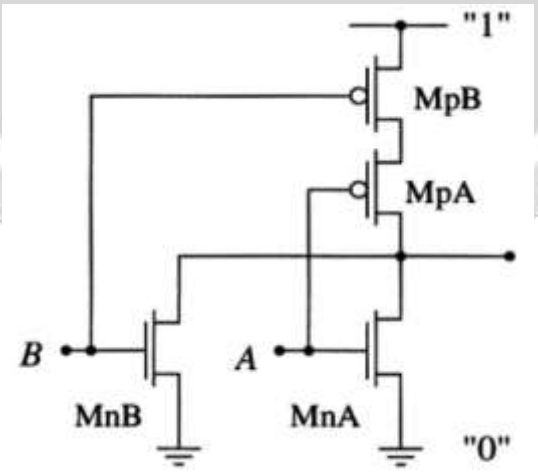

Fig.8 Logic Circuit

$V_{in,A}$	$V_{in,B}$	V_{out}
0v	0v	V_{DD}
0v	V_{DD}	0v
V_{DD}	0v	0v
V_{DD}	V_{DD}	0v

Fig.9 Truth Table

SG FINFET NAND GATE:

In this SDDG method of FinFET, i.e. simultaneously driven double gate FinFET both the gates are driven simultaneously. This arrangement is otherwise called Shorted gate FinFET implies as they are simultaneously driven so it additionally can be considered as shorted gate [4].The basic SG FinFET NAND gate is as shown.

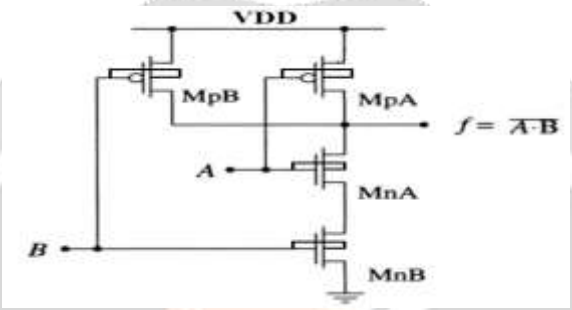

Fig.10 Short Gate (SG) FinFET NAND GATE

SG FINFET NOR GATE:

In the SG FINFET NOR gate PMOS are in series connected and NMOS is parallel connected. The figure shows the configuration of SG FINFET NOR gate.[7]

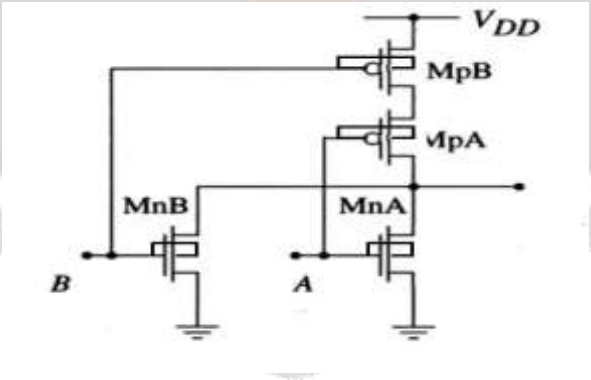

Fig.11 Logic Symbol

RESULT

The simulation for CMOS NAND and NOR gate is as shown.

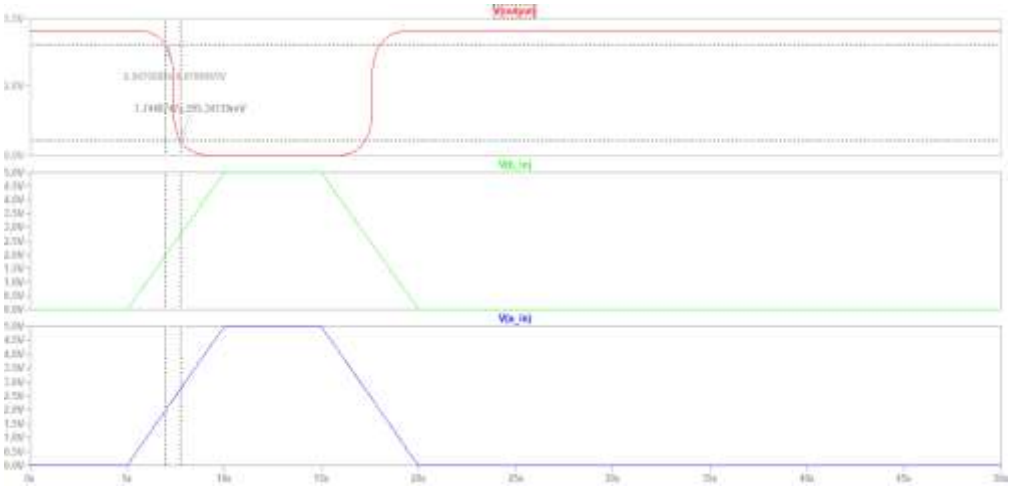

Fig.12 Transient response of CMOS NAND gate

The transient response is simulated as

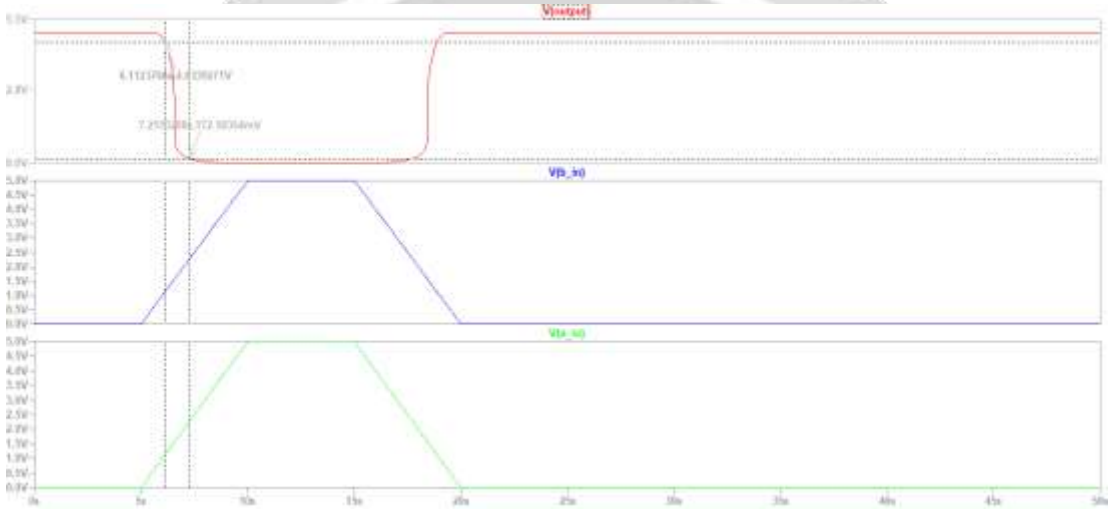

Fig.13 Transient response of CMOS NOR gate

Simulation of FinFET as Shown as

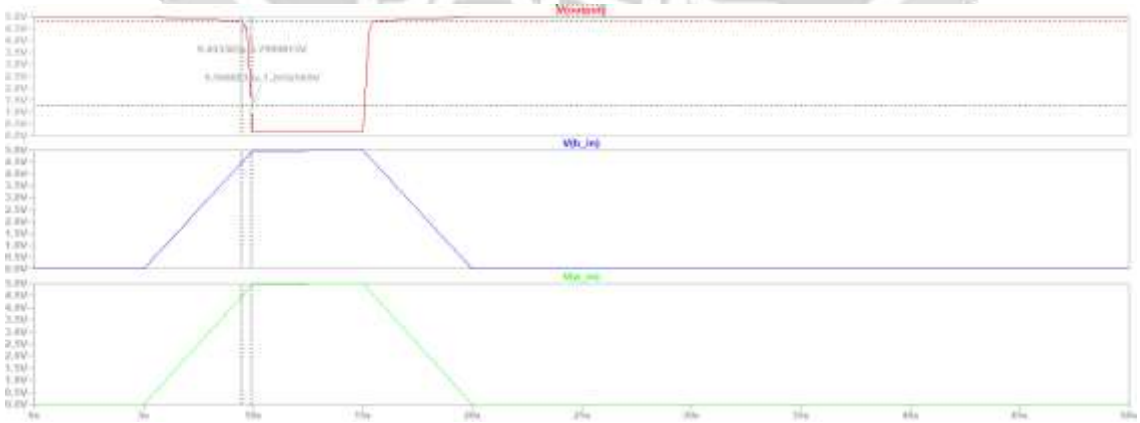

Fig.14 FinFET NAND Gate

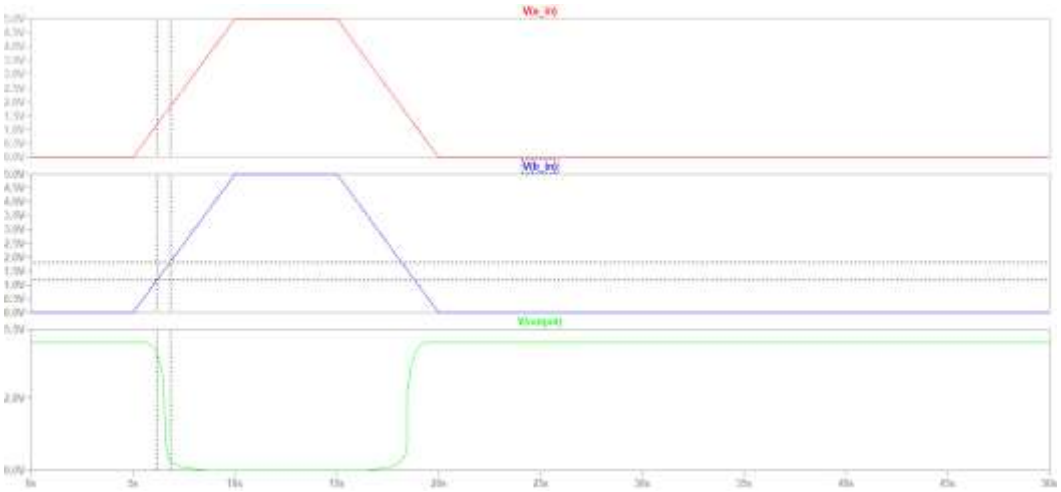

Fig.15 FinFET NOR Gate

The simulation time for universal gate is shown in table I.

	NAND GATE[ms]	NOR GATE[ms]
CMOS	0.78	1.13
FinFET	0.45	0.555

Table.I Transient Time

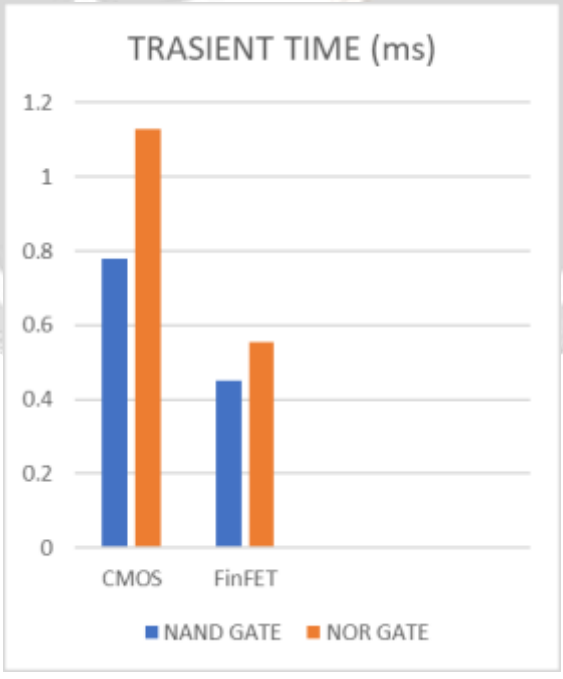

Fig.16 Transient time Graph

We observe from the table and graph that the transient time of FinFET based universal gate is far better in transient response. This makes the working of FinFET faster than single gate conventional CMOS devices.

Power consumption of each method is shown in table I1.

Voltage	CMOS NAND	CMOS NOR	FinFET NAND	FinFET NOR
Volt	**P=V*I (mW)**	**P=V*I (mW)**	**P=V*I (mW)**	**P=V*I (mW)**
1V	0.006	0.006	0.001	0.001
2V	0.007	0.008	0.002	0.003
3V	0.011	0.013	0.004	0.005
4V	0.014	0.017	0.005	0.006
5V	0.016	0.019	0.005	0.008

Table: II Power consumption of each method

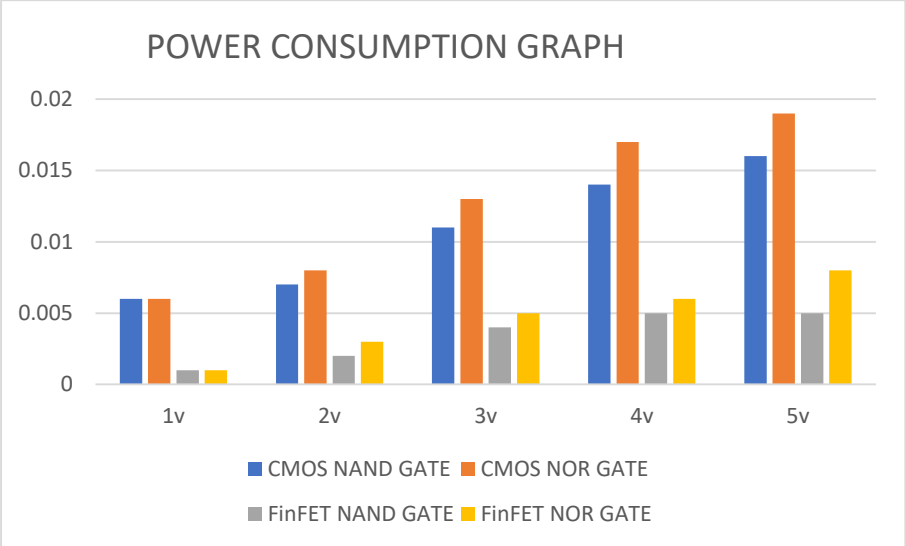

Fig 17. Power Consumption Graph

CONCLUSION

The transient time for CMOS NAND gate is found to be just 0.78ms compared to NOR gate which is almost 1sec. The FinFET NAND gate has transient time of 0.45ms.Which is almost half of it. The transient time for CMOS NOR gate is approximately 1s and the FinFET NOR gate has the transient time of 0.55ms. It is much clear that the FinFET technology has better response. As the transient time for FinFET is lesser the speed of FinFET gates will be higher.

The power consumption is calculated by taking various levels of voltages at the input to the maximum VDD level. The VDD level we have chosen is 5v. The formula used for power calculation is this simulation is given by

P= V*I

Where P is power, V is voltage and I is Current. The unit of power is Watt. The power consumption of CMOS NAND gate is 0.016mw whereas the power consumption of CMOS NOR gate is 0.019mw.The power consumption of FinFET NAND and NOR gate is 0.005mw and 0.008mw.It is observed from the simulation result that the power consumption is much lesser then CMOS technology.

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