DESIGN AND IMPLEMENTING COMMUNICATION BRIDGE BETWEEN I2C AND APB

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ABSTRACT

I2C master/slave controller is an interface that interconnects an advanced peripheral bus (APB) with Inter Integrated circuit (I2C) bus. The APB - I2C Bridge interfaces to the APB bus on the system side and the I2C bus. The APB interface is used to easily integrate the Bridge Controller for any SOC implementation. The controller performs the following functions. Parallel-to-serial conversion on data written to an internal 8bit wide,1024 deep FIFO. Serial-to-parallel conversion on received data, buffering it in a similar 8-bit wide,1024 deep FIFO. Device states are read by the APB using status registers that reflect the completion of I2C transfers. The APB bus is part of the Advanced Microcontroller Bus Architecture (AMBA) hierarchy of buses and is optimized for minimal power consumption and reduced interface complexity. to 100 Kbit/s in the Standardmode, up to 400 Kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the High-speed mode.I2C interface supports a Clock generation circuitry to derive I2C clock from APB clock. I2C interface supports various operational frequencies from 100 KHZ to 400 KHZ. It supports a simple bi-directional 2-wire bus for efficient inter-IC control.

Keyword *FIFO, APB, I2C, Bridge*

1.**INTRODUCTION**

Inter integrated circuit (I2C) bus transport is a two determination lines framework convention viz. serial information (SDA) and serial clock (SCL) signals. I2C transport has produced for passing the data from one module to different modules on one common communication network. I2C can be utilized for multi purposes to address by novel programmable address. I2C is communicating with different gadgets in a module by testing the SDA above Nyquist rate On the opposite side AHB giving interfaces to top of the line devices and here in the correspondence between these devices as full duplex parallel correspondence. AHB is a large data transfer capacity and rapid protocol. AHB is a less mind-boggling convention and good with any plan stream. In I2C convention has been discussed effortlessly with gadgets with no loss of information. Further, it gives rapid information transfer. the information has been spared in registers with the assistance of I2C convention. In I2C convention gave on less demanding medium to correspondence between the gadgets as it utilizes just two lines (SCL and SDA) for correspondence between the ace and slave. In [4], the creators' exhibited that the address and the chip select flag select the I2C gadgets. In this outline both chip select and address of the gadget are default to1 as configuration is for a particular slave only. In the creator shows how I2C ace controls transmits and gets information to and from the slave with appropriate synchronization. Be that as it may, I2C serial convention to AHB parallel convention for fast information change isn't yet revealed in the writing. In this paper, the information transfer from I2C master to I2C slave, AHB master to AHB slave by utilizing correspondence connect. Further, the territory and postponement for I2C to APB convention and I2c to AHB convention has been accounted for.

2. I2C PROTOCOL

Each I2C transport comprises of two signs: SCL and SDA. SCL is the clock flag, and SDA is the information flag. The clock flag is constantly produced by the present transport master; some slave devices may compel the time low now and again to defer the master sending more information (or to require more opportunity to plan information before the master endeavors to check it out). This is called "clock extending" and is depicted on the convention page. I2C tradition anticipated that would allow different slave fused circuit communicate with no less than one specialists on circuits. All data trade with two conditions. They are starting and stop bit condition. The condition begins with acknowledgment of start condition and is finished by encountering stop condition. At the point when start condition develops transport is believed to be involved and it will re-essential in a comparable state till all sales for the bus have been permitted. For the read/make assignment, first the slave's address is sent trailed by the looking at data, as showed up in figure 1. The recognize happens after each byte. The recognize bit enables the beneficiary to flag the transmitter. That the byte was effectively gotten another byte might be sent. The master produces all tickers beats including recognize ninth clock beat. The clock characterized as takes after the transmitter discharge than SDA line amid the recognize clock beat. So, the collector can pull the SDA line low and it stays stable low amid the high time of this clock beat.

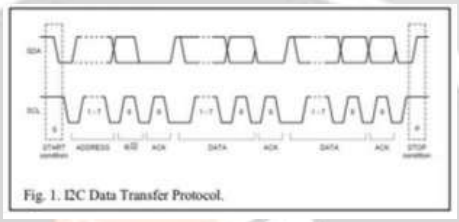

Figure.1: I2C Data Transfer Protocol

3.APB PROTOCOL

Figure.2 Explains the edge cycle as-IDLE: The default state. SETUP: When exchange is required the bus moves into the SETUP state, where the select flag, PSELx, is avowed. The exchange remains here for one clock cycle and moves to the ENABLE state on the running with rising edge of the clock. Attract: The enable hail, PENABLE, is imparted. The address, make and select signs need to remain stable in the midst of the advance from the SETUP to ENABLE state. If no further trades are required the vehicle returns to the IDLE state. Obviously, if another move's to be made then the exchange will move to SETUP. Address, make and select signs would glitch be able to in the midst of advance. In this paper isolates the reusability of I2C utilizing UVM and showed how the certification condition is manufactured and test cases are executed for this convention.

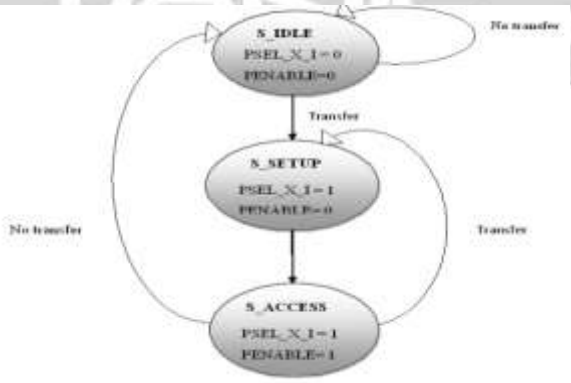

Figure 2: Operating States of APB interface

4.DESINGNED ARCHITECTURE

The illustrating square configuration of the finished correspondence assistants among I2C and APB is appeared in Fig. 3. The Structure contains two basic pieces, i.e. I2C Slave and APB Master. I2C Slave takes the

information from I2C Master in isolated course of action and offers it to APB Master. This APB Master likewise passes on this information to APB Slave in APB Protocol. In this manner a correspondence between I2C Master and APB Slave is finished.

A). Write Operation

- Whenever I2C Master needs to visit with APB Slave it would be done by frameworks for I2C Slave.
- I2C Slave will affirm Data Valid and Address Valid signs.
- Seeing these banners high, masterminded APB Master considers the memory for its responsiveness and begins APB shape state machine.
- I2C sends four bits of 8-bit information serially to be shaped on APB Memory at four unfaltering spaces.
- After trade of every byte APB Master keeps a mind tally whether each and every one of the four memory territories are vivified sensibly.
- As soon as the information at APB Master is restored it traded the same 32-bit information to APB Slave.

B). Read Operation

Here again when I2C need to investigate information from the APB slave, Correspondence will occur through APB master to I2C slave to I2C master APB Salve will send a banner to APB Master empowering that the information is available to be examined. APB Salve by then transmits the data to APB Master where it is secured in the internal memory to be brought by I2C Slave at time explanation behind time

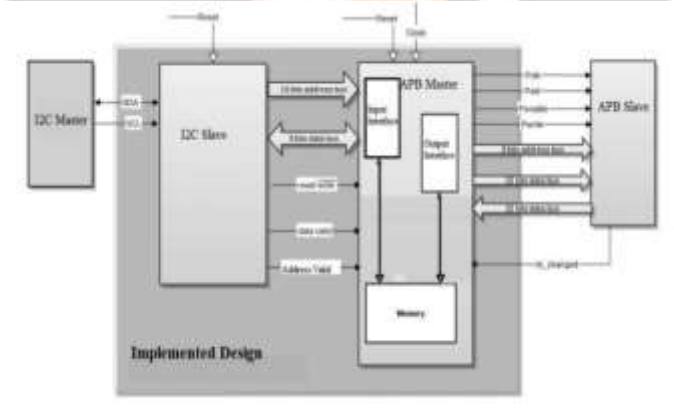

Figure.3 I2C Master and APB Slave

C.) AHB APB Interface Focus AHB to APB is an AHB slave and AMBA APB Master that gives an interface (associate) between the fast AHB space and the low-control APB territory. The Core AHB to APB interfaces with Core AHB/Core AHB Lite through the AHB interface, or Core APB through the APB interface.

D.)Key Features

- Bridges between Advanced Microcontroller Bus Architecture (AMBA) Advanced High-Performance Bus (AHB) and Advanced Peripheral Bus (APB).
- Automatic relationship with Core AHB/Core AHB Lite and Core APB in Smart Design.
- AMBA APB agreeable.

E). Maintained Interfaces

Center AHB to APB supports an AHB or AHB-Lite slave interface related with an AHB or AHB-Lite reflected slave interface (for example, Core AHB or Core AHB Lite) and likewise an AMBA APB pro interface that interfaces with an AMBA APB reflected pro interface (for example, Core APB)

F). Block Diagram

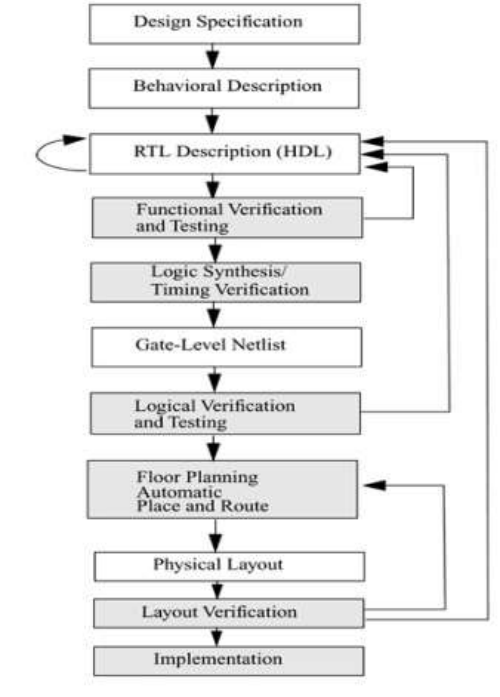

Figure.4 ASIC Design Flow

G. Description

The I2C-APB Bridge is used make a translation of AHB signs to APB signals. The I2C-APB Bridge is moreover used to isolate the tip top AHB (system transport) from the slower APB (Peripheral Bus). The I2C-APB Bridge is an AHB slave part which recognizes trades concentrating on an APB periphery, unravels the address, and gives an APB, periphery transport, trade to the concentrated-on periphery or memory. The I2C-APB Bridge can decipher up to sixteen APB peripherals. On create trades, the I2C-APB Bridge gives the form control (PWRITE), select (PSELx), and address (PADDR) and data (PWDATA) to the concentrated-on periphery or memory. On read trades, the I2C-APB Bridge multiplexes the concentrated-on periphery's data (PRDATA_device) to the AHB HRDATA with the most ideal arranging. The I2C-APB Bridge furthermore reestablishes the HREADYOUT movement back to the AHB pro to show that the IPC-APB Bridge has completed the APB trade and the data is read

5.SIMULATION RESULT

The I2C and APB Bridge circuit are implemented using verilog HDL and stimulated on ModelSim 10.3c. The RTL and the technology is done in Xilinx ISE 13.4.

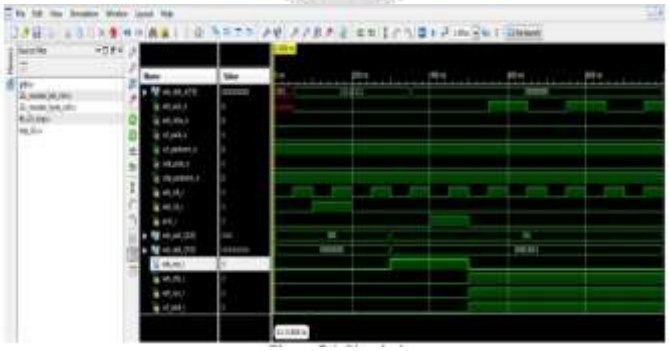

Figure 5 Simulation I2c result:

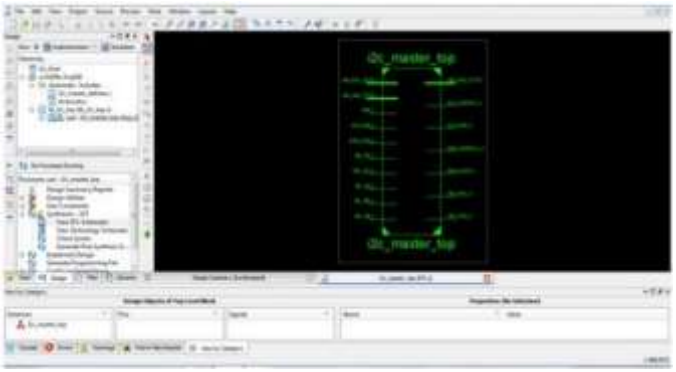

Figure 6 Top Module

Figure 7 RTL Schematic

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	127	960	13%
Number of Slice Flip Flops	127	1920	6%
Number of 4 input LUTs	227	1920	11%
Number of bonded IOBs	33	66	50%
Number of GCLKs	1	24	4%

Figure 8 Device Utilization

6. CONCLUSION

The realized correspondence associates between the I2C and AHB tradition. This tradition plot and completed in Xilinx ISE 14.7, Spartan 3E, Using Verilog HDL. I2C Bus tradition was viably made by the measures given by NXP Semiconductors. The tradition correspondences demonstrate was set up between I2C tradition and APB tradition and in my errand Communication could be completed to I2C and AHB traditions. The data trade spills out of I2C pro to I2c slave and AHB pro to AHB slave. It will be showed up in building diagram. I am ingested the reenactment occurs are checked and data trade from the I2c expert to AHB slave. It will be unmistakably devoured and seen in gave reenactment comes to fruition. As proposed it will take mind have been taken to arrange data trade speed of both the vehicles for better consistence. We have to plan to configuration appear with added bolsters at the interface to get significantly higher speed of data trade. Here what I am seen by actualizing the correspondence connect

between the I2C and AHB convention This paper exhibits and we will get less defer time and decreased zone what's more, diverged from data transmission among I2C and APB parallel traditions due to the High execution and less circuit multifaceted nature in parallel Advance High Performance(AHB) transport tradition.

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