

DESIGN AND SIMULATION OF 2.4GHz CMOS FREQUENCY SYNTHESIZER FOR S BAND APPLICATION

S. D. Shah¹, Dr A.C.Suthar²

Department of Master Engineering In Communication System Engineering,
L. J. Institute of Engineering and Technology, Ahmedabad, Gujarat

ABSTRACT

The frequency synthesizer is an electronic system for generation of one or more frequencies from one reference frequency sources. The frequency synthesizers are an essential part of any modern communication system. They are found in many modern devices like radio receiver, satellite receiver, wireless network devices, GPS system etc. The frequency synthesizer, which performs the main role of carrier generation. With the increasing demand for low cost and high performance of wireless transceiver building blocks, the low-power requirement is a great concern for radio-frequency integrated circuit (RFIC) designers. Intensive effort has been made to develop RF integrated circuits and systems in the higher frequency (GHz) range using the low-cost CMOS process. Another concern for frequency synthesiser is phase noise. The performance in power consumption and channel selection of frequency synthesizer are limited by the two most important building blocks, namely the programmable frequency divider and the voltage-controlled oscillator (VCO). The objective of this research work is to design this critical blocks for the frequency synthesizer with low power requirement. Software to be used is LTSpice Specially 2.40-2.50 GHz band is ISM band, so we can develop system in this band with 5MHz reference frequency.

Keywords: Frequency synthesizer; CMOS; RFIC; PLL; charge pump; frequency divider; VCO.

I INTRODUCTION

The frequency synthesizer generates a set of signals of given frequencies with the stability and precision referred to a single frequency reference source. It is regarded as one of the most critical modules in modern wireless communications systems. Figure 1.1 shows the architecture of a typical modern transceiver. The output signal generated by the frequency synthesizer is normally termed as the local oscillator (LO) signal, since it is used as the reference oscillator for frequency translation and channel selection in communication systems. At the receiver side, the high frequency LO signal is used to down-convert the incoming signal into a lower frequency (baseband or intermediate frequency (IF)) where it can be processed to extract the information it is carrying. The same LO signal can be used to up-convert the baseband signal to an RF frequency, so that it can be transmitted over the medium.

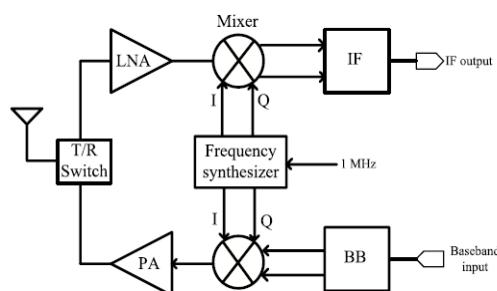


Fig. 1 The role of frequency synthesizer in a transceiver

The frequency synthesizer is normally implemented using phase-locked loop (PLL). The PLL based frequency synthesizer is one of the key building blocks of an RF front-end transceiver. The PLL frequency synthesizer system is designed to ensure the accuracy of its output frequency under operating conditions. Phase

noise is one of the most critical performance parameters of the frequency synthesizer. The goal to meet fine frequency resolution with reasonable levels of power consumption remains a challenging task for the circuit designer.

II. LITERATURE REVIEW

After having discussed briefly about the fundamentals of phase-locked loop, we now compare the state of the art 2.4 GHz frequency synthesizers. In reference [5] a new supply regulated LC-VCO that reduces the impact of process variations and temperature on current consumption and phase noise. A single ended charge pump architecture offers very high output impedance over a wide output voltage range. 0.18 μ m CMOS technology is used, Power dissipation:18.4mW Phase noise:-114.79dBc/Hz In reference [4] indirect synthesis uses a PLL Programmable frequency divider in the loop using three or four 4-bit BCD counter stages providing a large number of frequencies from a single reference frequency CMOS 0.18 μ m technology with An integer-N fully programmable divider employs a novel True-single-phase-clock (TSPC) 47/48 prescaler and 6 bit P and S counters are used. The PLL uses a series quadrature VCO (S-QVCO) to generate quadrature signals. Power dissipation:7.0mW Phase noise:-122.4dBc/Hz In [2] a switched varactor array based LC-VCO is used, the charge pump current is programmed proportional to division ratio. By combination of these techniques, a constant loop bandwidth is achieved over Operating frequency range from 3.45 to 4.22 GHz. 0.13 μ m technology with Power dissipation : 21.1mW and Phase noise:-117.3dBc/Hz. In reference [1] A single synthesizer with a dual-band VCO used to generate two separate frequency band. The programmable loop divider uses the pulse-swallow made up of a divide by N/N+1 prescaler, a fixed divide-by-P program counter and a programmable swallow (S-) Counter. With 0.18 μ m technology, Power dissipation:22.7mW, Phase noise:-132.6dBc/Hz In [3] with noise filtering technique a hybrid fractional-N frequency synthesizer for wireless application is implemented with TSPC. With 0.18 μ m technology Power dissipation:20mW and Phase noise:-113.51dBc/Hz.

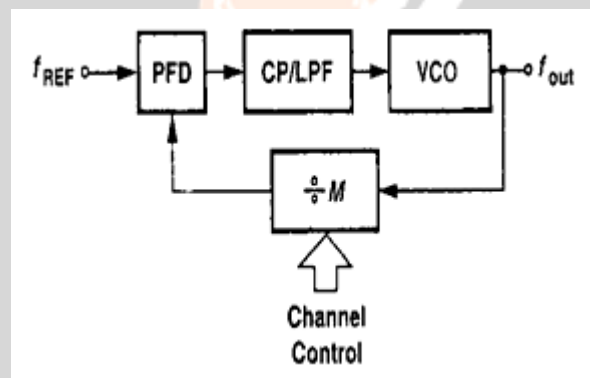


Fig.2 Block diagram of frequency synthesizer

III. STUDY OF DIFFERENT BLOCKS

Different blocks are explained below.

A. PFD

A phase detector (PD) is a circuit whose average output is linearly proportional to the phase difference between its two inputs. In an ideal case, the relationship between and is linear. The gain of the PD is K_{PD} expressed in V/rad .

A familiar example of phase detector is the exclusive OR (XOR) gate. As the phase difference between the inputs varies, so does the width of the output pulses, thereby providing a dc level proportional to phase. The XOR PD produces error pulses on both rising and falling edges.

The major drawback of XOR PD is its inability to detect frequency difference. As any frequency difference exists, the phase difference would be accumulated either in a positive direction (reference frequency slower than divider frequency) or in a negative direction (reference frequency faster than divided frequency). The second issue is that, when the PLL is locked, the average of XOR PD output is zero. This zero voltage is averaged from a square wave of twice the reference frequency. Therefore, the pole of LPF has to be low enough to attenuate this reference spur. The XOR PD is sensitive to the duty cycle of the input signals.

I. Tri-State Phase Frequency Detector (PFD)

The EXOR and DFF based PD's fail to detect the frequency difference and are not suitable for PLL applications where initial VCO oscillation frequencies are far away from reference. A tri-state PFD [5] detects both phase and frequency difference. Fig.4 shows the state diagram and the implementation of the PFD.

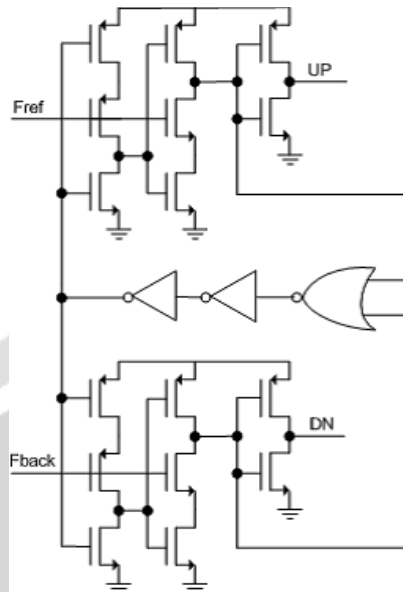


Fig. 3 Phase Frequency Detector

A PFD compares two signals and produces the phase error as output. These are basically digital circuits. A dynamic logic PFD is used in the PLL. These use lower number of transistors and consume less power when compared to a static logic PFD [2]. Reduction in dead-zone is also achieved by this configuration as shown in Fig. 3

B. Charge Pump with loop filter

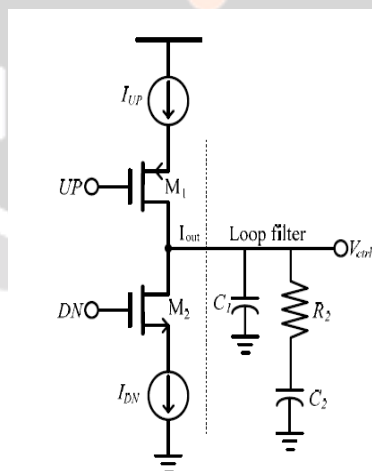


Fig.4 Charge pump with loop filter

A charge pump generally consists of two current sources that are switched on and off at the proper instance of time. positive pulses appear at UP while DN stays at 0. Under this condition, M1 is turned-on and M2 is turned-off such that the current IUP charges the loop filter to pull-up the VCO frequency. When positive pulses appear at UP while DN stays at 0. Under this condition, M1 is turned-off and M2 is turned-on such that the current IDN discharges the loop filter to pull-down the VCO frequency[15]. Under locked condition, both switches M1 and M2 are on for a short period equal to the dead zone pulse width and net current flowing into

the loop filter is negligible. Loop filter filter outs this control voltage to control output of VCO. Here second order loop filter is used. Values of C1,C2,R2 can be given as from given equations[7].

$$C2 = \frac{I_{cp} * K_{vco}}{2\pi N (W_n)^2}$$

$$C1 = \frac{C2}{16}$$

$$R2 = \frac{1}{2\pi W_z 1 C2}$$

Where W_c = loop bandwidth

W_n = natural frequency = $W_c/2$

W_z1 = zero frequency = $W_c/4$

N = division ratio

C. Voltage Controlled Oscillator (VCO)

The voltage controlled oscillator (VCO) is an important building block of a PLL synthesizer which generates periodic signals. Commonly, both ring oscillators and LC oscillators are used in GHz range applications. However, ring oscillators suffer from poor phase noise compared to that of LC oscillators and are less suitable for high-end wireless communication systems. LC oscillators are more attractive due to their better phase noise performance and lower power consumption [15]. However, they occupy larger area compared to that of ring oscillators. Here MOS varactor is used to tune frequency.

D. Frequency dividers

The frequency divider is one of the building blocks of a PLL frequency synthesizer which converts the oscillator high output frequency to a lower frequency which can be compared to a reference source. As the VCO is operated in multi GHz range, the PLL requires high frequency dividers.

However, the requirement of the channel selection in the frequency synthesizer demands a programmable frequency divider. The four key design issues related the design of the programmable

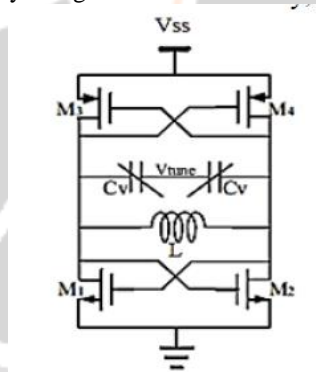


Fig.5 LC VCO[15]

dividers are the high input frequency, programmability of the division ratio, power consumption and input sensitivity (minimum amplitude of the input signal)[7]. In general, the power consumption of the divider is linearly proportional to the operating frequency. Its maximum operating frequency depends on the architecture style, supply voltage and output load. The design of analogue dividers are based on the injection locking technique where as digital dividers are implemented using dynamic or static latches and flip-flops.

Digital frequency dividers which divide the input signal by N times are normally termed as modulo- N counters which can be classified as ring or binary counters. Modulus counters need to incorporate programmable logic circuits to provide various division ratios. Fig. 6 illustrates the proposed frequency divider. As it is obvious, we have replaced S counter and P counter with an integrated P&S counter. Output of integrated P&S counter controls Modulus logic bit of prescaler[13]. As with channel space of 5MHz, the frequency band from 2405MHz to 2480MHz we need a frequency divider from 481 to 496 to cover all 16 available channels. These numbers can be obtained by a divide-by-7/8 dual modulus prescaler ($M=7$), $P = 64$ and $33 \leq S \leq 48$.

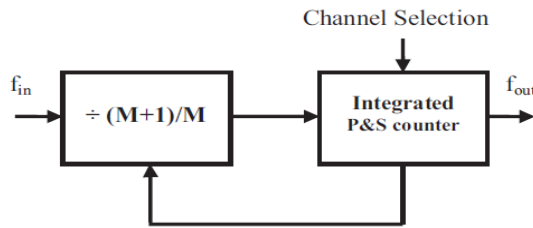


Fig.6 Asynchronous programmable modulo-P counter

I Dual Modulus Prescaler

Fig.7 shows divide-by-7/8 dual modulus prescaler. block diagram. This prescaler includes a divide-by-3/4 dual modulus prescaler and a divide-by-2. When the modulus bit is zero, this divides input frequency by 8. When the modulus bit changes to 1, output of Q1 is reset by M1-M3, as Q2Q3=11. So the number of Q1Q2Q3=111 is eliminated and the input frequency is divided by 7. A TSPC D-Flip Flop (DFF) that has been used in the dual modulus prescaler.

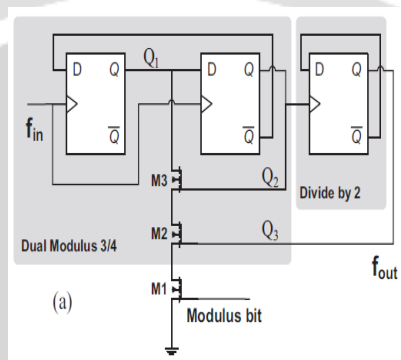


Fig.7 Dual modulus prescaler

II. Integrated P&S counter

Fig. 8 shows the block diagram of Integrated P&S counter. As it is apparent, this counter consists of a divide-by-64 (P counter) that is made up of 6 divide-by-2. Digital circuit consists of XNOR gates (X0 - X4), AND gates (A0, A1) and a RESETSET Flip Flop (RSFF). This digital section has replaced S counter in conventional ones and has the duty to control modulus bit of dual modulus prescaler. A1 gate is driven by XNOR gates (X0 - X4). So when the value of P counter (P5-P0) is equal to predefined C number (1C4-C0), output of A1 gate becomes logic 1. In this moment, as P5 is 1 as well, RSFF is set by A2 gate and dual modulus prescaler divide input frequency by 7. When P5 changes to 0, RSFF is reset and dual modulus prescaler return to divide-by-8 state. For more details, assume the P counter {P5-P0=000000}. As P5 is equal to 0, FF is reset prescaler divides input frequency by 8. Suppose we want the PLL to work in 6th frequency channel and we load the number of 6 on C4-C0. Input signal is applied and P counter increases until the value of P counter reaches the predefined C {P5-P0=1C4-C0}. In this value of P counter, output of XNOR blocks and P5 are logic 1 that causes FF to be set by A1 and A2 gates. After this time, the prescaler divide input frequency by 7 till the P counter reaches to value (111111) and next value is 000000. FF is reset by P5, prescaler returns to divide-by-8 situation and the cycle repeats again.

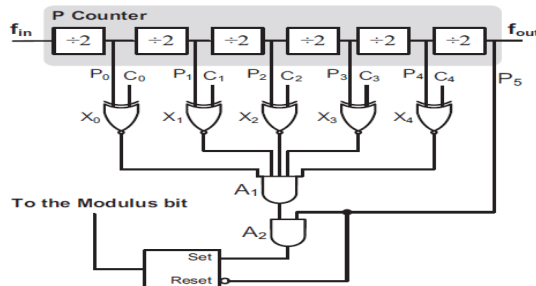


Fig.8 Integrated P&S counter

For predefined C value (1C4C3C2C1C0=C), prescaler divide input frequency by 8 and for rest of number (64 - C) it divides input frequency by 7. For a cycle we will have:

$$N = 8 * C + 7 * (64 - C) = 7 * 64 + C$$

$$f_{vco} = f_{ref} * N = 5\text{MHz} * (448 + C)$$

$$2405\text{MHz} \leq f_{vco} \leq 2480\text{MHz}$$

For $33 \leq C \leq 48$

IV SIMULATION RESULT

Simulation results are shown below,

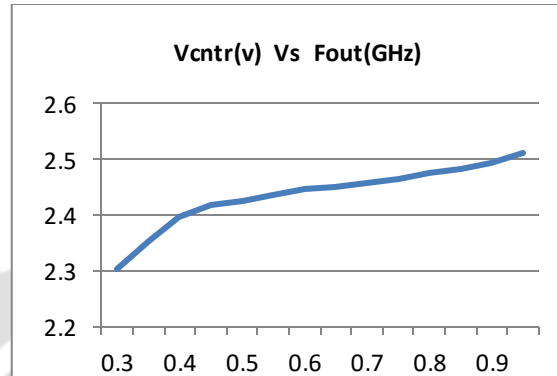


Fig.9 Vcntr(v) Vs Fout(GHz)

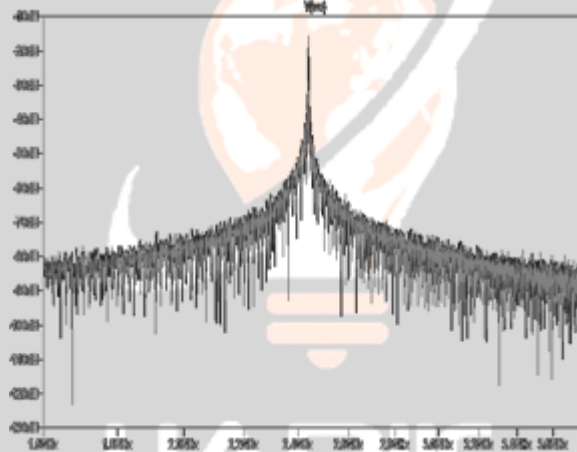


Fig.10 VCO output for Vcntr=0.25v

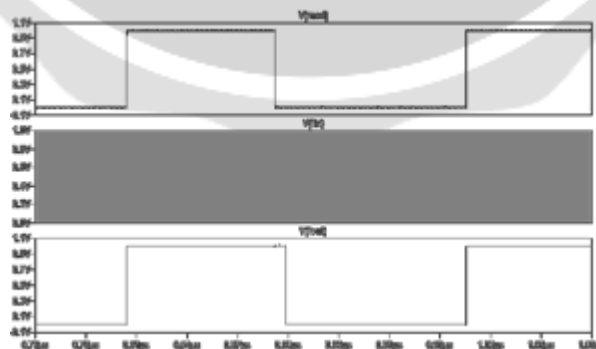


Fig.11 Divider output for c4c3c2c1c0=00001

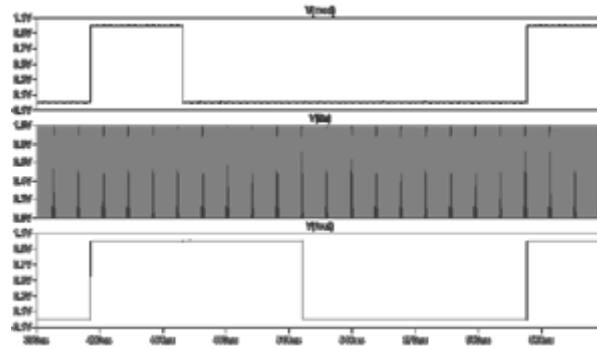


Fig.12 Divider output for c4c3c2c1c0=10000

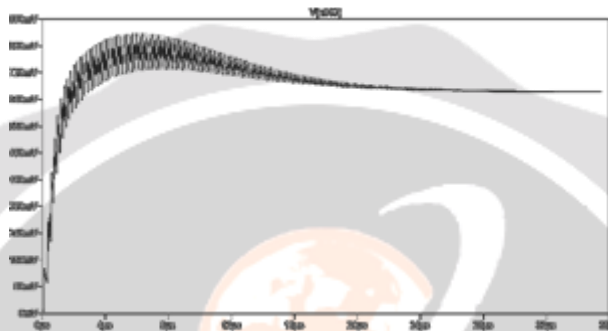


Fig.13 Ventr for VCO for c4c3c2c1c0=00001

V RESULTS

This research work focuses on the design techniques of PLL based frequency synthesizer low power requirement and performance of designed synthesizer is shown below.

Parameters	Value
Technology	45nm BSIM CMOS
Frequency band	2.4-2.5GHz(ISM)
Channel spacing	5MHz
Power dissipation	225.15uW
Power dissipation (divider)	29.01uW
Power dissipation (vco)	90.01uW
Settling time	42us

Table 1 : Performance parameters

Performance comparison is shown below.

Parameter	This Work	Ref[7]	Ref[]	Ref[6]
Technology	45nm	180nm	180nm	180nm
Frequency band	2.4-2.48 GHz	2.42-2.48 GHz	2.24-2.42 GHz	2.4-2.48 GHz
Reference frequency	5MHz	1MHz	25MHz	290 MHz
Channel spacing	5MHz	1MHz	--	--

Power dissipation	225.1uW	3.6mW	13.6mW	14.1mW
Power dissipation (divider)	29uW	0.6mW	--	--
Power dissipation (vco)	90.65uW	2.8mW	--	--
Settling time	34us	58us	--	--

Table 2 : Performance compression

VI – CONCLUSION

This research work focuses on the design techniques of PLL based frequency synthesizer for 2.4 GHz ISM frequency band with integer N division of frequency, low power requirement and lower phase noise by using proper design of programmable frequency divider and VCO, using CMOS 45nm technology results shows power dissipation of 225.1uW only and settling time of 42us, with channel spacing of 5 MHz.

ACKNOWLEDGMENT

The authors thanks Prof. A. K. Sisodia & Asst. Prof. Ami M. Patel. from L. J. Institute of Engineering and Technology for technical discussion & processing support without whom this paper would never be completed.

REFERENCES

PAPERS:

- [1]. Masoud Moslehi Bajestan, Eugene Foli, Hajir Hedayati, and Kamran Entesari “A 1.6GHz/4.8GHz Dual-Band CMOS Fractional-N Frequency Synthesizer for S-Band Radio Applications” IEEE Radio Frequency Integrated Circuits Symposium 2014 978-1-4799-3864-3/14 pp. 429-435.
- [2]. Xiaolong Liu, Lei Zhang, Li Zhang, Yan Wang, and Zhiping Yu “A 3.45-4.22 GHz PLL Frequency Synthesizer with Constant Loop Bandwidth for WLAN Applications” 978-1-4799-4132-2/14 2014 IEEE pp. 745-752.
- [3]. Jhin-Fang Huang, Wen-Cheng Lai and Chu-Hao Fu “A 2.4GHz Fractional-N Frequency Synthesizer with Noise Filtering Technique for Wireless Application” 978-1-4799 -4208-4/15 2015 IEEE
- [4]. Radu Gabriel Bozomitu, Vlad Cehan, Constantin Barabaşa, Neculai Cojan “A VLSI Implementation Of A Frequency Synthesizer Based On A Charge Pump PLL” IEEE 20th International Symposium For Design And Technology In Electronic Packaging (SIITME) 2014 978-1-4799-6962-3/14 pp. 141-145.
- [5]. Wen-cheng Lai, Jhin-fang Huang, Jia-lun Yang And Chieh Wen Shih “A Frequency Synthesizer With A Discrete-time Sample-hold-reset Loop Filter Dedicated To Implantable Medical Microsystems” 2014 7th International Conference on BioMedical Engineering and Informatics (BMEI 2014) 978-1-4799-5838-2/14 pp. 189-192..
- [6]. Sudip Shekhar, Daibashish Gangopadhyay, Eum-Chan Woo, and David J. Allstot “A 2.4-GHz Extended-Range Type-I $\Sigma\Delta$ Fractional-N Synthesizer With 1.8-MHz Loop Bandwidth and -110-dBc/Hz Phase Noise” IEEE Transactions On Circuits And Systems—ii: Express Briefs, Vol. 58, No. 8, August 2011 1549-7747 pp.472-476
- [7]. M.Vamshi Krishna, J.Xie, M.A.Do,C.C.Boon, K.S.Yeo and Aaron V.Do “A 1.8-V 3.6-mW 2.4-GHz Fully integrated CMOS Frequency Synthesizer for IEEE 802.15.4” 2010 18th IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC 2010) 978-1-4244-6471-5/10/2010 IEEE pp.387-391.
- [8]. Chin-Ying Chen, Jyh-Jier Ho, Wan-Rone Liou, and Robert Y. Hsiao “A 5.2GHz CMOS Fractional-N Frequency Synthesizer With a MASH Delta-Sigma Modulator” 978-1-4244-2167-1/08 2008 IEEE pp.738-742
- [9]. Mohammad Gholami, Hamid Rahimpour, Gholamreza Ardeshtir, Hossein MiarNaimi “Digital delay locked loop-based frequency synthesiser for Digital Video Broadcasting-Terrestrial

- receivers” IET Circuits Devices Syst., 2014, Vol. 8, Iss. 1, pp. 38–46
- [10]. Calogero Marco Ippolito, Alessandro Italia, and Giuseppe Palmisano “A 1.7-mW Dual-Band CMOS Frequency Synthesizer for Low Data-Rate sub-GHz Applications” 978-1-4244-6664-1/10/2010 IEEE pp142-145.
- [11]. Intissar Tohria, Rim Ayadi, Mohamed Masmoudi “ An Effective CMOS Charge Pump-Phase Frequency Detector Circuit for PLLs Applications ” 10th International Multi-Conference on Systems, Signals & Devices (SSD) Hammamet, Tunisia, March 18-21, 2013 ISBN 978-1-4673-6457-7 pp.1-7
- [12]. Yusuf Siddik “Design Of C-band Frequency Synthesizer For Fmcw Transmitter” Proceedings Of International Conference On Circuits, Communication, Control And Computing (I4c 2014) pp37-40
- [13]. Ali Sahafi, Jafar Sobhi, Mahdi Sahafi, and Omid Farhanieh “An Ultra Low Power Frequency Divider for 2.4GHz Zigbee Frequency Synthesizer” ELECO 2011 7th International Conference on Electrical and Electronics Engineering, 1-4 December, Bursa, TURKEY pp. 214-216
- [14]. Nesreen Mahmoud Hammam Ismail and Masuri Othman “Low Power Phase Locked Loop Frequency Synthesizer for 2.4 GHz Band Zigbee” American J. of Engineering and Applied Sciences, ISSN 1941-7020, 2009, pp. 337-343
- BOOKS:**
- [15]. Baker, Li, Boyce Circuit Design, Layout And Simulation 3rd Edn.1997,Wiley-IEEE Press ISBN 978-0-470-88132-3
- WEBSITES:**
- [16]. <http://www.linear.com/LTspiceIV>

