DESIGN OF CURRENT STARVED VCO USING POWER GATED INVERTER FOR PLL

Meenakshi Tiwari[1]

[1] *Assistant Professor, Electronics & Communication, St. Wilfred's Institute of Engg. & Technology Ajmer, Rajasthan, India*

ABSTRACT

From the basic topologies, a new current starved VCO topology is introduced using power gated inverter. A five stage CS VCO is designed and simulated in 180nm CMOS process in Tanner 13.0v. Current starved voltage controlled oscillator is simple ring oscillator consisting of cascaded inverters. Comparative analysis is done in terms of low voltage and low power consumption.

Keyword: - *Current starved VCO, low power, low voltage, power gated inverter*.

1. INTRODUCTION

Oscillators occur in many applications and make possible circuits and subsystems that perform very useful functions. In these oscillators, a voltage controlled oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits. They appear in many analog and RF signal processing systems. Wireless and optical communication systems have shown a explosive growth during the last few years. This exponential growth has driven the need for more compact, more cost-effective, fully integrated, low noise, low power voltage controlled oscillator (VCO) [1]. As the feature size getting smaller, CMOS technologies became attractive for the realization of high speed and less power ICs. Reducing power in phase lock loop is becoming essential for portable and battery operated compact electronic devices, which decreases the risk of reliability problems [2]. In recent years, the design of low power and low voltage PLL for the different application has become one of the greatest challenges in high performance very large scale integration (VLSI) design [3]. As today's integrated circuits are converging towards CMOS, the design of robust and high-performance CMOS oscillators, more specifically, voltage-controlled oscillators (VCOs), has become extremely important [4]. This paper presents the design of low power low voltage current starved voltage controlled oscillator by using low power technique. From the basic topologies, a new current starved VCO topology is introduced using power gated inverter.

2. CIRCUIT DESCRIPTION

2.1 Current Starved VCO

The most popular type of the VCO circuit is the current starved voltage controlled oscillator. In this circuit the number of inverter stages is fixed. The simple way to control the charge and discharge time of an inverter is to control the current through the inverter, via a voltage controlled current source, Vcrtl, as depicted in Fig. 1[5]. This current source is driven by the control voltage and the current will determine the charge up and discharge time of the inverter. This topology is called current-starved inverter, as the regular inverter is short of the current they are normally allowed to consume. With correct sizing and current levels, an odd number of stages of these current starved inverters can make a decent VCO. This design is simple and the oscillation frequency can achieve reasonably fast and due to the square law change in current levels in the footer device.

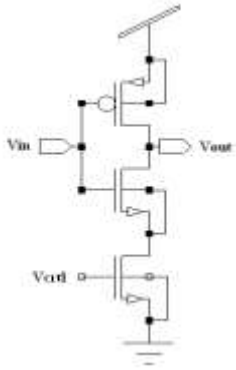

Fig -1: Current Starved VCO

However there are several problems with this design. First, the inverter doesn't work at very low bias voltages, such as zero, when the current in the inverter is been shut off. Second, the DC level of the VCO output is not constant; this can cause problems at high frequency when trying to amplify the VCO output to full swing. Third, the output of each stage drives two gates, which limits the maximum oscillation frequency [6]. The operation of current starved VCO is similar to the ring oscillator. Fig. 2 shows designed five stage Current-Starved VCO. Each delay cell consists of one pMOS and nMOS which operate as inverter, while upper pMOS and lower nMOS operate as current sources.

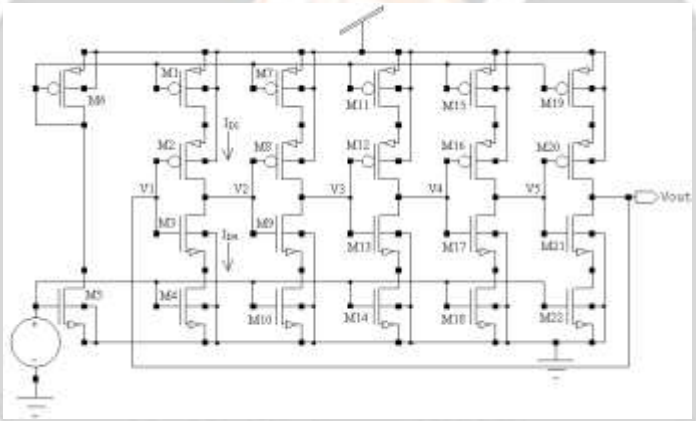

Fig -2: Schematic of 5 stage Current Starved VCO

The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first nMOS and pMOS are mirrored in each inverter current source stage. pMOS and nMOS drain currents are the same and are set by the input control voltage. There are different types of voltage controlled oscillators used in PLL, one is Current starved VCO. At high oscillation frequencies, the power consumption of the ring oscillators may not be low which is a key requirement for battery operated devices.

2.2 Current Starved VCO with Power Gated

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting of the flow of current to blocks of the circuit that are not currently in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling. An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. CMOS switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current. Leakage current consequently increases exponentially with reduction in threshold voltage. The leakage current is going to be a limiting factor for successive scaling down of transistors. Due to the smaller feature sizes in nanometre technologies, shorter channel lengths cause subthreshold current to increase when the transistor is in the off state. The lower subthreshold voltage gives

rise to increased subthreshold current as well, because transistors cannot be switched off completely [7]. Since with every successive technology the number of transistors per given area is on a rise, the leakage power in an integrated circuit for successive generations is increasing , because transistors leak even when they are not activated and significant power dissipation takes place even during inactive state of circuits. Thus it is essential to reduce static power during the idle or standby mode of operation of the circuits. In this work two approaches are used which reduce total power consumption of the circuit. This technique is used to cut off pull-up or pull-down or both networks from supply voltage or ground using sleep transistors [7]. We can size the footer device wider so that it doesn't affect the output swing much. Fig. 3 [7] shows the Power Gated Inverter technique using with Current Starved VCO.

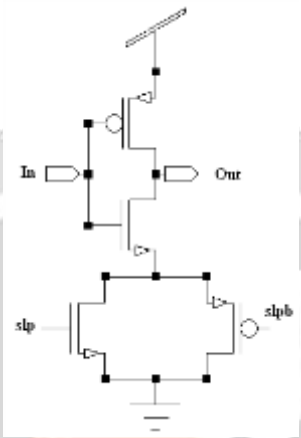

Fig -3 Power Gated Inverter

However there are several problems with this Current Starved VCO. First, the inverter doesn't work at very low bias voltages, such as zero, when the current in the inverter is been shut off. Second, the DC level of the VCO output is not constant; this can cause problems at high frequency when trying to amplify the VCO output to full swing. Third, the output of each stage drives two gates, which limits the maximum oscillation frequency [7].

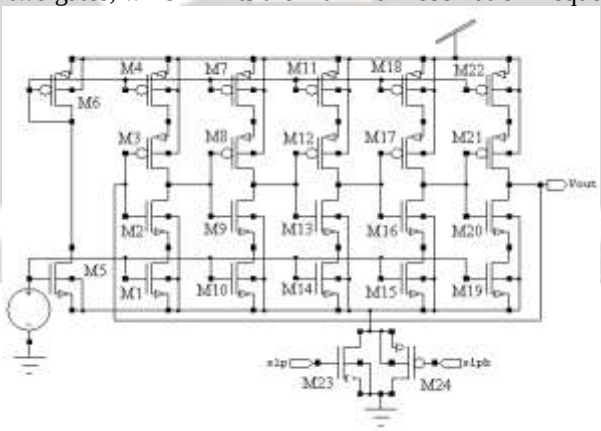

Fig -4: Schematic of 5 stage Current Starved VCO using Power Gated Inverter

Typically, high voltage sleep transistors are used for power gating. The sleepy inverter provides good leakage power reduction. The use of sleep transistors for leakage reduction, which are also called gated- V_{DD} and gated- GND techniques. When it enters into sleep mode it loses the state information. A different power gating technique is used in five stage current starved voltage controlled oscillator. This method is shown in Fig. 4. This technique provides low leakage and state retention at large total power consumption. Though this obtain results in good output during active mode [7].

3. SIMULATION RESULTS

3.1 Output Waveforms

Fig. 5 shows the output waveforms of current starved VCO at 1.1V VDD. The graph shown in Fig. 6 shows that the relationship between the DC bias voltage and Power Consumption. Fig. 7 shows the output waveforms of current starved VCO using power gated inverter at 1.1V VDD.

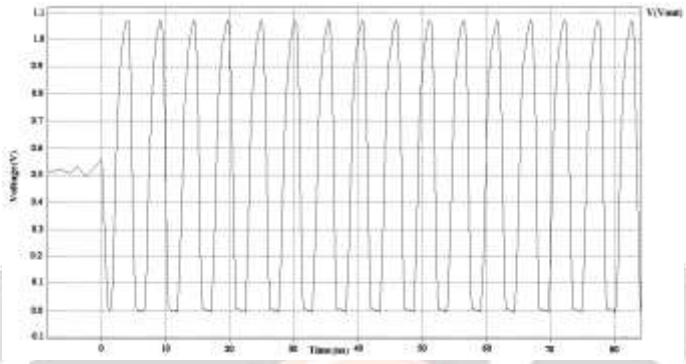

Fig -5: Waveform of 5 stage Current Starved VCO

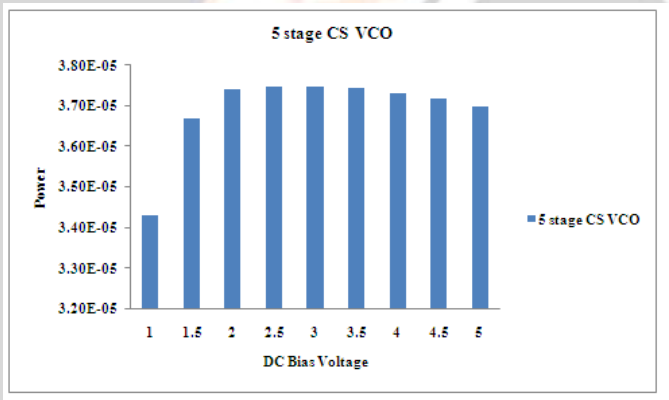

Chart -1: Shows the relation between DC Bias Voltage and Power consumption of CS VCO

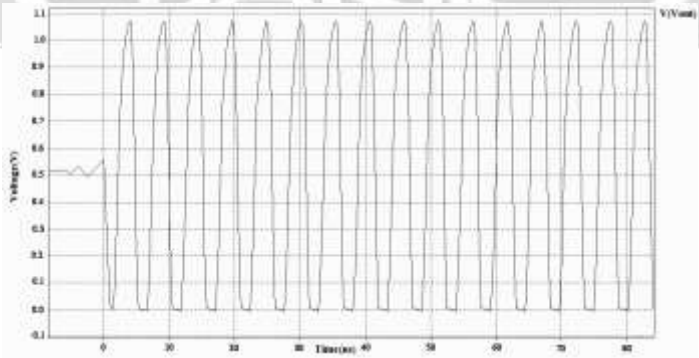

Fig -6: Waveform of 5 stage Current Starved VCO using Power Gated Inverter

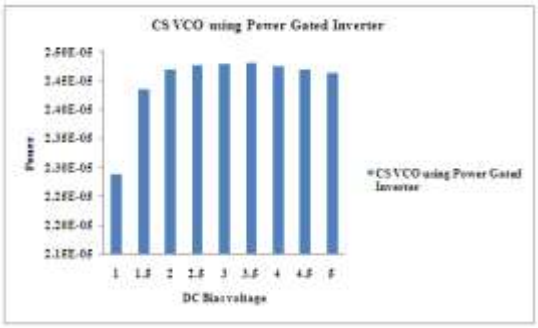

Chart -2: Shows the relation between Bias Voltage and Power consumption of CS VCO using Power Gated Inverter

3.2 Performance Comparison

Fig. 9 showing comparison, it is observed that two VCOs – Five stage Current Starved VCO and Current Starved VCO using Power Gated Inverter showing relationship in terms of power consumption and DC bias voltage and Current starved VCO using Power Gated Inverter consume less power than Current Starved VCO.

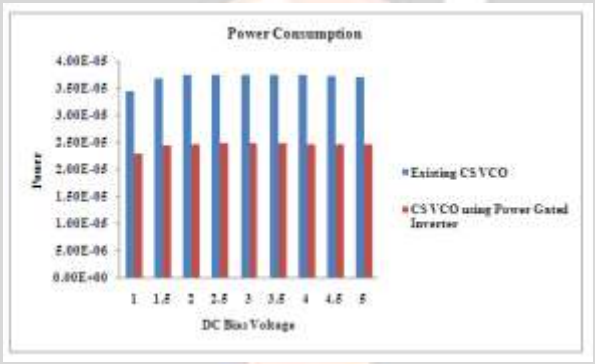

Chart -3: DC Bias Voltage Vs Power Consumption

4. CONCLUSIONS

Current starved voltage controlled oscillator have been designed using CMOS technology. From the graph showing comparison of power consumption, it is observed that two VCOs – Five stage Current Starved VCO and Current Starved VCO using Power Gated Inverter showing relationship in terms of power consumption and DC bias voltage. VCO have been improved using current starved voltage controlled oscillator and then transient analysis have been carried out to observe the less power consumption. Though there are many design requirements of a VCO, but the most important design among them is consume less power on the basis of which comparative study of VCOs is carried out. From Fig. 9, it is observed that the Current Starved VCO using Power Gated Inverter consume less power. Special attention has been given to the integration of design of Oscillators in order to achieve lower power when the design is implemented in an advanced CMOS process [8].

5. REFERENCES

[1] Jan M. Rabaey, "Digital Integrated Circuits", Second Edition, Pearson Education, 2003.
[2] R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation," *IEEE solid-state circuits second edition, 2005.*
[3] Bin Wan, "A design and design analysis of high performance voltage controlled oscillators," A thesis submitted by the Graduate School of Cornell University, 2006.

[4] B. Razavi, "Design of Analog CMOS Integrated Circuits," Fifth edition, McGraw Hill company, 2001.
[5] B.P. Panda, P.K. Rout, D.P. Acharya and G. Panda,"Design of a Novel Current Starved VCO via Constrained Geometric Programming," *International Symposium on Devices MEMS Intelligent System Communication,* April 12-14, 2011(ISSN 0975-8887) (ISBN 978-93-80747-80-2).
[6] Rashmi K Patil, M.A. Gaikwad, V.G. Nasre, "Area Efficient Wide Frequency Range CMOS Voltage Controlled Oscillator For PLL In 0.18um CMOS Process," *International Journal of Engineering Research and Applications (IJERA)* ISSN: 2248-9622, Vol. 2, Issue4, July-August 2012,pp. 1696-1699.
[7] Rajani H.P and Srimannarayan Kulkarni, "Novel Sleep Transistor techniques for low leakage power peripherals circuits," *International Journal of VLSI design & Communication Systems (VLSICS)* Vol.3, No. 4, August 2012.
[8] Rashmi K Patil, Vrushali G. Nasre, "Currant Starved Voltage Controlled Oscillator for PLL using 0.18um CMOS Process," *International Journal of Computer Applications,* 2012.