DESIGN OF HIGH PERFORMANCE, AREA EFFICIENT FIR FILTER USING CARRY SELECT ADDER

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ABSTRACT

Adders are the most widely used components in many data-processing processors to perform arithmetic functions. Carry Select Adder (CSLA) is known to be the fastest adder among the conventional adder structures. The main advantage of CSLA is its reduced propagation delay characteristics with increase in area .The area of the CSLA will be reduced by using a simple and efficient gate-level modification. The basic idea is to use ***Binary to Excess-1 Converter (BEC)*** *instead of RCA with cin=1 in the regular CSLA to achieve lower area .The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. Based on this modification 4,7,11 and 16 bit square-root CSLA (SQRT CSLA) architecture will be developed and compared with the regular SQRT CSLA and ripple carry adder architecture. The proposed design will reduce the area & delay as compared with the regular SQRT CSLA. Analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA. The high performance & area efficient carry select adder has been implemented in the design of FIR filter to improve the performance of filter.*

1. INTRODUCTION

Design of area - efficient high-speed data path logic systems is one of the most substantial areas of research in VLSI system design. Addition usually impacts widely the overall performance of digital systems and a crucial arithmetic function. In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes adders come in to the picture. As we know millions of instructions per second are performed in microprocessors, so speed of operation is the most important constraint to be considered while designing multipliers.

This brief is structured as follows. Section II presents the detailed structure of Ripple Carry Adder (RCA) and Carry Select Adder (CSLA). Section III presents the detailed structure and the function of the BEC logic. The 4-bit, 7-bit, 11-bit and the 16-bit Regular CSLA has been compared with the 4-bit, 7-bit, 11-bit and the 16-bit Modified CSLA. The comparison shows that the area and the delay of Modified CSLA have been reduced as that of Regular CSLA. The graphical comparison of area and delay are presented in Section IV. Finally, the work is concluded in Section V.

2.RIPPLE CARRY ADDER

The block diagram of n-bit ripple carry adder is shown in fig 1. In normal Ripple Carry Adder (RCA), the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. As carry ripples from one full adder to the other, it traverses longest critical path and exhibits worst-case delay.

Si = Ai xor Bi xor Ci

Ci+1 = Ai Bi + (Ai + Bi) Ci; where i = 0, 1, …, n-1

To reduce the propagation delay, we go for Carry Select Adder (CSLA).

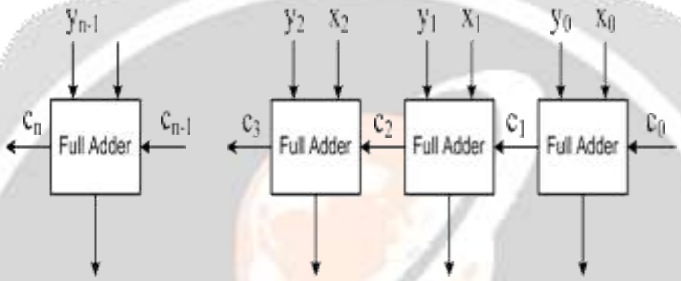

Fig -1: **n-bit ripple carry adder**

2.1 Carry Select Adder

The carry select adder comes in the category of conditional sum adder. Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 prior the input carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. The conventional carry select adder consists of k/2 bit adder for the lower half of the bits i.e. least significant bits and for the upper half i.e. most significant bits (MSB's) two k/bit adders. In MSB adders one adder assumes carry input as one for performing addition and another assumes carry input as zero. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of output carry and sum. The selection is done by using a multiplexer. This technique of dividing adder in to stages increases the area utilization but addition operation fastens. The block diagram of carry select adder is shown in fig 2

However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin =0 and Cin=1, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III.

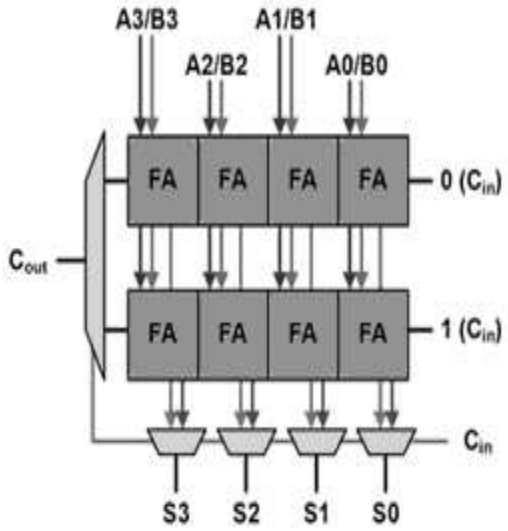

Figure 2: Carry Select Adder

2.2 BEC

The figure shows the logic diagram of 4-bit Binary to Excess-1 Converter (BEC's). The inputs are denoted as B0,B1,B2,B3 and the output's are represented as X0,X1,X2,X3 for an 4-bit BEC

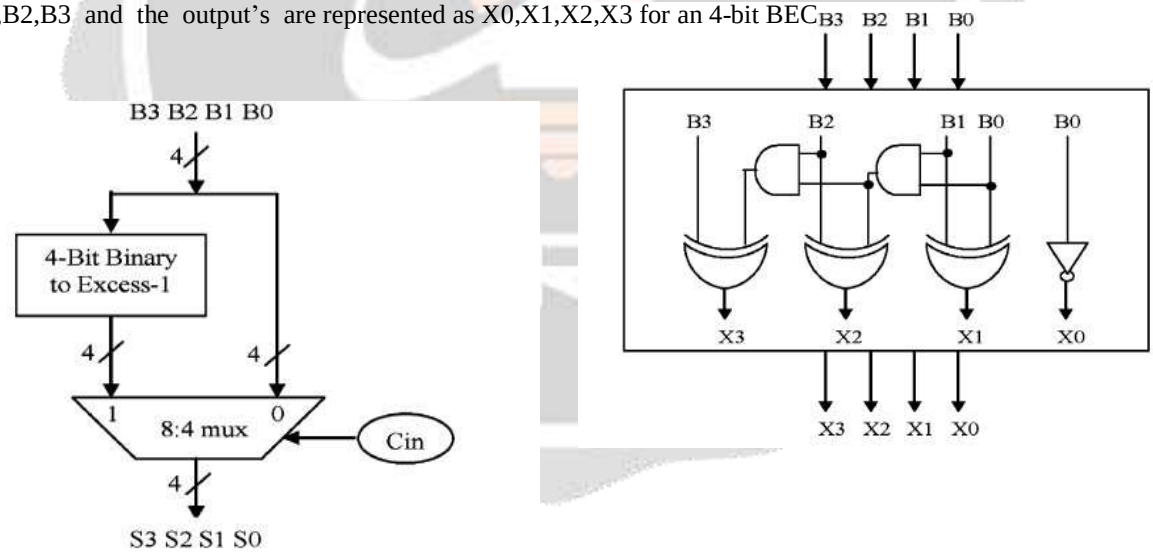

Figure 3: 4-bit BEC

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X0=~B0

X1= B0^B1;

X2=B2^(B0 & B1);

X3=B3^( B0&B1&B2)
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As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and the delay in the regular CSLA. To replace the n-bit RCA, an n- bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 4 and Table II, respectively. Fig. 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4- bit BEC is listed as (note the functional symbols ~ NOT, &AND, ^XOR)

3. REGULAR SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Figure **4. BEC with 8:4 mux**fig 5**Figure 4**. It has five groups of different size RCA. The carry output of first 2-bit RCA is given as a select signal for the multiplexer. The sum is individually calculated by considering input carry =0 & 1. Depending on the carry out from the first stage, either of the two outputs will be selected. The process continues until the entire 16-bit sum has been calculated. The 16-bit has been splitted into 2bit, 2bit, 3 bit,
4bit & 5 bit.

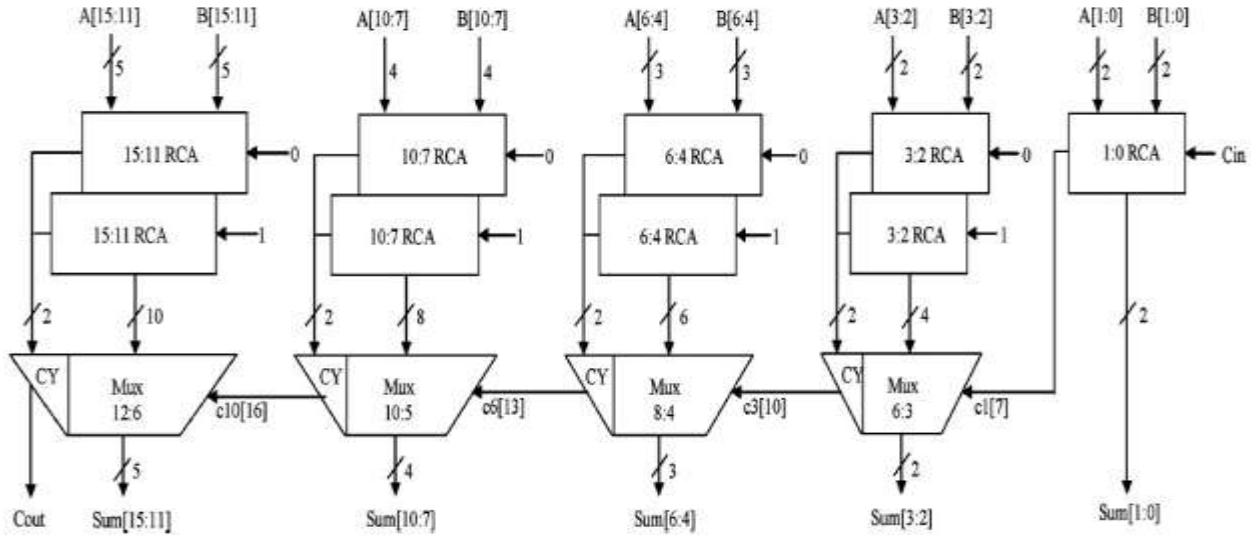


Figure 4: Regular 16-bit SQRT CSLA

3. 1 Modified 16-Bit SQRT CSLA

The structure of the 16-bit modified SQRT CSLA is shown in fig 6. Here, instead of RCA with Cin=1, a Binary to Excess-1 Converted has been used. The output of the normal RCA with Cin=0 is fed as an input to the Binary to Excess-1 Converter, where the output is one more than the output of RCA output. Depends on the input carry from the previous stage of RCA, the output either from the RCA with Cin=0 or the output from the Binary to Excess one Converter will be selected. The process is repeated until all the 16-bit has been summed up.

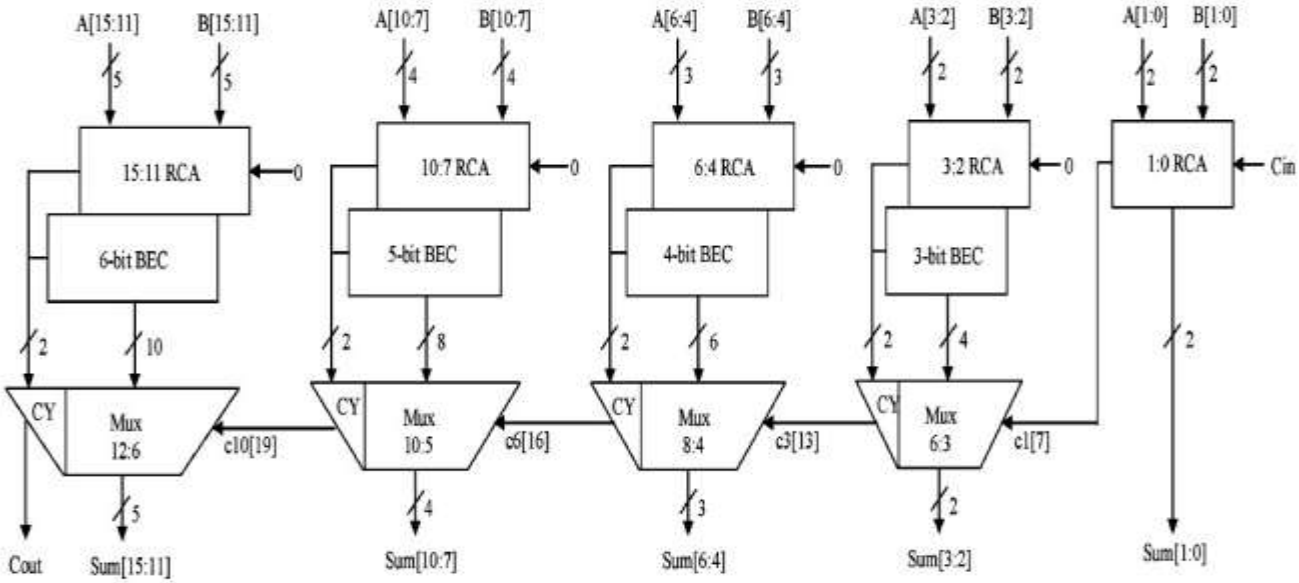
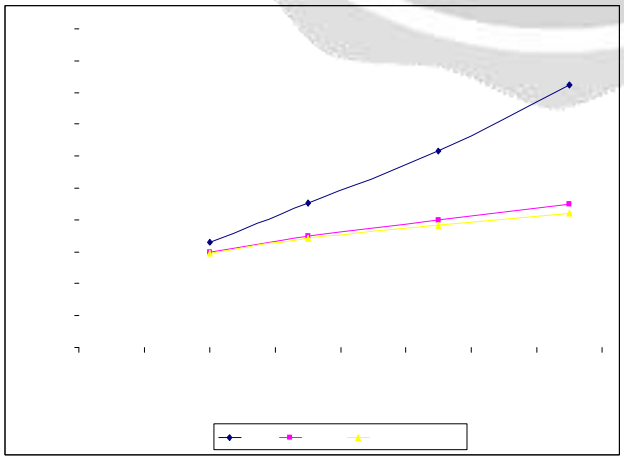
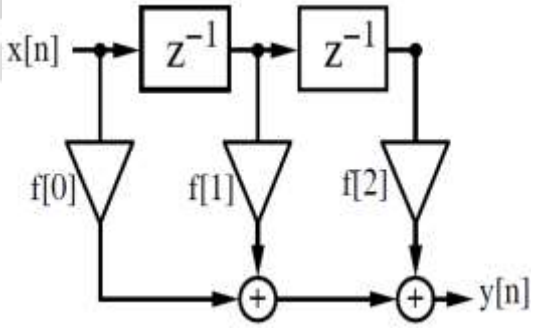


Fig -5: Modified 16-bit SQRT CSLA. The parallel RCA with Cin=1 is replaced with BEC





Graph 1:Delay Comparison of RCA, CSLA & Modified CSLA

Word Size	Adder	Area	Delay
4-bit	Ripple Carry Adder	4	9.926ns
	Regular CSLA	9	8.932ns
	Modified	8	8.876ns
8-bit	Ripple Carry Adder	8	13.616ns
	Regular CSLA	18	10.444ns
	Modified	14	10.242ns
11-bit	Ripple Carry Adder	13	18.536ns
	Regular CSLA	31	11.9488ns
	Modified	24	11.484ns
16-bit	Ripple Carry Adder	18	24.686ns
	Regular CSLA	47	13.535ns
	Modified	36	12.602ns

Comparison Table

4. CONCLUSION

A simple approach is proposed in this paper to reduce the area of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area . The compared results show that the modified SQRT CSLA has lower area & lower delay when compared with the regular SQRT CSLA.The modified CSLA architecture is therefore, low area, simple and efficient for VLSI hardware implementation. It would be interesting to test the design of the modified 128-b SQRT CSLA.

5. REFERENCES

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