Design Analysis and Implementation of Two Stage Operational Amplifier

Raj Kesarwani

Department of Electronics and Communication Engineering

ABES Engineering College, Ghaziabad

Rahul Pandey

Department of Electronics and Communication Engineering

ABES Engineering College, Ghaziabad

Sahil Agarwal

Department of Electronics and Communication Engineering

ABES Engineering College, Ghaziabad

Shailendra Bisariya

Department of Electronics and Communication Engineering

ABES Engineering College, Ghaziabad

Mudit Saxena

Department of Electronics and Communication Engineering

ABES Engineering College, Ghaziabad

Abstract - *The operational amplifier is regarded as the most crucial electronic component. This paper outlines the process for designing a two-stage CMOS operational amplifier (Opamp) and examine how different factors affect the Opamp design's properties. The primary focus of this study is the design of an optimum Opamp gain. Opamp specs are considered, including gain, phase margin, slew rate, power dissipation, and others, while keeping this as the primary consideration.*

The design and implementation of a two-stage CMOS operational amplifier, operating at ±1V supply voltage, are shown in this study. The simulation process is performed using an EDA program called Cadence Virtuoso, which uses 90nm technology. With a phase margin of 560 and a power dissipation of 38.02μW, the resultant gain is 84db.

Keywords- gain, Opamp, Cadence, 90nm Opamp, CMOS

I. INTRODUCTION

The most often utilized components in electrical circuits are operational amplifiers. They have a wide range of applications. They are utilized in comparators, filters, integrators, differentiators, and digital-to-analog converters. Scaling these devices to reduce size and power consumption is the primary problem in CMOS technology. Op-amps typically have two inputs and one output, and they can be configured in various ways, including but not limited to inverting and non-inverting amplifier configurations. This report's primary goal is to design and optimize size in order to boost 90nm technology's gains. This modulation results in increased operating frequency and efficiency. The challenge is in designing and implementing a two-stage CMOS Opamp while taking a number of constraints into account. The W/L ratio, which is tangentially related to gain, is the specification that serves as the goal in this work.

Nonetheless, a rise in gain maintains the device's stability and enhances performance.

II. BLOCK DIAGRAM OF TWO STAGE OPERATIONAL AMPLIFIER

According to the block diagram, it contains two stages: stage 1 is the differential amplifier, and stage 2 is the common source amplifier. The differential amplifier amplifies the differences between two input voltages by having two separate voltage inputs, vin+ and vin-. Since the first stage's gain is insufficient, a common source amplifier is used in the second stage.

As a result, the common source amplifier receives the differential amplifier's output and increases the gain even further. It incorporates a compensation circuit for times when the device is experiencing negative feedback in order to achieve low gain at high frequencies and preserve device stability.

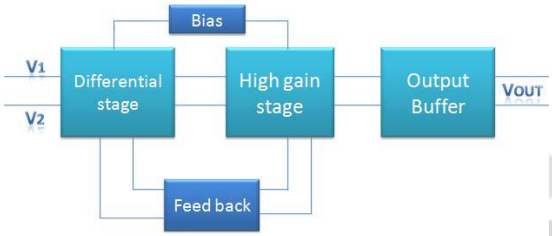


Fig.1. Block Diagram of Two Stage Opamp

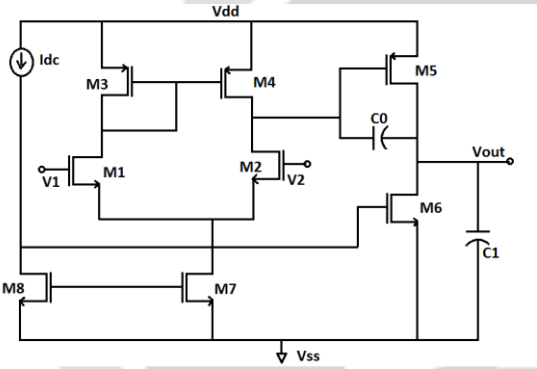


Fig.2. Circuit Diagram of Opamp

III. DESIGN PROCEDURE

We created a circuit in the cadence tool to determine the Vth and β effective values for NMOS and PMOS.

A. NMOS And PMOS Bias Circuit

To compute the values of βeff and Vth, we employ the NMOS and PMOS bias circuit.

To calculate μnCox and μpCox for βeff = μ at 90nm.Cox (W/L) where Cox is the oxide capacitance, μ is the electron mobility, and βeff is the MOSFET transconductance effective factor.

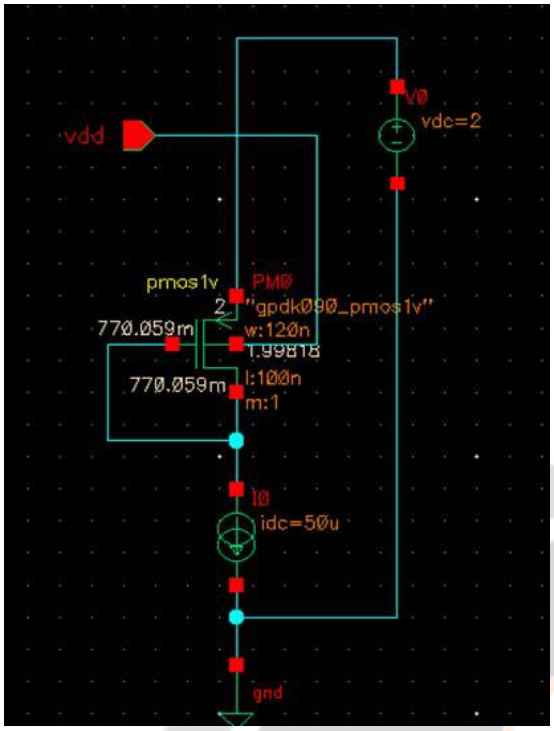


Fig.3. NMOS Circuit to find process information

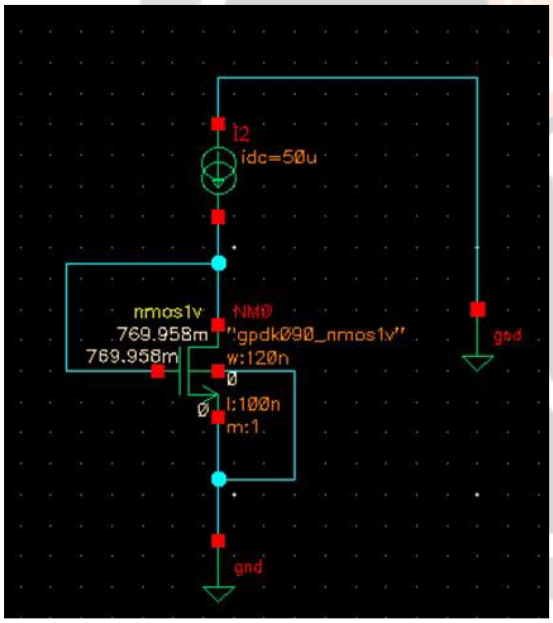


Fig.4. PMOS Circuit to find process information

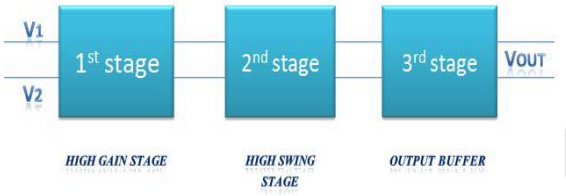
NMOS	PMOS
$\beta_{eff} = 432.025u$	$\beta_{eff} = 171.572u$
K=10	K=10
$\mu_n Cox = 285u$	$\mu_p Cox = 142u$
$V_{thn} = 148.938m$	$V_{thp} = -214.774m$

Table I. Vth and βeff values of PMOS and NMOS

B. Design of Opamp

Av defines the overall gain of a two-stage CMOS Opamp. The product of Av1 and Av2 yields the matching equation.

In this case, Av2 is referred to as the common source amplifier gain and Av1 as the differential amplifier gain.



Parameters	Specifications
Vdd	1.8V
Vss	-1.8V
Gain	80db
Bandwidth	5MHz
Slew Rate	5V/µsec
ICMR+	1.6V
ICMR-	0.8V
Load Capacitance	10pF
Power	3mV

Table II. Parameters and Specifications

C. Design Equations

The formula is as follows: Av = Av1. Av2. Where Av1=V01/Vin; nevertheless, for a common source amplifier, V01 = Vin2. Consequently,

Av2 = V0ut/V01

gm2 = √(2β2 Ids2) = √(2β1 * Ids1) = gm1
Iss/2=Ids1=Ids2
Therefore, gm1 = √ (β1*Iss).

Ids2 travels through M2 and M4, whereas Iss splits through MOSFETS M1 and M3.
Considering that M1 and M2 are the same, gm1 = gm2.

First, let's discuss the stability criterion:
It has been found that the phase margin needs to be larger than 45˚ in order to meet stability requirements.

gm6 /C0≥2.2 (gm1/C1)
C0>(2.2* gm1* C1)/ gm6

$gm1/ gm6 \leq 0.1$

$C0 \geq 0.22.C1$ (1)

The obtained relation of C1 and C0 as

$C1 \geq 0.22C0$

so,C0=2.5pF (2)

From slew rate

$(dV0/dt) \geq 10v/\mu secs$

$=>C0*(dV0/dt)=IDS7$

$IDS1= IDS2=ISS/2$

Neglecting λ from saturated transistor current,

$Vgs=Vt \sqrt{(2 Ids/\beta(W/L))}$ (3)

ICMR evaluation

$Vinmin=Vss + Vdsat7 + Vgs1$ (4)

$=Vss+Vdsat7+ Vt1+\sqrt{(2 Ids1/\beta(W/L)1)}$

$Vinmax=Vdd-Vt3 -\sqrt{(2 Ids3/\beta(W/L))3-Vds1+Vgs1}$ (5)

$=>Vdd-Vtp3-\sqrt{(2 Ids3/\beta(W/L)3)+Vtn3}$

By using Vdsat=Vgs-Vt relation,

$=>Vdd-Vtp3+Vtn1-\sqrt{(2 Ids3/\beta(W/L)3)}$ (6)

By substituting for Vdd, Vtp, Vtn and Ids3, (W/L)3 is obtained.

Hence (W/L)3=(W/L)4 (7)

Evaluation of (W/L)1 and (W/L)2

Given,

GBW= gm1/C1= gm2/C0 (8)

$gm1= gm2=\sqrt{(2 Ids1.\beta(W/L)1)}$

Therefore (W/L)1 is obtained

Hence, (W/L)1=(W/L)2.

Evaluation of (W/L)7

As known from the equation,

$Vinmin=Vdsat7+Vss+Vt1+\sqrt{(2 Ids1/\beta(W/L)1)}$

(W/L)7 is obtained.

Evaluation of (W/L)8

dIds8/dVgs8= gm8 (9)

$=>\beta p8.(Vgs8-Vt8)$

$= >\beta p8.Vdsat8$

Therefore,

$(W/L)8= gm8/(\beta p8* Vdsat8)$

So, first evaluate Vdsat8

Voutmax= VDD- Vdsat8 (10)

Vdsat8= VDD- Voutmax

So, (W/L)8 is obtained.

Similarly, (W/L)3= (W/L)4,

(W/L)7= (W/L)8

Using the above equations calculated (W/L) values for all MOSFETS are listed below.

MOSFETS	Theoritical values (W/L)
M1	7
M2	7
M3	84
M4	84
M7	9
M8	9

Table III. Theoretical Values for MOSFETs

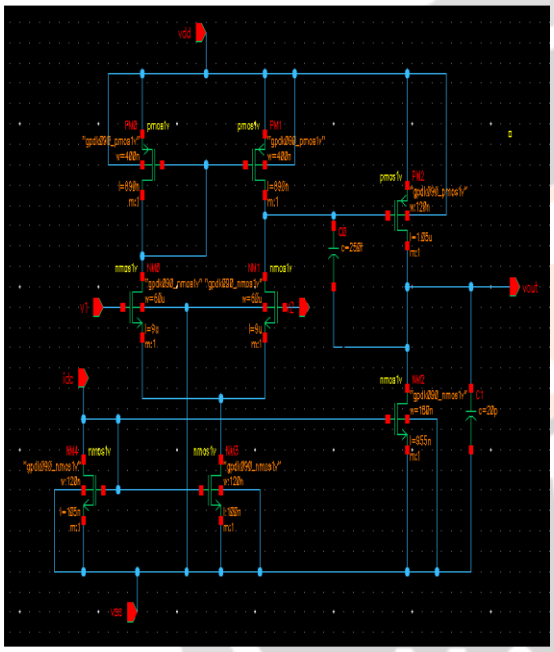


Fig.6. 90 nm Technology Opamp Circuit Diagram

IV. RESULTS

Using 90nm technology in the cadence tool, a two-stage CMOS OPAMP has been designed and optimized to boost the gain. The device's numerous parameters are restrictions and minimal parameter changes result in the modified gain. Additional resizing is carried out by utilizing theoretical values.

Additionally, Fig. 8 illustrates how changing the W/L ratios of MOSFETs, as indicated in Table IV, improves the flexibility of this two-stage CMOS Opamp gain.

MOSFETS	Practical values (W)	Practical values (L)
M1	60u	9u
M2	60u	9u
M3	400n	890n
M4	400n	890n
M5	120n	1.05u
M6	180n	955n
M7	120n	100n
M8	120n	100n

Table IV. MOSFETs W/L ratio is realized with reference to the table III theoretical values for 84 dB gain

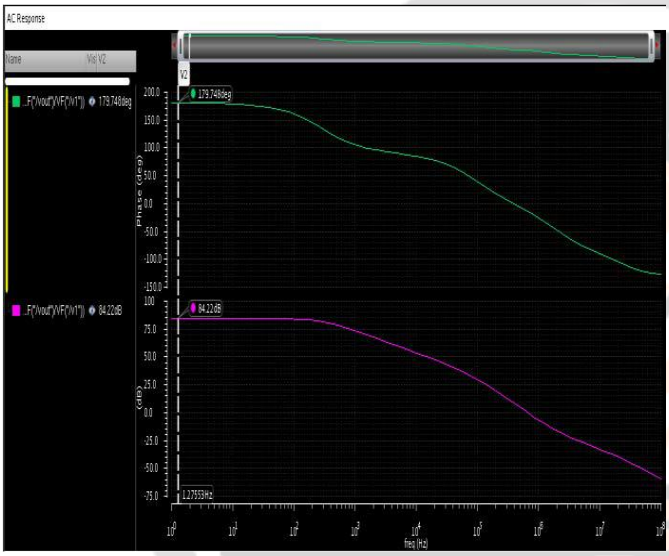


Fig.8. Frequency response of Opamp representing gain bandwidth of 90 nm and a gain of 84 dB.

V. CONCLUSION

The 90nm technology Cadence tool was used to perform the simulation. The gain has been raised through parameter optimization, such as (W/L) value selecting and properly sizing the circuit's structure using the design formulae.

Under a unity gain feedback setup, the system achieves an 84dB gain, a 560 phase margin, and a 38.02µW power dissipation.

VI. REFERENCES

[1] B. Razavi, “Design of Analog CMOS Integrated Circuits”, New York: Mc-Graw Hill, 2001.

[2] D. Johns and Ken Martin, “Analog Integrated Circuit Design”, Wiley India Pvt. Ltd, 1997.

[3] Boaz Shem-Tov, Mucahit Kozak, and Eby G. Friedman, “A High Speed CMOS Op-Amp Design Techniques using Negative Miller Capacitance, “proceedings of the 11th IEEE International Conference on Electronics, circuit and systems, December 2004.

[4] K. Bult and G.J.G.M. Geelen, “A fast-settling CMOS op amp for SC circuits with 90-dB DC gain”, IEEE J. Solid- State circuits, 1990, Vol. 25, No. 6, December, pp. 1379-1384.

[5] Rajkumar S. Parihar, Anu Gupta "Design of a Fully Differential Two- Stage CMOS Op-Amp for High Gain, High Bandwidth Applications".

[7] Henil Langalia, Sarthak Lad, Mangesh Lolge and Surendra Rathod, "Analysis of two-stage CMOS Op-Amp for Single- Event Transients" International Conference on Communication, Information & Computing Technology (ICCICT), Oct. 19-20,2012, Mumbai, India, pp. 1-4.

[8] Sunil M.P and Hari Krishna Murthy, "Design and Implementation of 90dB-4mW Two Stage CMOS Operational Amplifier Using 180nm" 3rd International Conference on Electronics and Communication Systems (ICECS-2016) 25-26th, February 2016, Coimbatore, Tamilnadu, India