Design and Development of High Power Amplifier At 3.4 GHz For IRNSS

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ABSTRACT

This paper gives a step-by-step of the design, simulation and measurement of a Power Amplifier (PA) operating frequency from 2.5GHz to 4.5GHz. The design of Class A Power amplifier was performed in Agilent ADS and the performance was tested with SZA3044Z BJT.

Keyword: - *RF Power Amplifier, Bipolar Junction Transistor (BJT), IRNSS, High Gain, satellite transponder*

1. INTRODUCTION

In a communication satellite serving the earth, the transponder transforms the received signals into forms appropriate for the transmission from space to earth. The transponder may be simply a repeater that amplifies and frequency signals. In this paper, the technologies of the major transponder elements are presented and amplifying devices.

One of the key elements of any spacecraft transponder is the output transmitter, consisting of a high power amplifier (HPA) and the associated power supply. The amplifier is operated at or near saturation (maximum output power level) to attain a high overall efficiency of converting dc energy from the power supply into useful radio frequency (RF) energy that carries information.

The transmitter is required to amplify the wanted signal without distortions and without other impairments which would decrease the usefulness of the signal. Two types of amplifiers (transmitters) are in common use, electron beam devices (commonly TWTAs) and solid state power amplifiers (SSPAs). For the TWTAs, the electrical power supply is often required to supply a number of high voltages (in the multikilovolt range), which presents a series of technology and design challenges. show in fig 1.

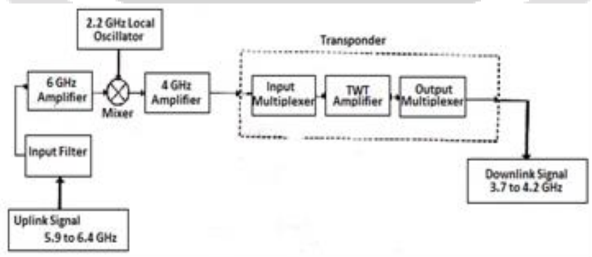


Fig -1 Transponder power amplifier diagram

2. DESIGN APPROACH

The wireless communications in satellite transponder increasing demands on systems designs. A critical element in Radio Frequency (RF) front ends is the Power Amplifier (PA). Main specifications for PA design include high linearity, better gain and efficiency. This paper describes the process of designing a single stage class A Power Amplifier for operation in the 2.5-4.5 GHz band.

The active device specified for this design was a *Rfmd SZA3044Z BJT*. Table I shows the performance specifications for the designed Power amplifier.

TABLE I

TARGET SPECIFICATION

Parameter	Symbol	Specification
Frequency range	f_o	2.5-4.5 GHz
Gain	S_{21}	≥15dB
Input return loss	S_{11}	≤ -10dB
Output return loss	S_{22}	≤ -10dB
Input/output Impedance	Z_0	50Ω
Output power	P_0	1W

3. STABILITY CONSIDERATION

Before PA design, it is important to determine the stability of the transistor. The stability of an amplifier is very important in the design and if not taken care, can create self-oscillation of the device due to reflected wave.

Amplifier is not reliable when it is unstable condition. The stability of a circuit is characterized by stability factor. The transistor is stable when K>1 and Δ<1.

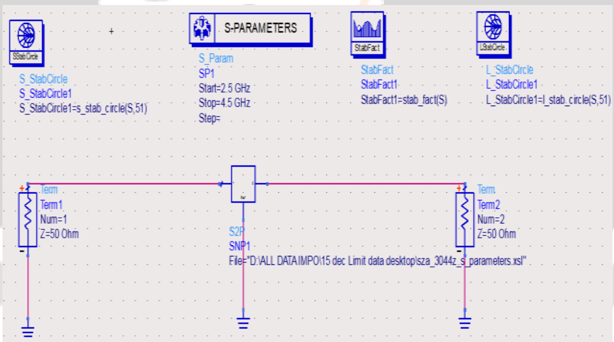


Fig 2- Stability simulation

After simulation ,the value of stability factor (K) is 6.673(K>1). So, now the transistor is in stable region.

STABILITY FACTOR, K (SHOULD BE >1)

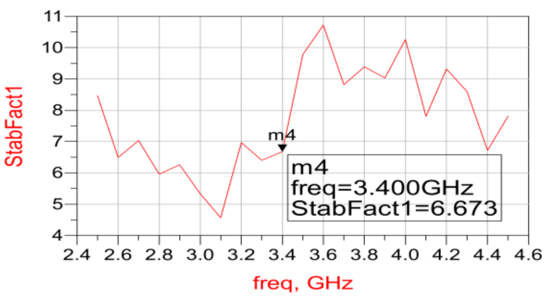


Fig 3- Stability result

4. MATCHING NETWORK DESIGN

Impedance matching is required to maximize the power transfer and minimize the reflections. Smith chart is used for impedance matching. According to maximum power transfer theorem, maximum power delivered to the load when the impedance of load is equal to the complex conjugate of the impedance of source (Z_S=Z_L*).

A.INPUT MATCHING NETWORK

The first set of measurements we are taken for S11 with the device mounted on the board and biased, but without matching networks. These measurements were de-embedded in ADS to obtain the input impedance at the device terminal.

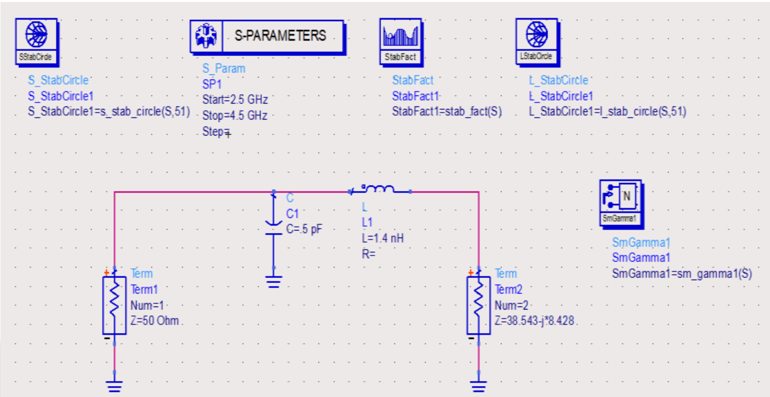


Fig 4- Input matching network

The circuit was then conjugate matched from this point to the 50Ω impedance presented by the trace line. The input matching network shown in Figure 3, was designed using the $S_m$gamma function in ADS. The input matching network uses a series inductor and parallel capacitor. A parallel capacitor is the value of 0.5pF and series inductor is the value of 1.4nH. A lumped component matching at 3.4GHz is a viable option but it would not provide the option of tuning.

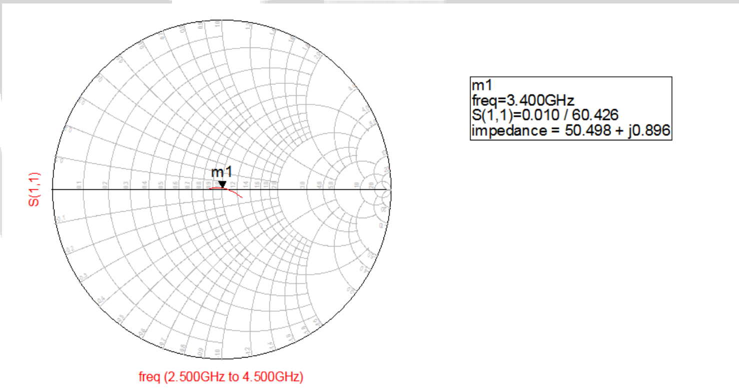


Fig 5- Input impedance result

B. OUTPUT MATCHING NETWORK

To design the output matching network, S22 of the biased, unmatched system was measured and de-embedded back to the device terminals. Simulations were then performed to determine the impedance presented to the drain that would maximize small signal gain. The matching network was designed in the same fashion as the input matching network.

This method gave several different optimal load impedances, indicating that trade-offs would be necessary to meet all specifications. The output matching network shown in Figure 5, was designed using the $S_m$gamma function in ADS.

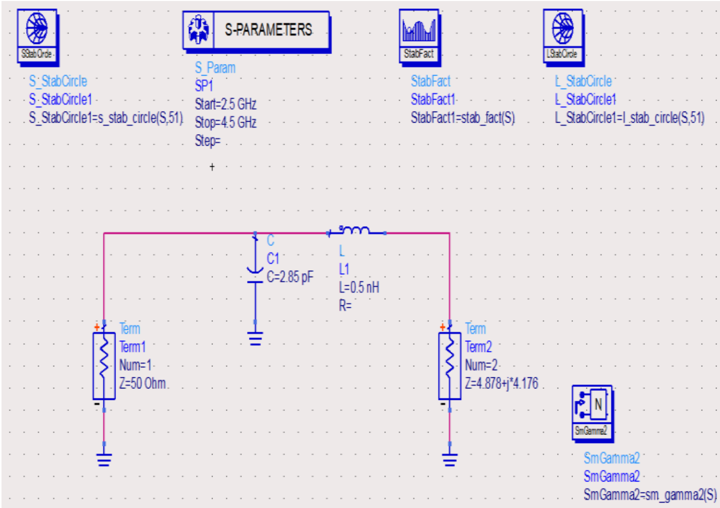


Fig 6- Output matching network

The output matching network uses a series inductor and parallel capacitor. A parallel capacitor is the value of 2.85 pF and series inductor is the value of 0.5nH. A lumped component matching at 3.4GHz is a viable option but it would not provide the option of tuning.

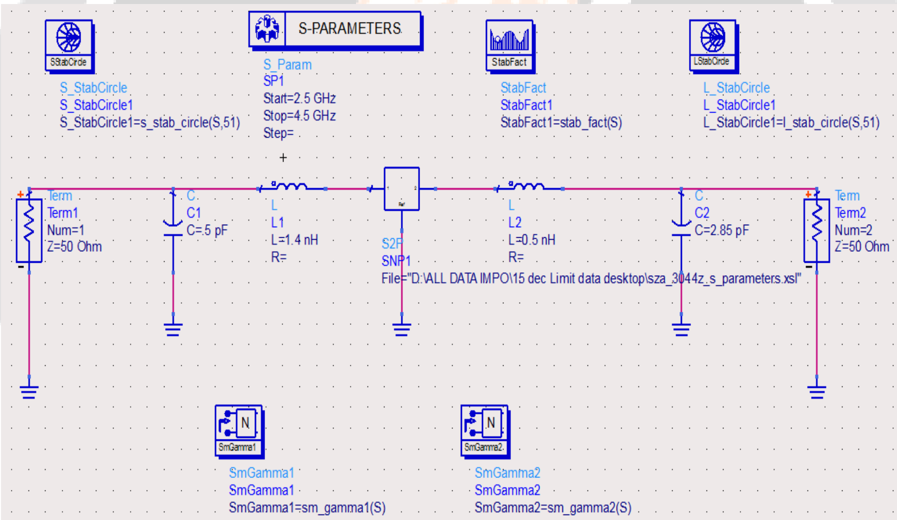


Fig 7- schematic of power amplifier with input output matching networks

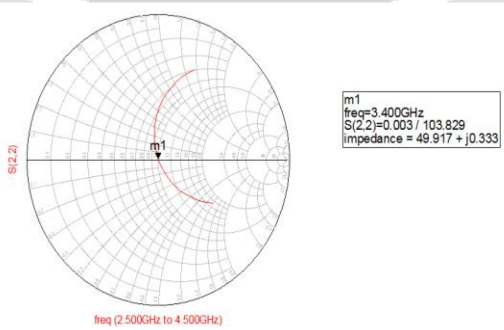


Fig 8- Output impedance result

INPUT RETURN LOSS AND OUTPUT RETURN LOSS

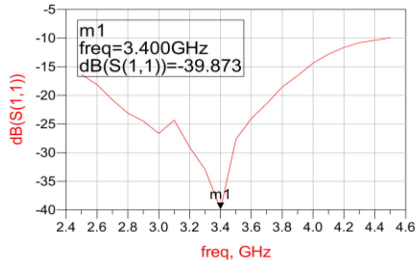


Fig 9-S11

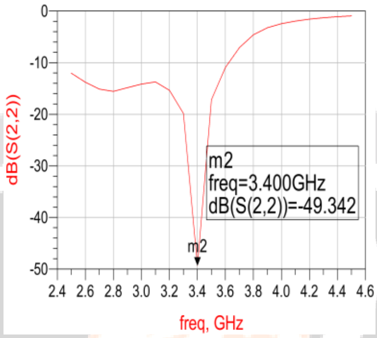


Fig 10- S22

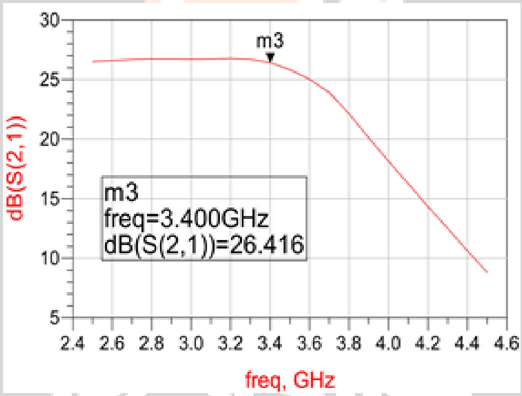


Fig 11- S21 Gain

5. BIASING NETWORK OF POWER AMPLIFIER

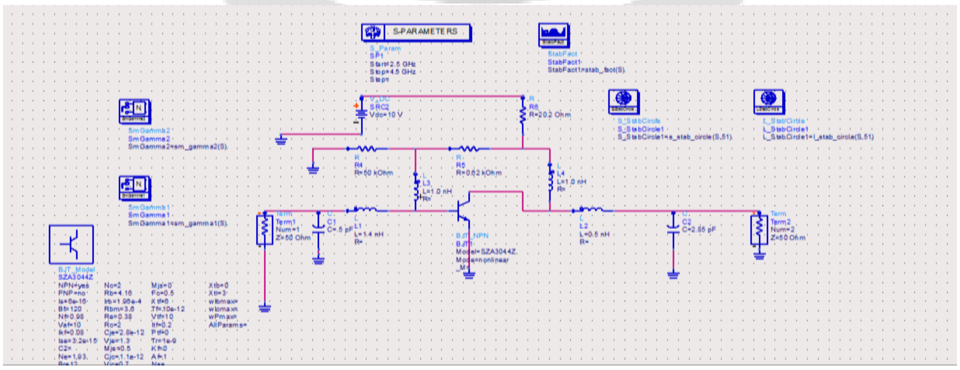


Fig 12- Biasing network of power amplifier

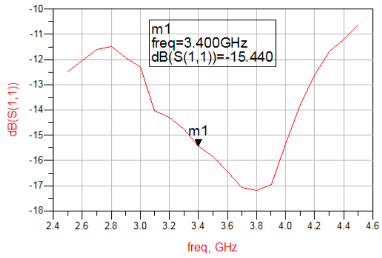


Fig 13 S11 After Biasing

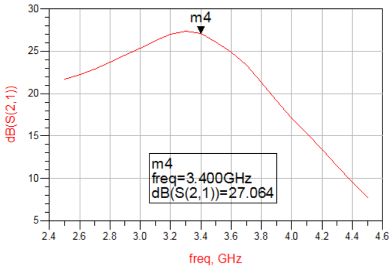
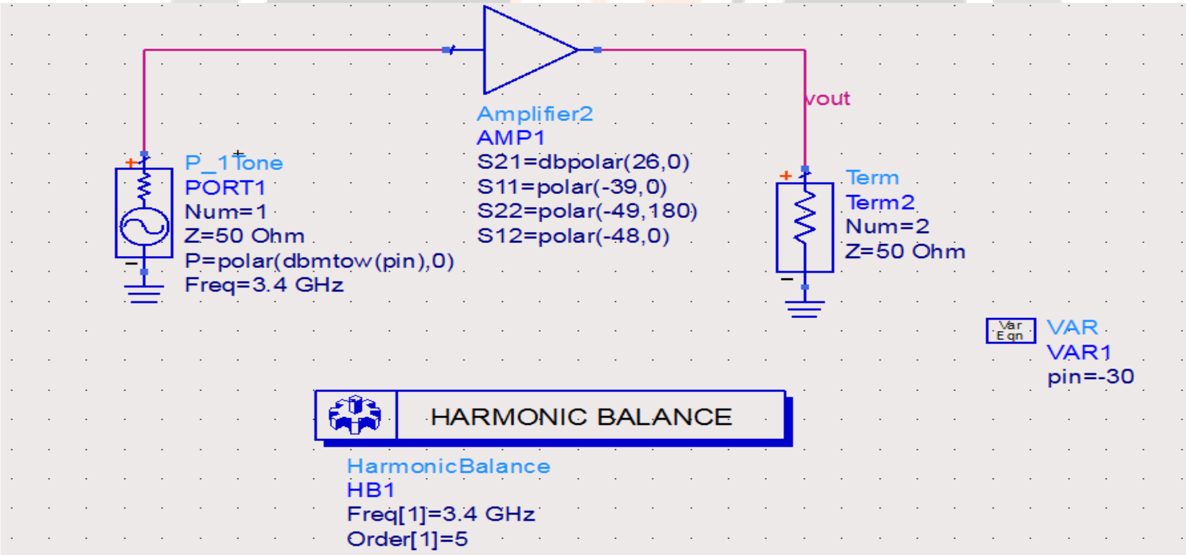


Fig-14 S21 After Baising Gain

6.HARMONIC BALANCE IN ADS:



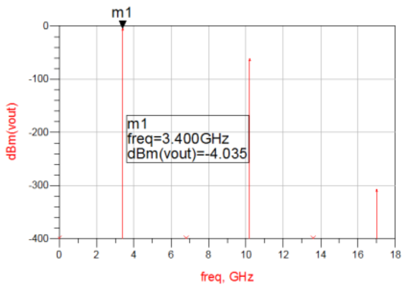


Fig 15 dBm(vout)

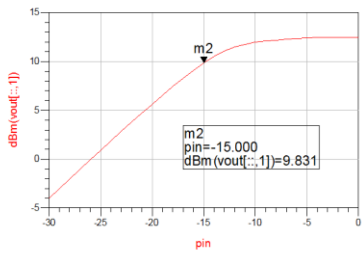


Fig 16 1st Harmonic

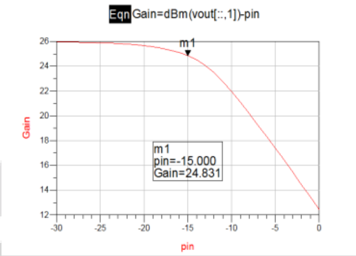


Fig 17 Gain Harmonic

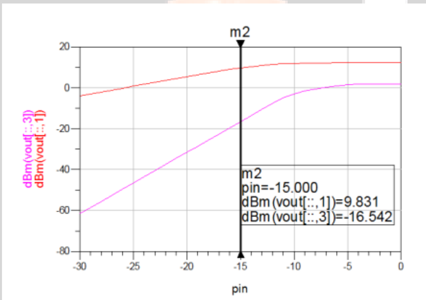


Fig 18 1st & 3rd Harmonic

7. MESURED RESULTS

Parameter	Symbol	Specification	Measured results After Impedance Matching	Measured results After Biasing Network
Gain	S_{21}	≥15dB	26.412dB	27.064dB
Input return loss	S_{11}	≤ -10dB	-39.873dB	-15.440dB
Output return loss	S_{22}	≤ -10dB	-49.342dB	-15.725dB
Input/output Impedance	Z_0	50Ω	50Ω	50Ω

CONCLUSION

The power amplifier presented here doesn’t meet many of the required specifications. Still a Stable Power amplifier with certain loss of power has been designed with proper matching networks. But working on this design provided a lot on insight into design of power amplifiers and the problems faced when the specifications require designs to be extremely competitive in terms of performance.

The choice of transistor in this power amplifier has influenced the design specifications in an unexpected manner. To make a power amplifier utilizing this device, a wide variety of matching networks should be explored along with an appropriate device modelling in ADS. Also Complete the Impedance Matching , Biasing Network , Harmonics Balance.

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