Design and Implementation of a low power high speed full adder cell for low power applications

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Abstract

An integral functional unit of every computational circuit, the one-bit full adder cell is one of the most commonly used digital circuit components in arithmetic logic units (ALUs). To date, a great deal of work has been done to enhance the architecture and functionality of complete adder circuit designs. This paper presents the implementation of two designs for 1-bit full adder cells at 90nm CMOS technology. One is conventional CCMOS 1-bit adder cell and other one is Transmission Gate Logic (16-T) are used in 1-bit full adder cells. The proposed adder cells outperform the existing adder cells in terms of power consumption, delay, and power delay product (PDP), according to the simulation results comparing the proposed and existing adder cells.

Keywords - Conventional Adder, CMOS Adder, Full Adder, Transmission Gate Full-adder Cell.

I. INTRODUCTION

The need for battery-powered portable electronic systems is growing daily because these devices must be powered by batteries in order to be portable. Therefore, when designing devices like laptops, tablets, cell phones, notebooks, and many other personal communication devices, speed and power consumption become the primary considerations. Power consumption is an important factor in VLSI technology. Increased power consumption raises the temperature, which shortens battery life and necessitates the use of a cooling fan to keep the circuitry cool. As a result, power consumption has an impact on both the system's overall cost and battery life. The adder circuit's performance and power dissipation have suffered as a result of the circuits' considerable increase in complexity in an attempt to shrink the chip's area. In order to minimise chip size and power dissipation, circuit design in low power VLSI design is a concern. MOSFET technology has two different forms of power dissipation: dynamic power dissipation and static power dissipation. A few parameters in static power dissipation, such as sub threshold leakage, reverse biased junction leakage, gate direct tunnelling leakage, and gate induced drain leakage, have a significant impact on different scaling parameters. Switching and short circuit power are the two main factors taken into account in dynamic power dissipation. The equations in (1) and (2), respectively, can be used to theoretically calculate the static and dynamic power dissipations.

P(static) = I_C * V_{dd} (1)

P(dynamic) = ^{1}2 C_L(ΔV_o^2)f (2)

Where V_{dd} is the supply voltage, C_L is the load capacitance, ΔV_o is the logic voltage swing, and f is the operating frequency. I_C Leakage current.

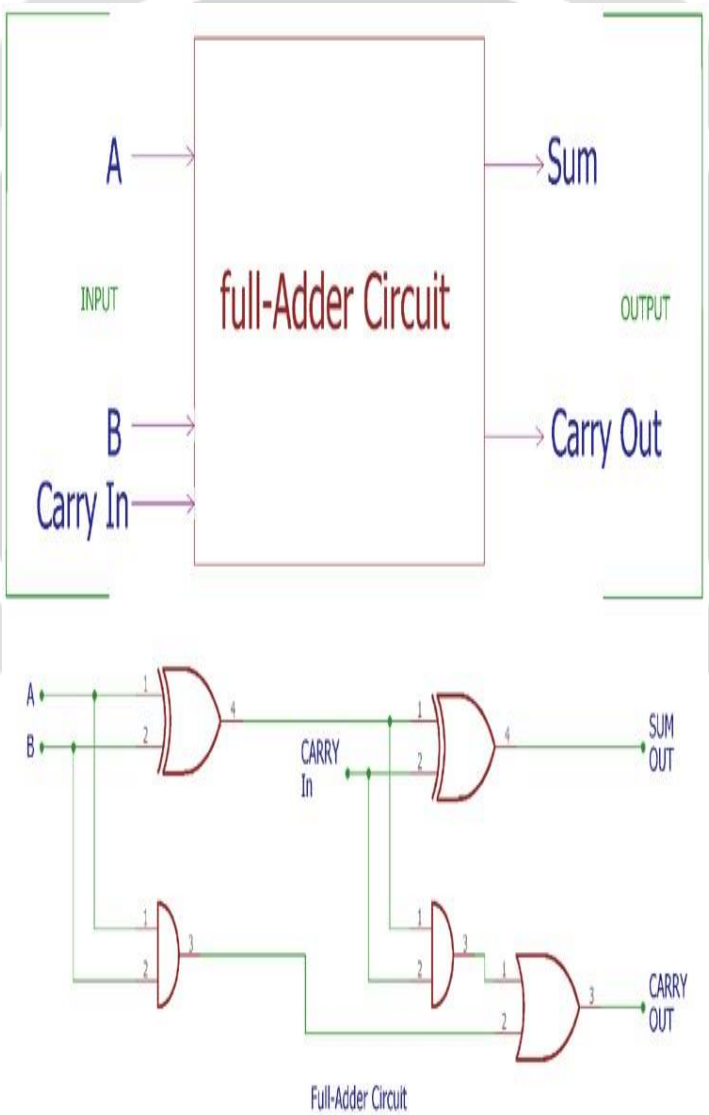
In this paper, different adder circuits are compared using the power delay product (PDP) parameter to estimate the optimised results at different operating frequency regions or at a single operating frequency. The power delay product can be computed theoretically using the following equation
(3).

PDP = P_{AVG}* T_D(3)

where T_D is Circuit delay and P_{AVG} is Average power dissipation.

II. LITRATURE SURVEY

Low power consumption, high speed, and compactness are some of the main goals that the C-CMOS Full Adder Cell design strives to accomplish. These can be accomplished by the cell through the use of complementary metal-oxide semiconductor (CMOS) technology, which makes use of both PMOS (P-type Metal Oxide-Semiconductor) and NMOS (N-type Metal-Oxide-Semiconductor) transistors. The optimisation of multiple metrics, including power consumption, delay, area, and robustness against process variations, is a common focus of C-CMOS Full Adder Cells. To increase performance and efficiency, various circuit topologies, transistor sizes, and layout strategies are investigated. In the realm of integrated circuit design, research on the Conventional C-CMOS Full Adder Cell is still ongoing and is vital to the creation of effective digital systems.



Full Adder Truth table

INPUTS			OUTPUTS	
A	B	C_{in}	SUM	CARRY $_{OUT}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1. C-CMOS Full Adder Cell

Based on the standard CMOS topology, the conventional C-CMOS 1-bit adder cell with 28 transistors is depicted in Fig. 1. Because so many transistors were used in the circuit's design, it has a high-power consumption and a longer propagation delay because the circuit's critical path includes five transistors in its forward path. The main benefit of this circuit design is that it produces full output voltage swing, which means it has a high noise margin and can operate reliably at low voltages. It also reduces short circuit current because it does not use complement of input signals.

Expression for sum and carry out

Sum = A'.B'.Cin +A'.B.Cin'+ A.B'.Cin'+
A.B.Cin (4)
$= (A \oplus B) \oplus Cin$ (5)

Carry out (Cout) = A'.B.Cin +A.B'.Cin+
A.B.Cin' +A.B.Cin(6)
= A.B + B.Cin + Cin.A(7)
$= (A \oplus B)\ Cin + (A \oplus B)'\ B$ (8)

Where A, B, and Cin are the binary input bits representing the two numbers to be added and the carry-in bit, respectively, and S and Cout are the binary output bits representing the sum and carry-out bit, respectively.

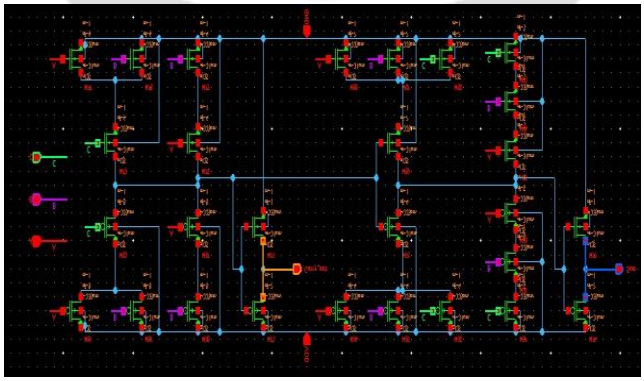


Fig.1. C-CMOS Full Adder Cell

(Conventional full adder cell)

2. Transmission Gate (16T) Full Adder Cell

The transmission gate is a parallel combination of nMOS and pMOS transistors with gates controlled by complementary voltages. An electrical switch known as a transmission gate is used to either selectively allow or prohibit signals. It consists of two gates: one that allows switching to occur and another that prevents it. The signal flows through when the gate is enabled and is blocked when it is disabled.
There are numerous benefits to building a full-adder circuit with a transmission gate. It first removes the requirement for any extra parts, like transistors or relays. Secondly, by shortening the signal path, power consumption is decreased and response times are improved. Thirdly, it makes switching operations quicker and design more effectively possible.

Expression for sum and carry out

Carry Propogate P= A ⊕ B
Carry Generate G=A.B

Sum = A'.B'.Cin +A'.B.Cin'+ A.B'.Cin'+
A.B.Cin
= Cin (AB + A'.B') + Cin'(A'.B+ A.B')
Let x= A ⊕ B , x'= A ⊙ B

Sum= Cin . x' + Cin'. x= x ⊕ Cin
= P ⊕ Cin

Carry Out (Cout)= A.B + B.Cin+ ACin
= AB + Cin(A+B)
=G + P Cin

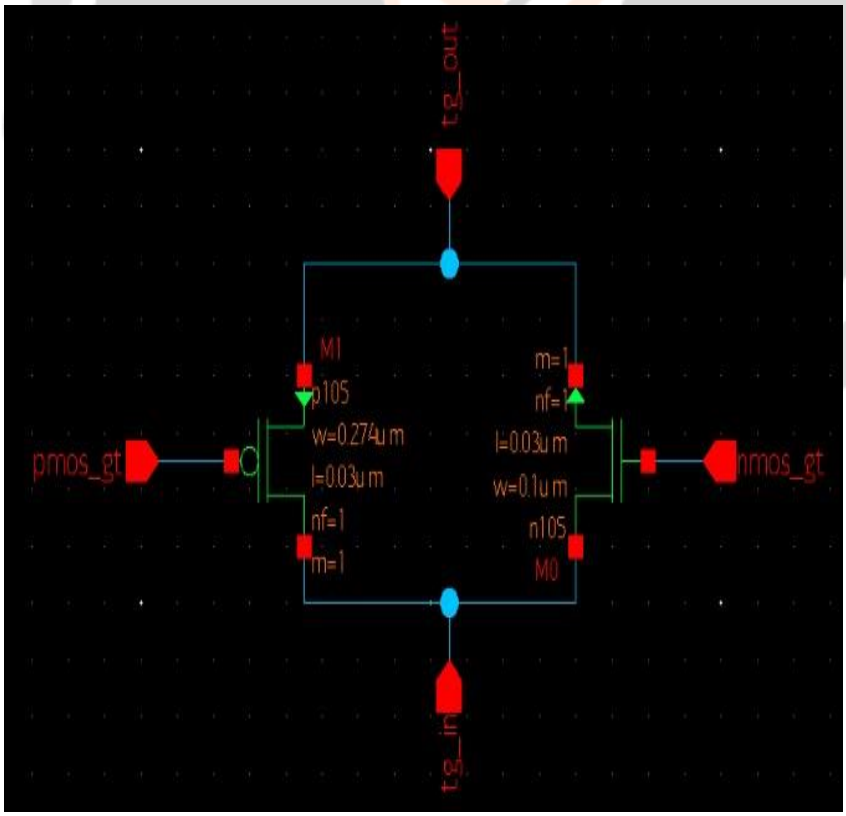


Fig.2.Transmission Gate

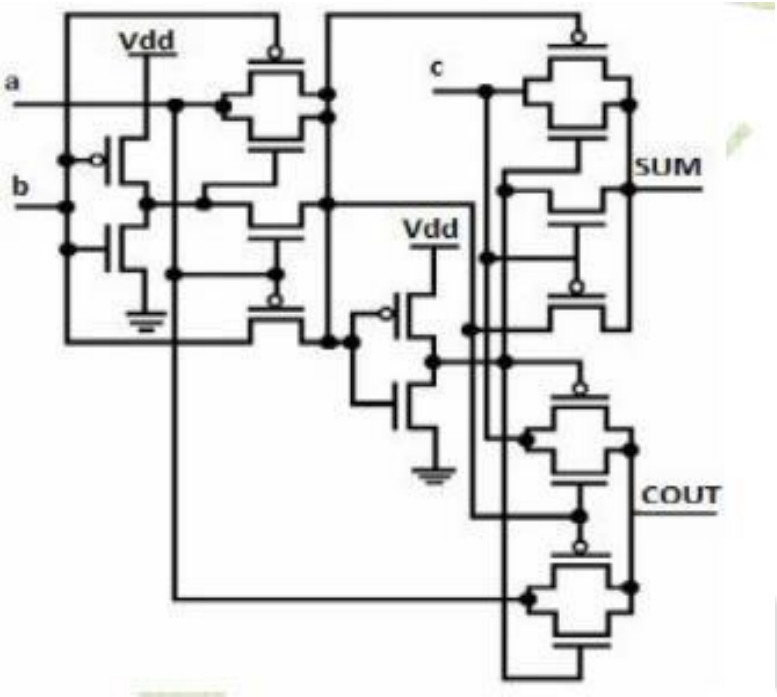


Fig .3. Full adder circuit using transmission gates

3. PERFORMANCE TABLE

SR. NO	Parameter	CMOS	TGL
1	Technology	90nm	90nm
2	Supply Voltage	1.2V	1.2V
3	Power	1037nw	715.7nw
4	Layout Area	128.32μm^2	85.42μm^2

4. RESULTS

Using 90nm technology in the cadence tool, a Transmission Gate (16T) Full Adder Cell has been designed and optimized to boost the power. The device's numerous parameters are restrictions and minimal parameter changes result in the modified power. Additional resizing is carried out by utilizing theoretical values. Additionally, it illustrates how changing the W/L ratios of MOSFETs, as indicated in, decrease the area of the circuits.

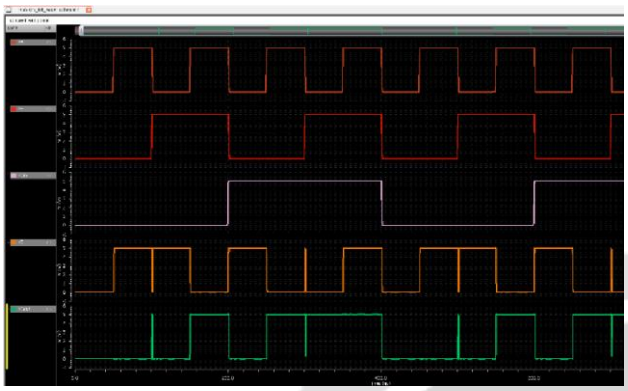


Fig.3. Output

5. CONCLUSION

The Virtuoso tool was used to generate simulation results for two complete adder circuits that were discussed in this paper. The results were then compared with adder circuits that are currently in use at 90nm CMOS technology. The simulation results show that, in comparison to a c-cmos full adder cell, which has a power saving of 1037nw, the suggested designs have achieved a maximum power saving of 715.7nw.

6. REFERENCES

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