Design and Simulation of Low Noise Amplifier at 3.4GHz for Receiver Terminal of Satellite Transponder (IRNSS)

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ABSTRACT

This paper describes the design and simulation of a single stage Low Noise Amplifier (LNA) at 3.4 GHz frequency. The single stage amplifier is designed by using MGF4941AL super –low noise InGaAs HEMT. This low noise amplifier (LNA) is design for application of Receiver Ground Station in Ranging Transponder of Indian regional navigation satellite system (IRNSS). The key points are analysis device's stability with Stability factor and the input and output impedance matching with Smith Chart and Tuning. Finally, the performance parameters of LNA were obtained with the simulation of S parameters. The target simulation are gain (S_{21}) with >15dB, noise figure with <2dB, Input and output return loss <-10dB. A single stage LNA has successfully designed with 17.112dB forward gain (S_{21}), 1.811dB noise figure, -13.215dB input return loss (S_{11}), -10.466dB output return loss (S_{22}) by ADS software.

Keywords- *low noise amplifier (LNA); ADS software; noise figure; optimization design; IRNSS;*

1. INTRODUCTION

The low-noise amplifier (LNA), one of the most important blocks in a receiving system, governs the receiving sensitivity of the entire system. Most of the radio frequency (RF) and microwave LNAs are designed in CMOS, BiCMOS, GaAs FET and p-HEMT technologies, and are used in a variety of applications including wireless communication, radio astronomy, RADAR etc.

The requirement of the LNA originates mainly to have the lowest possible noise figure (NF) with a reasonable gain. The general topology of an LNA consists of three stages: the input matching network (IMN), the amplifier itself and the output matching network (OMN). In addition to selection of the appropriate active component, the IMN and OMN are the critical factors in achieving the specified overall amplifier performances.

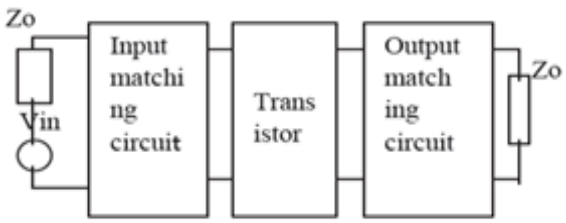

Figure 1 Block diagram of single stage LNA

This paper presents the design of a single stage LNA working at 3.4 GHz. The circuit design starts with the selection of proper active device for the frequency band of interest. For design and simulation purposes, Advanced Design System (ADS) provided by Agilent Technologies, is used. The S-parameters and noise parameters of the device are included in simulation file.

2. LNA DESIGN

In the designing of low noise amplifiers, the important goals are minimizing the noise figure of low noise amplifier, producing higher gain, lower power consumption and providing good input and output matching.

2.1. Transistor Selection

In this paper, InGaAs HEMT transistor has been chosen for designing the low noise amplifier. Gallium arsenide is preferred over silicon due to its superior performance at microwave frequencies. It has low noise provides enough amplification and minimum degradation of signal-to noise ratio (SNR).

LNAs are used in various applications like, Cellular Handsets, GPS Receivers, Cordless Phones, and Wireless LANs, Wireless Data, and satellite communications etc. Low noise amplifiers are used in many systems where low-level signals must be sensed and amplified.

In LNA design it is necessary to compromise its simultaneous requirements for high gain and low noise figure, stability, good input and output matching. The proposed low noise amplifier design is carried out with a systematic procedure and simulated by Advanced Design Systems (ADS) designed by Agilent.

TABLE 1 SELECTION OF TRANSISTOR

MGF4941AL	
Company Name	Mitsubishi
Technology Used	Low noise GaAs HEMT
Frequency Band	S-Band(3.4GHz)
Gain(S_{21})	14.618dB
Noise Figure	0.916dB

2.2. Stability Consideration

Before LNA design, it is important to determine the stability of the transistor. The stability of an amplifier is very important in the design and if not taken care, can create self-oscillation of the device due to reflected wave.

Amplifier is not reliable when it is unstable condition. The stability of a circuit is characterized by stability factor. The transistor is stable when K>1 and Δ<1.

TABLE 2 CRITERIA FOR STABILITY

Stability	Criteria
Unconditionally stable	$K>1 \& \lvert\Delta\rvert<1$
Potentially unstable	$K>1 \& \lvert\Delta\rvert>1$ or $K<1 \& \lvert\Delta\rvert<1$

Rollet's condition,

$$Stability\ Factor\ K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

$$Delta\ factor\ \Delta = S_{11}S_{22} - S_{12}S_{21}$$

TABLE 3 S-PARAMETERS OF TRANSISTOR

Parameter	Magnitude	dB
S_{11}	0.910∟-46.66°	-0.817∟-46.66°
S_{12}	0.044∟58.34°	-27.052∟58.34°
S_{21}	5.381∟129.6°	14.618∟129.6°
S_{22}	0.600∟-34.86°	-4.431∟-34.86°

The value of stability Factor (K) is 0.354(K<1). So, the transistor is unstable.

2.3. Transistor Stabilization

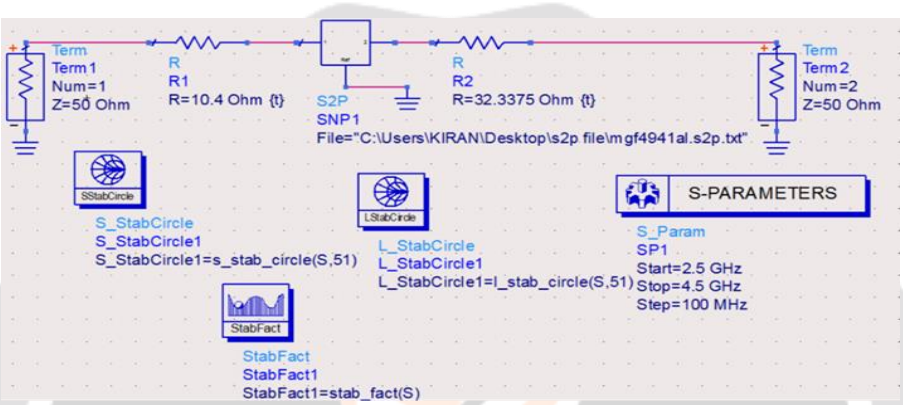

Figure 2 Transistor stability after connecting source and load resistance

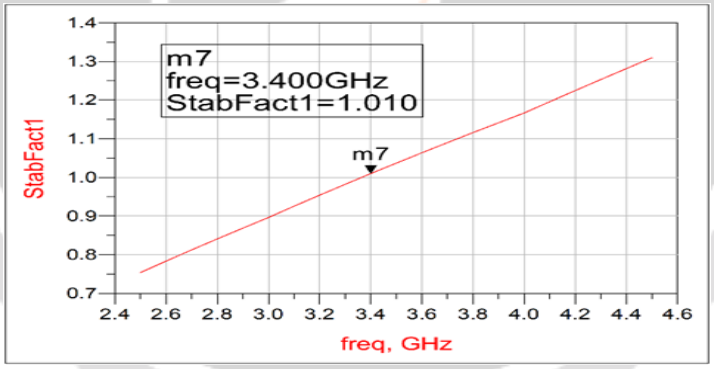

Figure 3 Stability factor

After connecting source and load resistance at source and load respectively, the value of stability factor (K) is 1.010(K>1). So, now the transistor is in stable region.

2.4. Impedance matching networks

Impedance matching is required to maximize the power transfer and minimize the reflections. Smith chart is used for impedance matching. According to maximum power transfer theorem, maximum power delivered to the load when the impedance of load is equal to the complex conjugate of the impedance of source ($Z_S=Z_L^*$).

A minimum noise figure and maximum gain can never be obtained simultaneously. So constant noise figure circles, together with constant available power gain circles are drawn on the Smith chart, from which reflection coefficients can be selected that compromise between the noise figure and gain performance. In the present communication, the stabilized amplifier is simulated to obtain the best noise matched at the input side and gain matched at the output side. The most critical part is the input stage where a 50 Ω input line has to be transferred into complex impedance varying with frequency. This complex impedance should also be as close as possible to

the value optimized for the best noise performance of the transistor. To reduce the size of the circuit, low impedance shunt stubs and high impedance series stubs have been employed.

There are two types of Impedance matching:

i) Input Matching

ii) Output Matching

i) Input Matching

For matching the source and transistor, Input matching network is required.
For input matching network, first we find the value of SmGamma1 in ADS. This value of SmGamma1 indicates that the impedance value and whose complex conjugate value (SmGamma1*) is required to match with 50Ω terminal impedance at input side.
The value of SmGamma1 is 4.685+j90.449Ω. And complex conjugate value (SmGamma1*) is 4.685-j*90.449Ω.

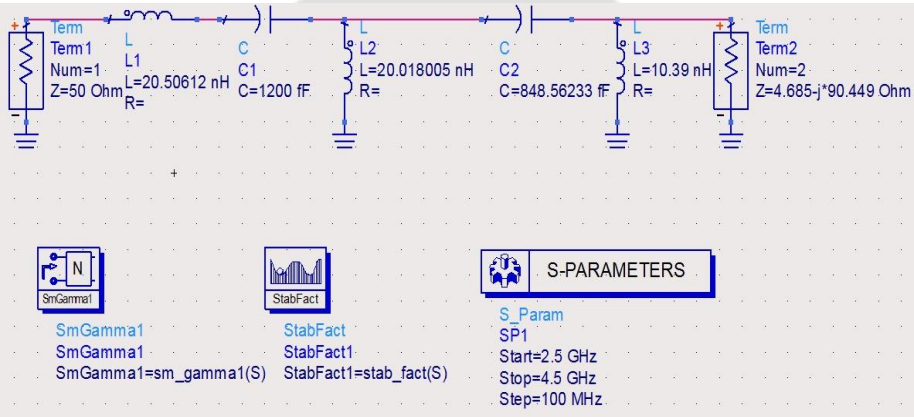

Figure 4 Input matching network

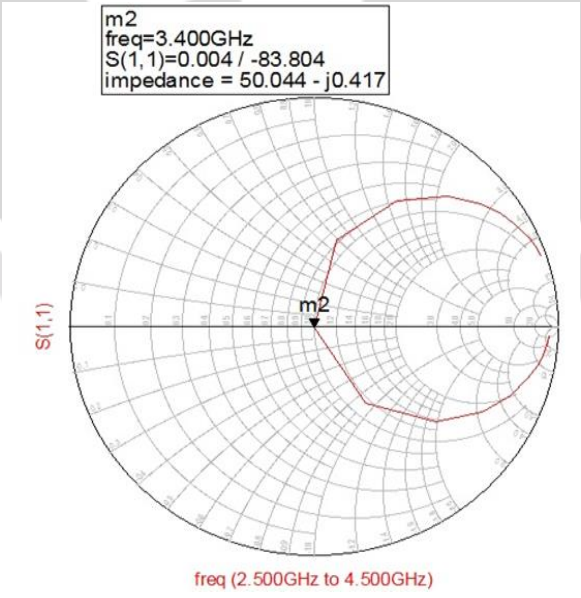

Figure 5 Input Impedance Matching

ii) Output Matching

For matching the Load and transistor, Output matching network is required.
For output matching network, first we find the value of SmGamma2 in ADS. This value of SmGamma2 indicates that the impedance value and whose complex conjugate value (SmGamma2*) is required to match with 50Ω terminal impedance at output side.

The value of SmGamma2 is 10.467+j78.166Ω. And complex conjugate value (SmGamma2*) is 10.467-j*78.166Ω.

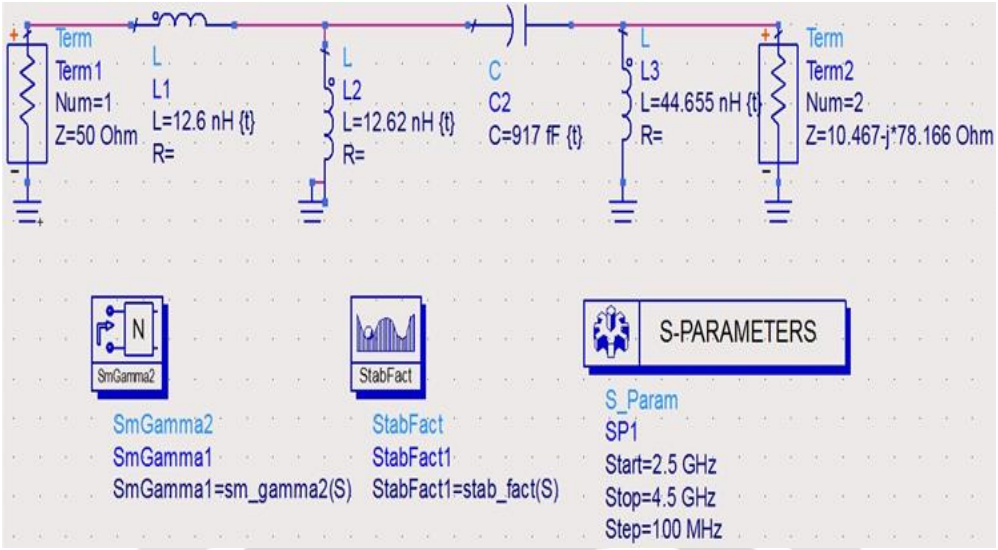

Figure 5 Output matching network

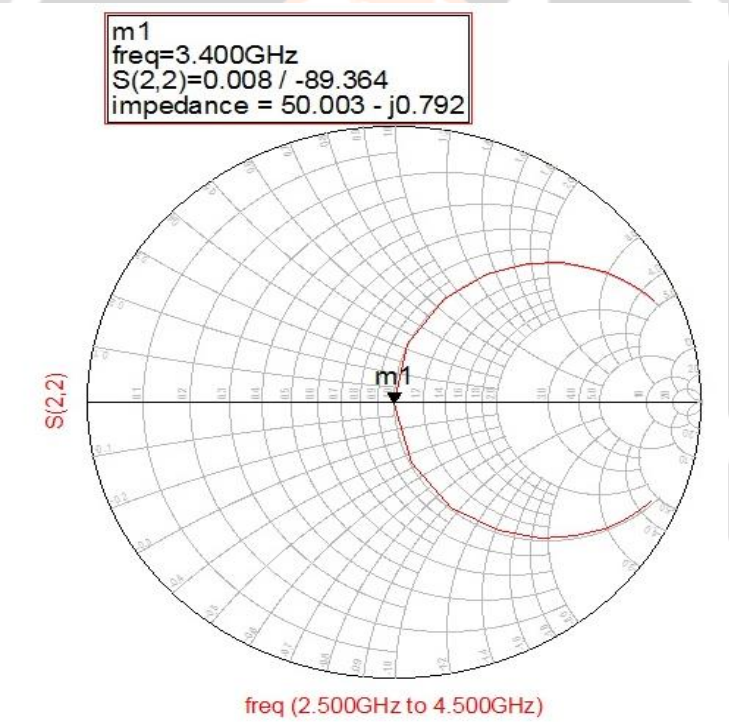

Figure 6 Output Impedance Matching

2.5. Biasing network

The process of obtaining a certain DC drain current at a certain DC drain voltage by setting up the operating point called biasing.

After establishing the operating point, when an input signal is applied, the output signal should not move the transistor either to saturation or to cut-off.

As per my transistor (MGF4941AL) datasheet, the Recommended Bias Conditions are V_{DS}=2V, I_D=10mA. So, I will design biasing network by proper value of resistors and make voltage and current at drain as per bias conditions.

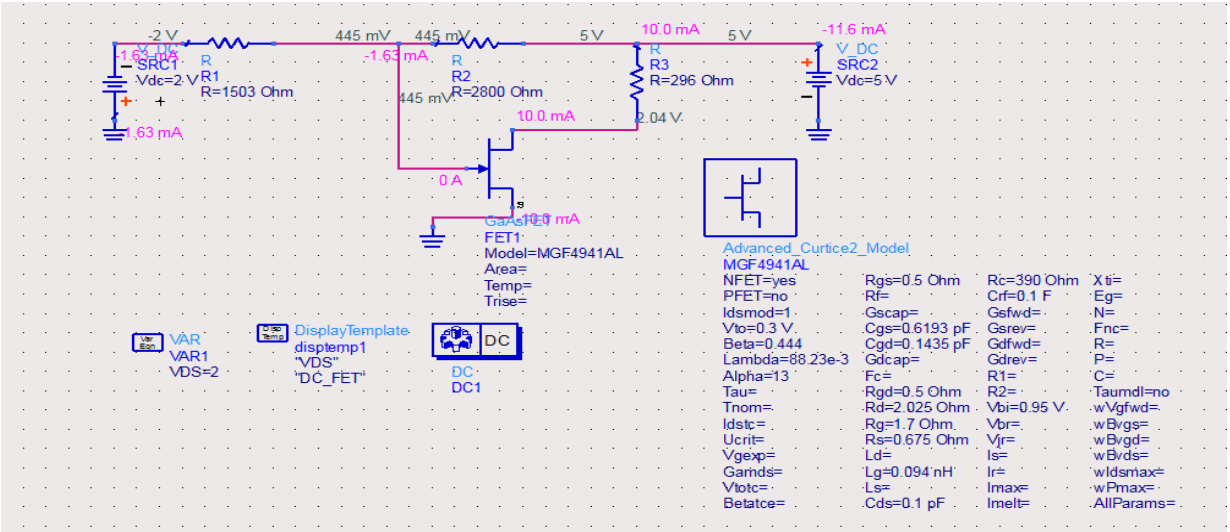

Figure 7 Biasing network

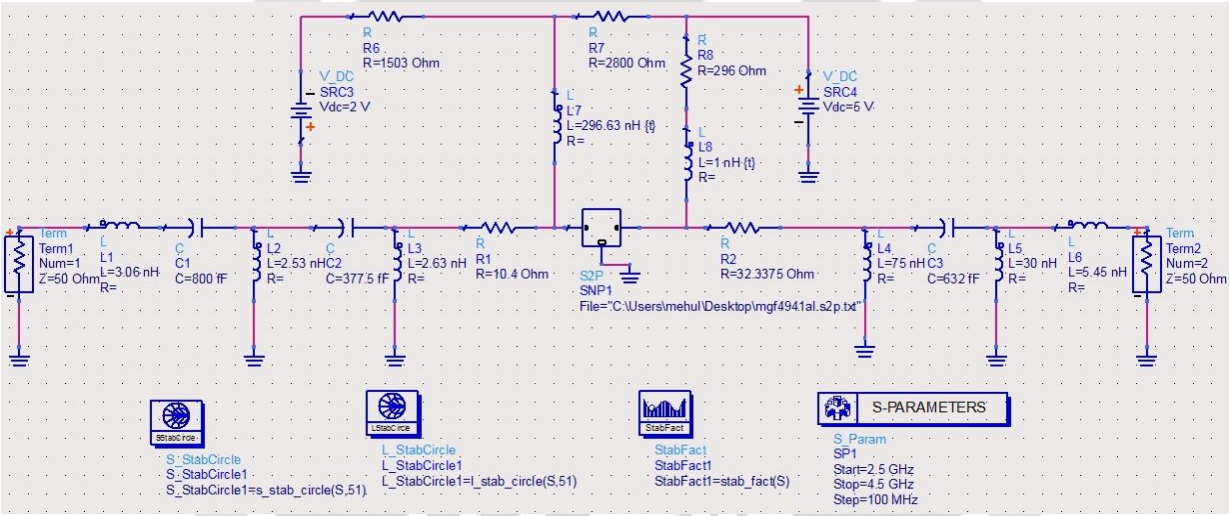

Figure 8 Final LNA circuit

2.6. Simulation Circuits & Results

By using Advance Design System (ADS) software design a Low Noise Amplifier. The Schematic diagram and simulation results of LNA are shown in figures (4-12).

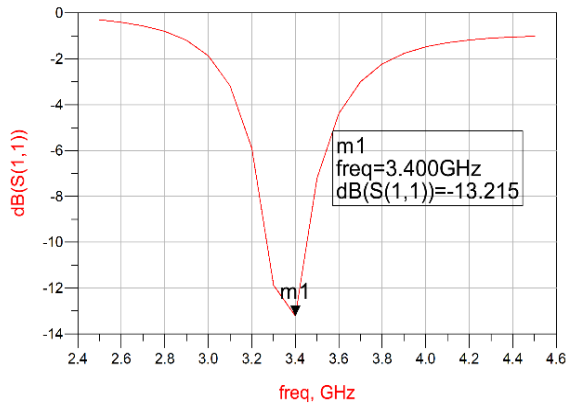

Figure 9 Input Return Loss

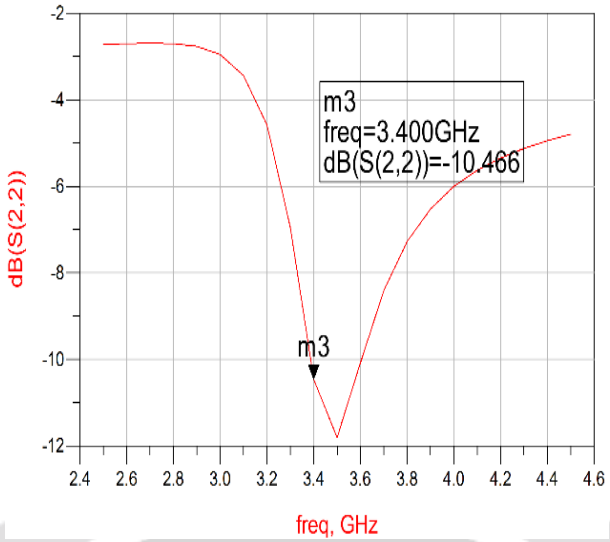

Figure 10 Output Return Loss

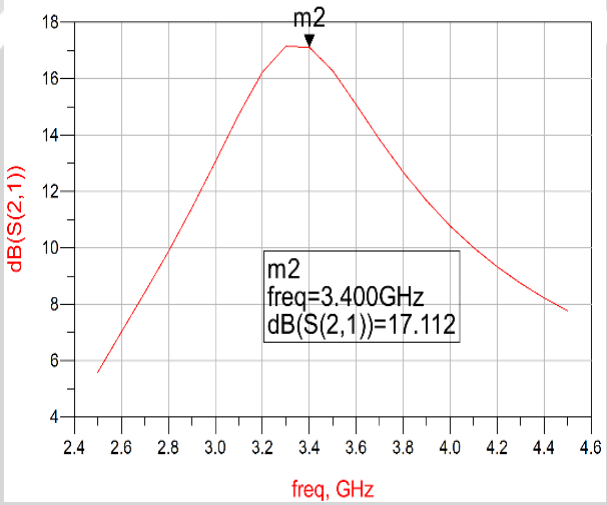

Figure 11 Gain

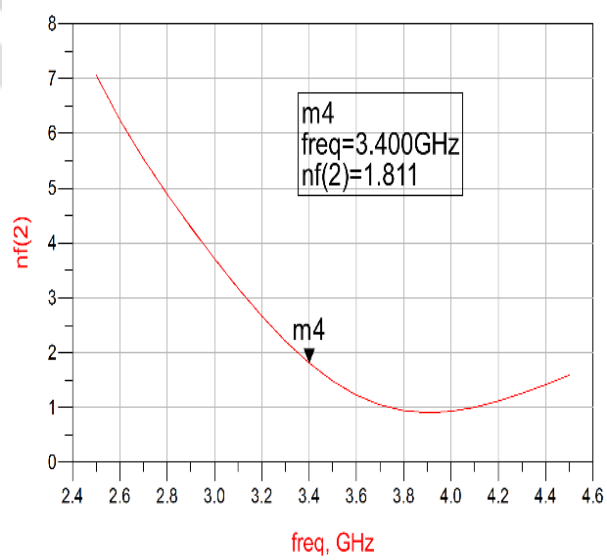

Figure 12 Noise Figure

3. SIMULATED RESULTS

The complete schematic of the Low Noise Amplifier is shown in Figure 4. The performance results are shown in the Figure 9,10,11,12.

TABLE 4 SIMULATED RESULTS

PARAMETERS	RESULTS	
	AFTER IMPEDANCE MATCHING NETWORK	AFTER BIASING NETWORK
Input Return Loss(S_{11})	-11.040dB	-13.215dB
Output Return Loss(S_{22})	-10.201dB	-10.466dB
Gain(S_{21})	18.025dB	17.112dB
Stability Factor(K)	1.010	>1
Noise Figure	1.750dB	1.811dB

5. CONCLUSION

A single stage low noise amplifier working at 3.4 GHz frequency is designed. After connecting biasing network and matching network the noise figure and gain of the prototype LNA is measured as 1.811 dB and 17.112 dB respectively. While all the target specifications are met, the input return loss is lower than the desired one.

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REFERENCES

[1] Chao Sun, Haoquan Hu, Qianyun Pang. “Design of a S-band Low Noise Amplifier” 2014 IEEE International, p.p. 258-261, ISBN: 978-1-4799-4245-9.

[2] Promad K B, KumarasHamy H.V, Praveen K B. “The Design and Simulation of Radio frequency Narrow Band Low Noise Amplifier with Input, Output, Intermediate Matching.”,2013 IEEE, p.p. 001-004, ISBN: 978-1-4799-0400-6.

[3] REENA K. PANCHAL, JAYESH P. PABARI. “Design of Power Amplifier and Low Noise Amplifier for 2.4 GHz RF Front End in Wireless Sensor Network”, International Journal of Engineering Sciences Research-IJESR, p.p. 851-858, ISSN: 2230-8504; e-ISSN-2230-8512, Vol.04, Issue 02; March-April 2013.

[4] Sunny Raj Dommaraju, Sanju Ren, “An 180nm CMOS Low Noise Amplifier with single Ended Input and Differential Output”, 2012 IEEE, p.p. 186-189, ISBN: 978-1-4673-2792-3.

[5] Chandan kumar Jha and Nisha Gupta, “Design of a Front End Low Noise Amplifier for wireless Devices”, 2012 IEEE, p.p. 001-004, ISBN: 978-1-4673-0455-9.

[6] Yu-na Su, Geng Li. “Design of a Low Noise Amplifier of RF Communication Receiver for Mine”, 2012 IEEE Symposium, p.p. 125-127, ISBN: 978-1-4673-2365-9.

[7] Prabir K. Saha, Subramaniam Shankar, Rob Schmid, Richie Mills and John D. Cressler, “Analysis and Design of a 3-26 GHz Low-Noise Amplifier in SiGe HBT Technology”, 2012 IEEE, p.p. 203-206, ISBN:978-1-4577-1155-8.

[8] Viranjay M. Srivastava, Ravinder Kumar. “Low Noise Amplifier for 2.45 GHz Frequency Band at 0.18 µm CMOS Technology for IEEE Standard 802.11 b/g WLAN”, I.J. Intelligent Systems and Applications, 2012, 9, p.p. 68-74, DOI: 10.5815.

[9] A. Baishya P.P.Sahu, M.K.Naskar. “A High gain Low Noise Amplifier for 0.9-6GHz wireless Applications”, 2011 IEEE, p.p. 001-004, ISBN: 978-1-4244-9190-2.

[10] Santu Kr.Giri, Chayanika bose, “Design and Development of an S-band Low Noise Amplifier.”, 2010 Annual IEEE India Conference (INDICON), p.p. 001-004, ISBN: 978-1-4244-9074-5.