Design and Testing of UART to SPI Bridge

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ABSTRACT

The UART-SPI interface provides usage for the universal asynchronous receiver/transmitter (UART) to serial peripheral interface (SPI). This interface can be used to communicate to SPI slave devices from a PC with UART port. The interface consists of three blocks: the UART interface, the UART to SPI Bridge interfacing block and the SPI Master interface The UART to SPI bridge allows these devices to communicate with SPI slave devices such as ADC, RTC, CODEC, LCD, and EEPROM through their standard UART.

Keywords: UART, RS232 and SPI.

1. INTRODUCTION

Universal Asynchronous Receiver and Transmitter (UART) is an asynchronous serial communication standard usually used in conjunction with RS232 communication protocol. Serial Peripheral Interface (SPI) is a synchronous high speed serial data link that operates in full duplex mode. UART to SPI Bridge enables communication between UART and SPI slave A UART (Universal Asynchronous Receiver and Transmitter) is device allowing the reception and transmission of information, in a serial and asynchronous way. A UART allows the communication between a computer and several kinds of devices (printer, modem,etc.), interconnected via an RS-232 cable.

2. UART

UART is Data transmission is made by the UART in a serial way, by 11-bit blocks , A 0 bit marks the starting point of the block, Eight bits for data, One parity bit, A 1 bit marking the end of the block, The transmission and reception lines should hold a 1 when no data is transmitted logic.

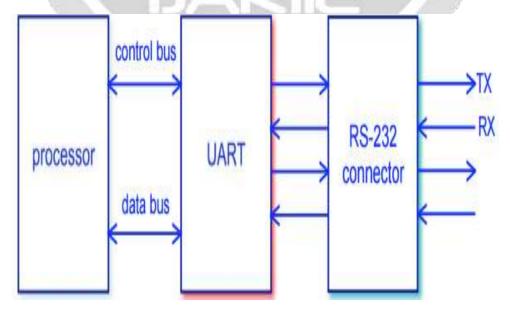
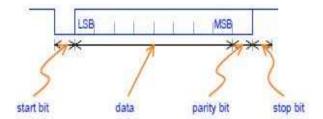


FIG. 1 SERIAL TRANSMISSION



Send the ASCII letter 'W' (1010111)

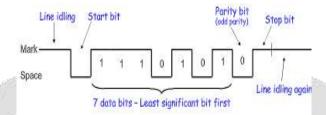


FIG. 2 EXAMPLE OF UART TRANSMISSION

3. SPI

Serial Peripheral Interface (SPI) is an interface bus commonly used to send data between microcontrollers and small peripherals such as shift registers, sensors, and SD cards. It uses separate clock and data lines, along with a select line to choose the device you wish to talk to.

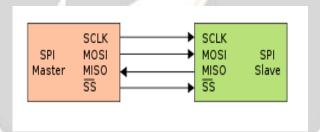


FIG. 3 SINGLE MASTER AND SINGLE SLAVE

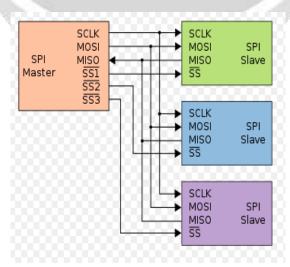


FIG. 4 SINGLE MASTER AND MULTIPLE SLAVES

3.1 SPI TRANSMISSION

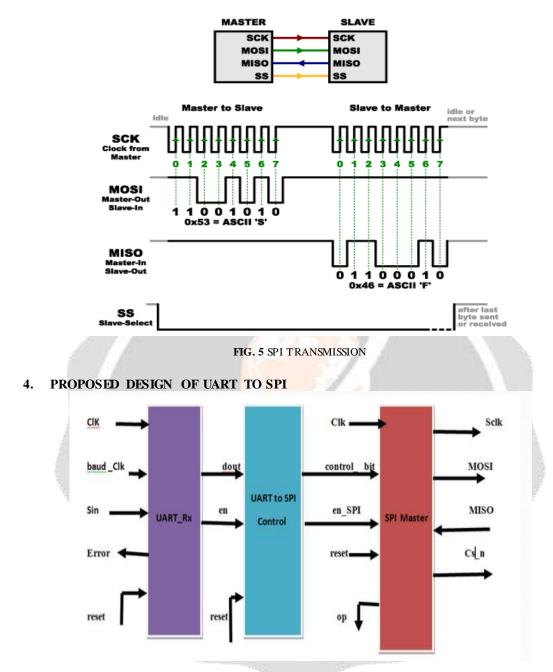


FIG. 6. BLOCK DIAGRAM OF PROPOSED WORK

This design example consists of three blocks: the UART interface, UART-to-SPI control block, and SPI master interface. The UART interface is achieved using Core UART by Micro semi. This block handles the data at the UART end .The SPI master block generates the control signals to interface to external slave devices. This interface communicates with the slave devices using the serial data out port (MOSI), serial data in port (MISO), output clock (SCLK), and slave select ports (SS_N [7:0]). There are three internal registers in the design: control register, transmit register, and receive register. The control register sets the different control bits, the transmit register sends the TX data to the SPI bus, and the receive register receives the Rx data from the SPI bus. After every reset, data received from the external UART go to the control Register.

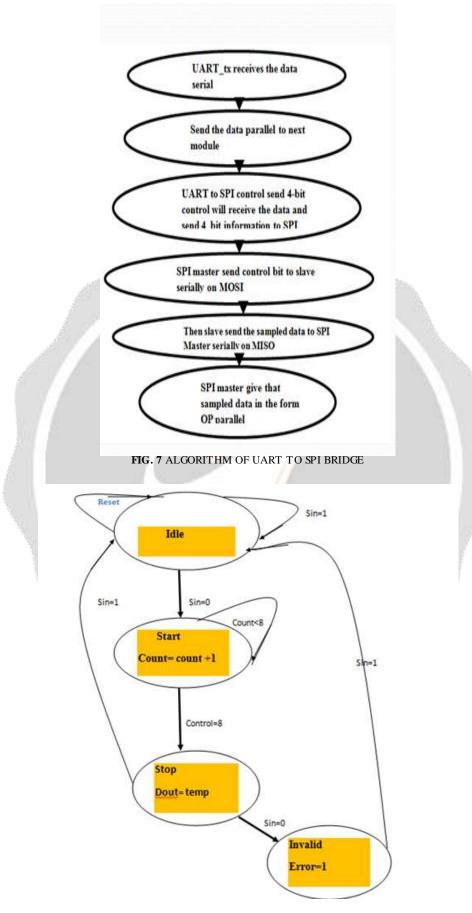


FIG. 8 UART TO SPI CONTROLLER

ASCII CODE	CONTROL_Bit				
47	1000				
48	1001				
49	1010				
50	1011				
51	1100				
52	1101				
53	1110				
54	1111				

TABLE 1: TATBLE OF ASCII CODE

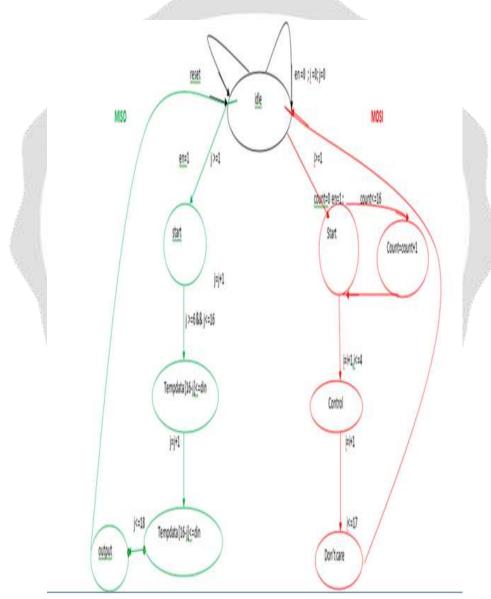


FIG. 9 FSM of SPI MASTER

5. TESTING

5.1. UART receiver testing

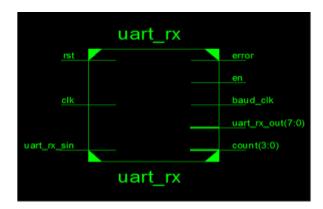


FIG. 10 RTL of UART RICEIVER

5.2 UART to SPI Controller

input	Uart_rx_out[7:0] or Ascii code	35	48	49	54	30	49	48	53	51	47	50
input	en	1	1	1	1	1	0	0	0	0	1	1
output	Control_bit[3:0]		1001	1010	1011						1000	1011

FIG. 11 TESTING OF UART TO SPI CONTROLLER

6. RESULT

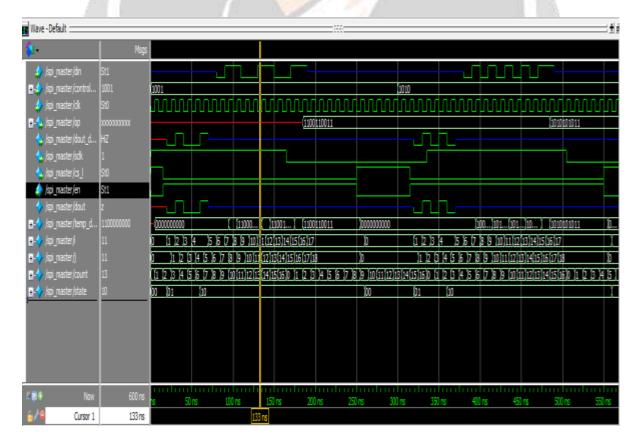


Fig. 12 SIMULATION WAVEFORM OF SPI MASTER

A. If Stop=1



You have output

no error

FIG. 13 SIMULATION WAVEFORM WITHOUT ERROR

B. If Stop=0



No output error

FIG. 14 SIMULATION WAVEFORM WITH ERROR

5. CONCLUSION

The UART-to-SPI can fit in any application where an SPI device has to be used. Typical applications include interfacing of EEPROM, flash memories, and sensor the portable electronics market requires devices that are small and highly efficient. The UART-to-SPI core described in this document reduces the real estate required on the board.

6. REFERENCES

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