Design and analysis of 6T SRAM cell using FINFET at Nanometer Regime

Monali S. Mhaske[1], Prof. S. A. Shaikh[2]

[1] ME , Dept. Of Electronics And Telecommunication ,PREC, Maharashtra, India
[2] Associate Professor, Dept. Of Electronics And Telecommunication ,PREC, Maharashtra, India

ABSTRACT

With the scaling of MOSFET there is a increase in the channel length modulation, Drain induced barrier lowering (DIBL), increase in sub threshold slope and gate leakage all these effects decreases gate coupling to the channel. FINFET technology is one alternative which can offer the performance as may be expected from next generation Si technology. FINFET is expected to replace conventional MOSFETs and also SOI MOSFET for integrated memory applications due to better resistant to some of the source of intrinsic parameter fluctuation. We can improve the performance of 6T SRAM using FINFET. Chip density increases due to smaller transistor dimensions. The stability of SRAM cell affected due to the nano technology nodes variation in Process, voltage, and Temperature (PVT). In the proposed work 6T SRAM is implemented using 32 nm Bulk MOSFET and FINFET and stability in hold/standby, read and Write mode is ananlysed. Design consider Bulk MOSFET, SOI MOSFET and FINFET at 32nm technological node. The working and stability of 6T SRAM in all modes of operation has been analyzed. Supply voltage, temperature, transistor scaling of Bulk MOSFET, SOI MOSFET and FINFET are analyzed during read and standby mode. A comparative study between Bulk 6T SRAM and SOI 6T SRAM and FINFET 6TSRAM has been made in this work. For this work we have use 32 nm FINFET and 32nm Bulk MOSFET PTM file, and all the simulation work is carried out in HSPICE 2008.3

Keyword: - *6T SRAM, SNM, Cell Ratio, Stability, Supply Voltage, Pull Up Ratio etc.*

1. INTRODUCTION :

1.1 SRAM Scaling Trends :

SRAM area has exceed to 90% of overall chip area because of the demand for higher performance, lower power, and higher integration. The SRAM has strong impact on chip cost and yield. To increase memory density memory bit cells are scaled to reduce their area by 50% each technology node to increase memory density. High density SRAM bit cells use the smallest devices in a technology to make SRAM more vulnerable with variations. For example, in state of the art 28 nm technology, a high density bit cell area is approximately 0.12 m2.

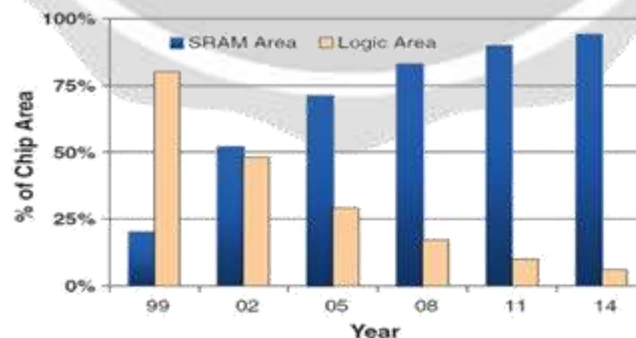

Figure 1: Logic area and SRAM versus technology scaling. SRAM dominates chip area in modern microprocessor and SoCs.

The predominant yield loss comes from the increase in process variations. In advanced CMOS technology nodes which strongly impacts SRAM functionality as the supply voltage is reduced. Local random variations due to line edge roughness (LER) decrease the robustness of SRAM operation.

2 Objective of Paper :

The objectives of this paper are
1)To design a SRAM cell which give better performance and require small area.
2) To study the Bulk-MOSFET SRAM,SOI-MOSFET SRAM,FINFET SRAM working of cell, its stability and process parameter effecting stability.
3) To study 6T SRAM cell using Bulk MOSFET, SOI MOSFET and FINFET, the stability & parameter effect on stability.
4) To compare bulk MOSFET SRAM, SOI MOSFET SRAM and FINFET SRAM for different parameters.

3. Modes of Operation & Stability of 6T SRAM :

3.1 *6T SRAM Working:*

The SRAM cell having three modes of operation that are Standby, Read and write mode. During standby mode word line is grounded. As long as SRAM is connected to VDD it is able to hold the data. In read mode before selecting the word-line, the bit-lines are usually precharged to VDD. At the cell storing side a logical low voltage through the access pull down and access transistor the bit line is discharged for developing differential voltage across bit lines. Word line is selected in write mode and Bit lines are access in complementary voltage levels through a write driver The internal storage nodes are discharged through the access transistor. In standby mode the word line is grounded as the cell stores the data indefinitely till it is connected to VDD.

The Fig.1 shows the basic 6T SRAM cell. To accumulate one bit of information , the cell consist of two cross-coupled CMOS inverters and access transistors are two N-type transistors(M2 and M5). To perform access read operation the bit lines (BL and BLB) transistor are connected to the word line (WL).

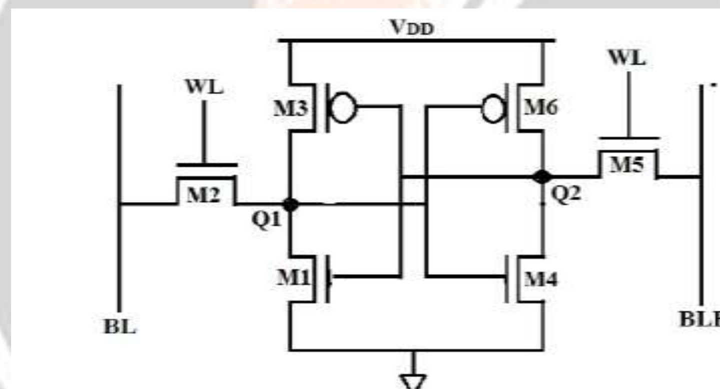

Figure 2: Basic 6T SRAM Cell

3.2 Failure Mechanisms :

Read Failure- :

While reading the content of SRAM cell read failure occurs. By increasing the difference between the trip-point of the inverter related with the voltage rise at the node storing “0” and node storing “1” read failure can be reduced.

Write Failure :

An unsuccessful write to the SRAM cell is write failure. During the turn on time of word line write failure occurs if the node storing logic 1 then it cannot be discharged through the access transistors. By increasing the turn on time of word line with write access time increased write failure can be reduced.

Access Failure :

At the time of sense amplifier firing if the voltage difference between the two-bitlines remains below the offset voltage of the sense amplifier Access failure occurs.

Hold Failure :

Because of high-leakage of the pull-down NMOS transistors which is connected to the node which store “1” the hold failure occurs. By reducing leakage in standby mode using high threshold voltage pull-down transistors this failure can be avoided.

4. 6T SRAM STABILITY :

The SRAM cell stability determines the soft-error rate it also determines the sensitivity of the memory to process tolerances and operating conditions. To analyze static cell stabilities due to dc perturbations, offsets and mismatch, Static Noise Margin (SNM) simulations have become dominant method to assess the cell reliability in high density memories. The focus of cell stability or implicitly the SNM analysis of SRAM cells have mostly restricted to the simulations, however, some works discuss this through providing analytical expression. This work deals with the SNM of SRAM cell both from analytic as well as simulations point of view. The advantage of mathematical representation is that it explicitly expresses the SNM as function of different cell parameters such as supply voltages, precharge voltages, bitline voltages, and source voltages.

4.1 *Static Noise Margin (SNM)*

Static Noise Margin is defined as the maximum value of dc disturbances that the cell nodes can tolerate before flipping its state. Static noise is dc disturbance such as offsets and mismatches due to processing and variations in operating conditions. In this work, only static-noise sources are taken into account. The SRAM cell should be designed such that under all circumstances, there would be some SNM to deal with the dynamic disturbances caused by alpha-particle incidences, crosstalk, supply voltage ripple, and thermal noise Figure 3 demonstrates the schematic diagram for SNM simulations using noise source. To simulate the SNM of this memory cell, two bitline and the wordline of the cell are kept at V_{DD}. This SNM is also called transfer curve (V_{TC}) of one inverter and the mirrored voltage transfer read SNM In order to estimate the stability, the noise margin can be examined with the aid of analytic expression. In this, however, a common graphical representation of SNM so called butterfly curve for a cell during read access and while holding data (unaccessed) is presented. Butter-fly curve is composed of the voltage curve of the other inverter (V_{TC}^{I}) in a single plot. Neglecting the mismatch and variation inside the cell, the two V_{TCS} are equivalent. In Figure 3.14 the V_{TCS} of one inverter is plotted for both read access as well as the hold mode. Finding the maximum size of square that can fit in the curve. The side of the square gives the value of SNM or we can measure the length of diagonal and divide it by square root of 2. The another graphical method.

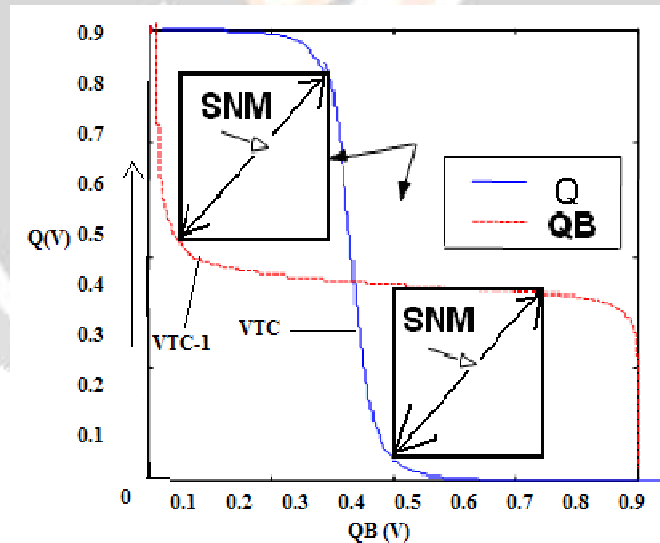

Figure 3: Measuring SNM by Butterfly curve

Fig. shows a stylized version in two coordinate systems which are rotated 450 relative to each other. The maximum and minimum of curve A represent the required maximum squares. Assume that the normal and mirrored inverter characteristics are defined by the functions y = $F_1(x)$and y = F_2'(x), where the latter is the mirrored version of y = F_2(x). To find F1 in terms of u and v, the (x, y) coordinates must first be transformed into the (u, v) system.

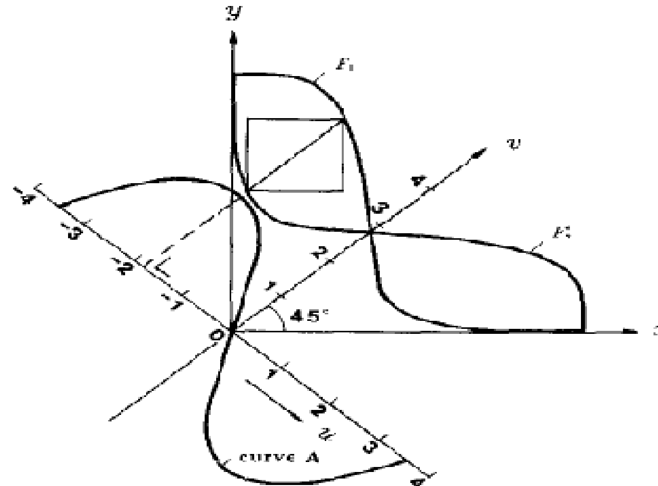

Figure 4: SNM based on “maximum squares” in a 450 rotated coordinate system

4.1.1 Read Stability :

Read stability of SRAM cell can be obtained by three types. First by plotting the SNM curve without changing the stored bit the Maximum value of DC noise voltage that can be tolerated by the SRAM cell is stability. For measuring the read stability of SRAM cell in large array third method is at the ‘0’ storage node BL current is monitored while ramping down the supply of cell with the bit line pre charged WL driven by nominal VDD. Whereas in read mode the bit lines are precharged to a high level VDD and then the word line is selected (pulsed to a high level).i.e.WL=1 BL=1 BLB=1.

4.1.2 Write Stability :

To measure write stability there are already five exiting static approach. During a write operation, until the trip point of the inverter formed by the PMOS and NMOS is reached and the bit cell is successfully written, a low going bit line voltage pulls down the ‘1’ storage node as the word line is held high. To measure write stability Bit line write margin (BLWM) is used. BLWM is the maximum bit line voltage which flip the cell state and it can be measured through monitoring the BL current at the ‘0’ storage node while ramping down the other bit line voltage with word line held high. The write stability can also be measured by Word line write margin (WLWM).It is the maximum of (VDD – VWL) in a word line voltage sweep node. In write mode operation, the bit-lines are driven to complementary voltage levels through a write driver and then the word line is selected. i.e. WL=1 BL=0 BLB=1.

4.1.3 Standby/Hold Stability :

In Standby mode the SRAM cell is able to hold the data indefinitely as long as it is connected to the VDD. Therefore, word line is grounded during standby mode. i.e.WL=0 BL=0 BLB=0

5. RESULT AND DISCUSSION

5.1 ***Effect of Temperature***

The SNM of both bulk and FINFET SRAM during read and standby mode reduces due to increase in temperature. Effect of temperature is seen more on FINFET SRAM than Bulk and SOI SRAM. As the temperature increases for 25 to 150 the stability during read mode of bulk SRAM increased 25.4%whereas the stability in standby mode decreases by 14.50%.for SOI SRAM it reduces 19% during read mode. where as the stability during standby mode decreases by 16%.But for FINFET SRAM stability during Read mode increased 4.5% and in standby mode decreased by 45.16%.

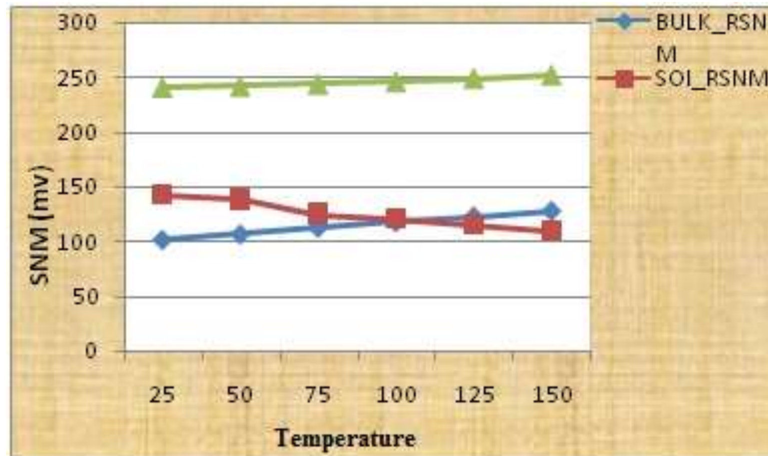

Figure 5: Comparison of impact of Temperature on SRAM Stability during Read Mode of Bulk,SOI and Finfet SRAM

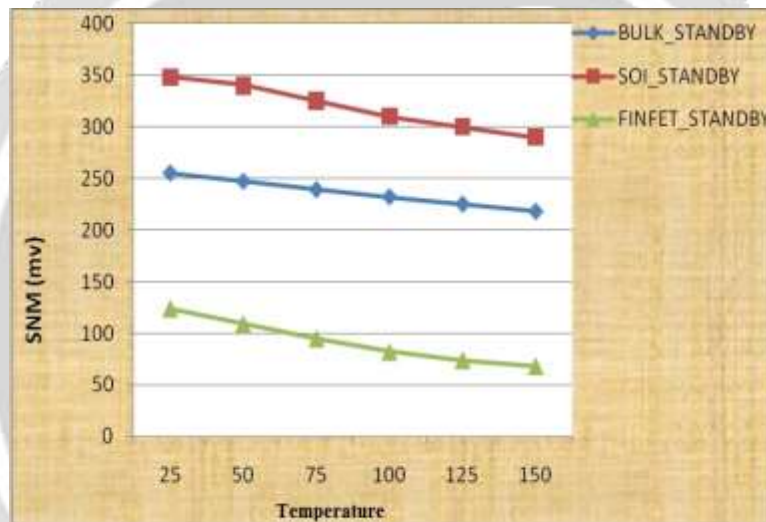

Figure 6: Comparison of impact of Temperature on SRAM Stability during Standby Mode of Bulk,SOI and Finfet SRAM

5.2 *Impact of Supply Voltage on Stability*

As the VDD decrease the value of SNM also decrease. So, it is essential to maintain full VDD during read cycle and standby mode so that we get a better value of SNM. That means a better stability. At every voltage the value of SNM for FINFET SRAM is greater than SNM of both Bulk and SOI SRAM. It means we can have a safe power consumption to a great extent using FINFET SRAM.

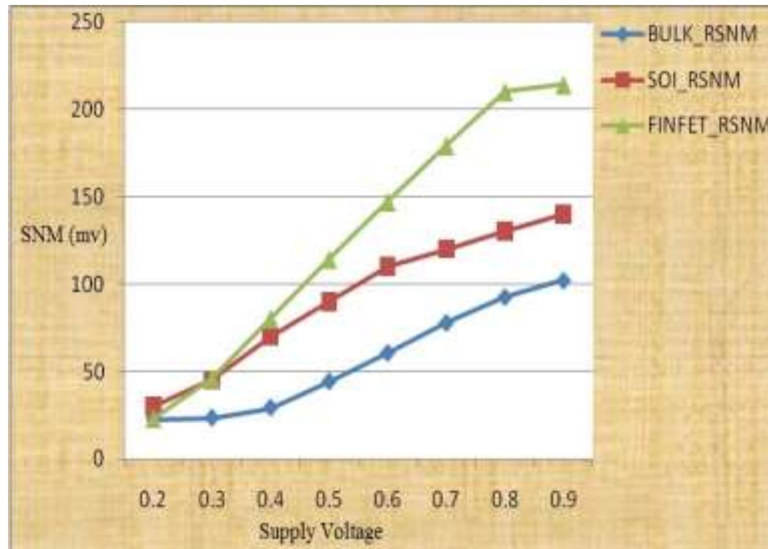

Figure 7: Comparison of impact of supply voltage on Stability during Standby and Read mode of Bulk ,SOI and FINFET SRAM.

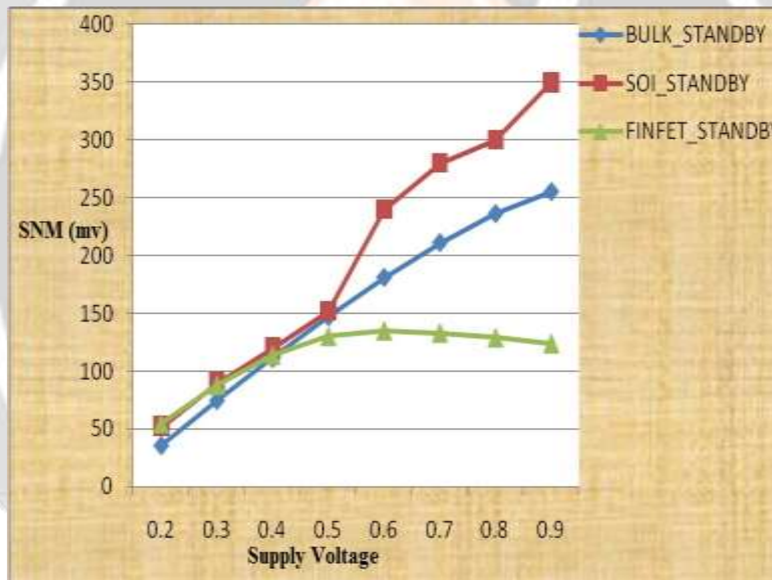

Figure 8: Comparison of impact of supply voltage on Stability during Standby mode of Bulk ,SOI and FINFET SRAM.

5.3 Effect of transistor sizing.

When the Cell ratio increases SNM during standby and read mode decreases for all the SRAM. But Decrease in SNM is very small in SOI SRAM comparison with FINFET and Bulk SRAM.

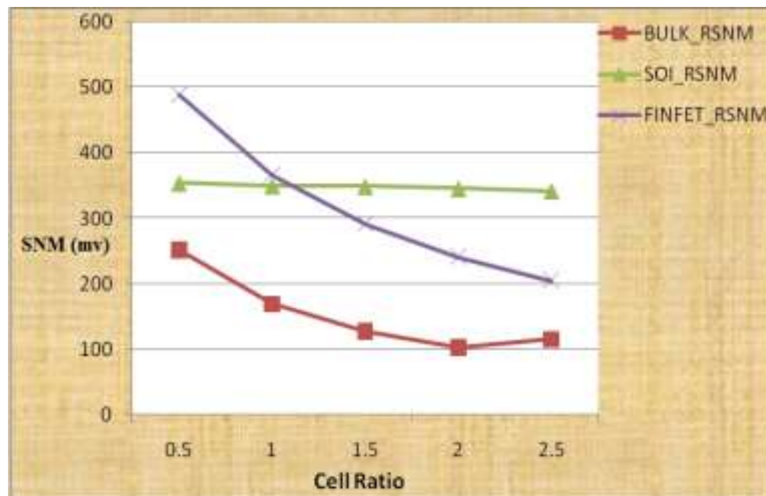

Figure 9 : Comparison of impact of Cell Ratio on Stability during Standby and Read mode of Bulk ,SOI and FINFET SRAM.

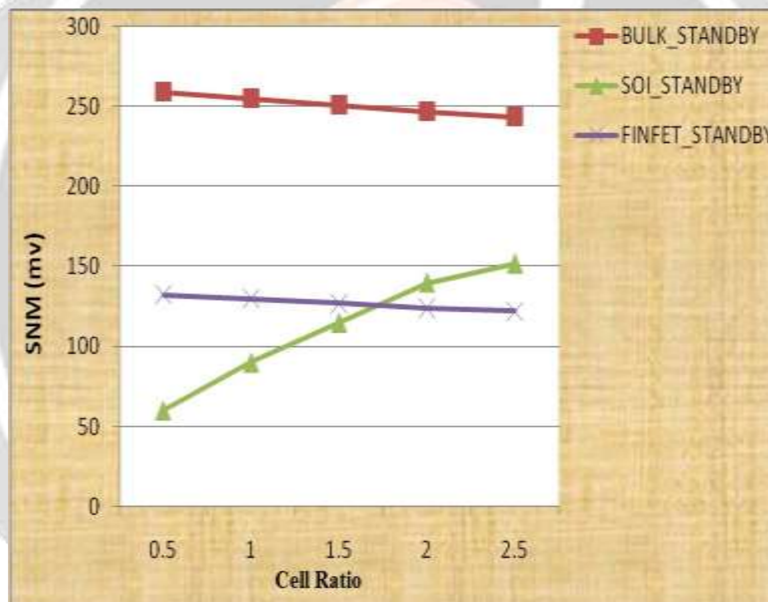

Figure 10: Comparison of impact of Cell Ratio on Stability during Standby and Read mode of Bulk ,SOI and FINFET SRAM.

MODES	Standby (SNM)	Read (RSNM)	Write (WLWM)
Bulk SRAM	255Mv	102mV	799Mv
SOI SRAM	349mV	141mV	685mV
FINFET SRAM	132mV	367mV	785mV

Table 1: Comparison of Stability for Bulk SOI and FINFET SRAM

CONCLUSION :

In the proposed work we have use same process parameter for Bulk MOSFET and FINFET. And Both are compared with SOI MOSFET at 32 nm node. Bulk 6T SRAM and FINFET 6TSRAM are designed using HSPICE.

A comparative study between Bulk 6T SRAM ,SOI 6T SRAM and FINFET 6TSRAM has been made in this work. The working and stability of 6T SRAM in all modes of operation has been analyzed. Supply voltage, temperature, transistor scaling of Bulk MOSFET, SOI MOSFET and FINFET are analyzed during read and standby mode. In read mode FINFET SRAM give better stability than Bulk and SOI SRAM. In standby mode FINFET SRAM gives better stability than Bulk SRAM. When the Cell ratio increases SNM during standby and read mode decreases for all the SRAM. But Decrease in SNM is very small in SOI SRAM comparison with FINFET and Bulk SRAM. At every voltage the value of SNM for FINFET SRAM is greater than SNM of both Bulk and SOI SRAM. It means we can have a safe power consumption to a great extent using FINFET SRAM. As the temperature increases for 25 to 150 the stability during read mode of bulk SRAM increased 25.4%whereas the stability in standby mode decreases by 14.50%.for SOI SRAM it reduces 19% during read mode.where as the stability during standby mode decreses by 16%.But for FINFET SRAM stability during Read mode increased 4.5% and in standby mode decreased by 45.16%.

REFERENCES

[1] S. S. Chopade, D. V. Padole, "*Stability Analysis of 6T SRAM Cell for Nano scale FD-SOI Technology*", ISBN: 978-1-4799-5364-6/14, 2014 IEEE.

[2] S. S. Chopade, D. V. Padole, "*Design of Double Gate MOSFET and FDSOI using high k material for Nano scaled Circuits*", ISBN: 978-1-4799-4075-2/14, 2014 IEEE.

[3] Jawar Sing, Saraju P. Mohanty and Dhiraj K. Pradhan,"*Robust SRAM design and analysis*", ISBN: 9781461408178, Springer, 2013

[4] Jerome Mazurier, Olivier Weber, Francois Andrieu, Alain Toffoli, Olivier Rozeau, Thierry Poiroux, Fabienne Allain, Pierre Perreau, Claire Fenouillet-Beranger, Olivier Thomas, Marc Belleville, Olivier Faynot "*On the variability in Planar FDSOI Technology: From MOSFET to SRAM Cells*", IEEE Transactions on electron devices, Vol 58, No 8, August 2011.

[5] Ajay Gadhe, Ujwal Shirode, "*Read stability and Write ability analysis of different SRAM cell structures*," International Journal of Engineering Research and Applications (IJERA) ISSN: 2248- 9622, Vol. 3, Issue 1, January -February 2013, pp.1073-1078

[6] Nahid Rahman, B. P. Singh, "*Static-Noise-Margin Analysis of Conventional 6T SRAM Cell at 45nm Technology*," International Journal of Computer Applications (0975 – 8887) Volume 66– No.20, March 2013.

IJARIIE