Design of Area Efficient Complex Number Multiplier Using Vedic Multiplication

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ABSTRACT

In this paper, an area reduced multiplier design is conferred. This structure is based on ancient algorithm of Vedas, proposed within the Vedic mathematics scripture of Sri Bharati Krshna Tirthai Maharaja. Complex number multiplication is a very important numerical operation to be performed with fast and less power utilization in frameworks like Digital Signal Processing. Hence in this paper, a design is proposed for a vedic real multiplier based on urdhva tiryakbhyam sutra of Indian Vedic mathematics. The partial product and also sums are produced in few stages that decreases the carry propagation from LSB to MSB. In the proposed design we have reduced the amount of logic gates (area), hence reducing the power consumed. Finally, the effect of the Vedic multiplication is contrasted with array multiplication.

Keywords: *Vedic real multiplier, Urdhva Triyakbhyam sutra, complex multiplier, FPGA, area efficient architecture, array multiplier*

1. INTRODUCTION

Multiplication based operations are some of the commonly used functions, at present actualized in numerous Digital Signal Processing (DSP) application, for example, digital image processing, arithmetic Logic Unit (ALU) of Microprocessors, convolution and filters. The delay increases for multiplication of higher bit numbers, so the development of a less delay with low power multiplier design is necessary. Moreover, the data in DSP units are in the form of complex numbers which further increase the design requirement for building a multiplier with low power and high speed.

Conventional array multiplier occupies more area and consumes a lot of power due to the large number of full adders. Since the carry is being propagated to next full adder the delay of array multiplier is high. One way to improve the speed as well as to reduce the power is to employ the ancient methods of mathematics known as Vedic mathematics. The word Vedic in Sanskrit means store-house of knowledge. The Vedic mathematics offers shortcuts to quickly perform the arithmetic operations. There is a total of 16 vedic sutras or formulas and 13 sub-sutras to perform different mathematical operation. For performing the multiplication operation there are two sutras- urdhva tiryakbhyam and nikhilam sutra. Out of this two, the urdhva tiryakbhyam sutra is discussed in this paper to design a multiplier and compared the speed and area with array multiplier. Complex number multiplication using Vedic multiplier is proposed and contrasted with array multiplier.

The paper is organized as follows. In section 2, demonstrate the 2x2 and 4x4 Vedic multiplier architectures of proposed architecture. Section 3 tells about the complex number multiplication using Vedic multiplier. The results and comparisons are included in section 4, while section 5 contains conclusion.

2. VEDIC MULTIPLIER

2.1 2X2 bit Vedic Multiplier

Consider two 2-bit numbers X and Y where A=a1a0 and B=b1b0. Initially, the least significant bits (LSB) a0 and b0 is multiplied which gives the LSB (s0) of the final product. Then, the LSB of the multiplicand a0 is multiplied with the next higher bit of the multiplicand b1. The result gives second bit s1 of the final product and carry c1 which was generated gets added with the partial product obtained by multiplying the most

significant bits a1 and b1 to give the sum s2 and carry c2. The sum s2 is the third bit and carry c2 becomes the fourth bit of the final product.

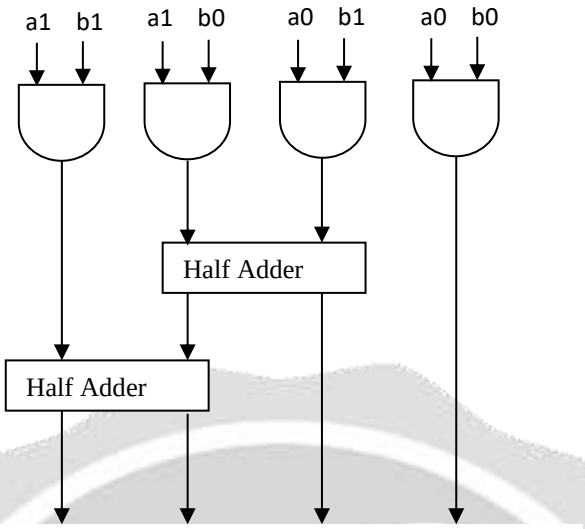

Fig -1: Block diagram of 2x2 Multiplier

$$s_0 = a_0 b_0 \quad (3.1)$$

$$c_1 s_1 = a_1 b_0 + a_0 b_1 \quad (3.2)$$

$$c_2 s_2 = c_1 + a_1 b_1 \quad (3.3)$$

The final result will be c2s2s1s0.

2.2 4x4 Vedic multiplier

The proposed block diagram of 4X4 vedic multiplier is shown in figure 2.2. To get the final product, 4 two-bit Vedic multipliers are used and three 4-bit ripple carry adders are required. In this proposal, the first 4-bit RC adder is used to add two 4-bit operands obtained from cross multiplication of the middle 2X2 bit multiplier modules. The second 6-bit RC adder is used to add two 4-bit operands, i.e., concatenated 4-bit ("00" & most significant two output bits of right hand most of 2X2 multiplier module) and one 4-bit operand we get as the output sum of hand most of 2X2 multiplier module. The 8X8 bit multiplier is constructed using four 4 bit multipliers and 16X16 bit multiplier is constructed using four 8 bit multipliers and so on.

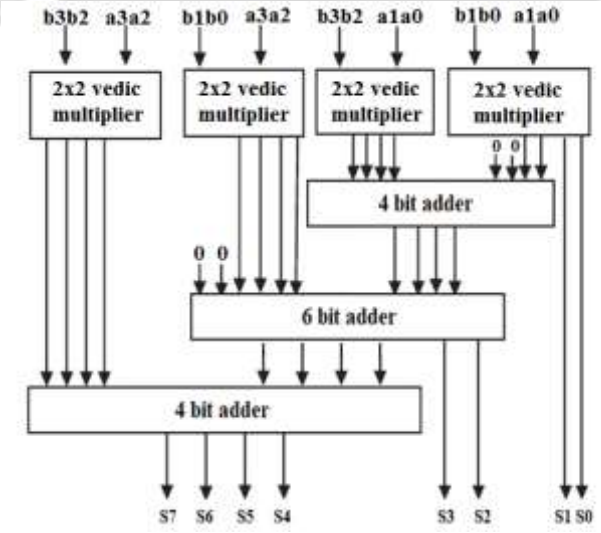

Fig -2: Block diagram for 4x4 Multiplier

2.2.1 Algorithm for 4X4 bit vedic multiplier Using Urdhva Tiryabhyam two Binary numbers

CP=Cross Product (Vertically and Crosswise)

X3 X2 X1 X0 Multiplicand

Y3 Y2 Y1 Y0 Multiplier

P7 P6 P5 P4 P3 P2 P1 P0 Product

PARALLEL COMPUTATIONAL METHODOLOGY

1. C0→ a0 = a0*b0
2. C1→a1 a0 = a1*b0+a0*b1
   b1 b0
3. C2→a2 a1 a0 = a2*b0 + a0*b2 + a1*b1
   b2 b1 b0
4. C3→a3 a2 a1 a0 = a3 * b0 +a0 *b3 + a2 * b1 + a1 * b2
   b3 b2 b1 b0
5. C4→a3 a2 a1 = a3*b1 + a1*b3 + a2*b2
   b3 b2 b1
6. C5→a3 a2 = a3*b2+a2*b3
   b3 b2
7. C6→a3 = a3 * b3
   b3

Where Cn=Cross Product, n=0,1,2,3,4,5,6

3. COMPLEX NUMBER MULTIPLICATION USING VEDIC MULTIPLICATION

Consider two complex numbers

$$a = ar + j\ ai; \quad (3.4)$$

$$b = br + j\ bi; \quad (3.5)$$

The product of *a* and b is given by

$$pr\ +\ j\ pi = ab = (ar + jai) * (br + j\ bi); \quad (3.6)$$

$$pr = (arbr - aibi) \quad (3.7)$$

$$pi = (arbi\ +\ aibr) \quad (3.8)$$

Where pr and pi represents the real part and imaginary part of the final product p, respectively. The above equations can be alternatively writer as follows

$$pr\ =\ arbr - aibi\ = ar(\ br\ +\ bi) - (\ ar\ +\ ai)bi \quad (3.9)$$

$$pi\ =\ arbi + aibr = ar\ (br\ +\ bi) + (\ ai\ -\ ar)br \quad (3.10)$$

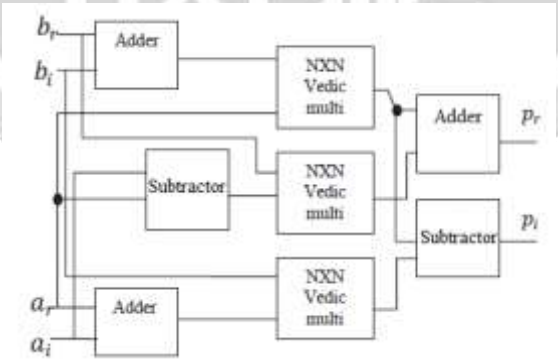

Fig -3: Three real Vedic Multipliers solution architecture for multiplication of two complex numbers

This reduces the number of multiplications from 4 to 3 nxn vedic multiplier as shown in figure

4. SIMULATION RESULTS

The basic 16x16 bit vedic multiplier is implemented in Xilinx Verilog 9.1 and extended to complex number multiplication. The simulation result of two complex number (11 + j5) and (5 + j2) is shown the figure. The array and vedic multiplier are compared in terms of number of slices and delay. From the table 4.1, there is a

decrease in the area and delay of the Vedic multiplier by 40%.

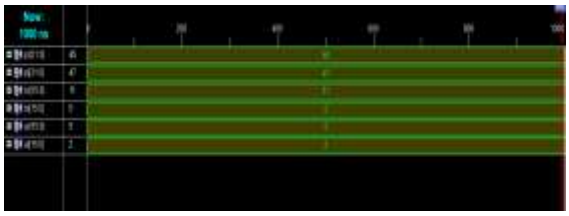

Fig -4.: Simulation result of Vedic complex multiplier using four real multipliers solution

The below table represent the comparison of array and vedic multiplication of complex number.

Table -1: Comparison between array and vedic architecture of complex number

Parameters	Array-16	Vedic-16	Percentage Improvement	Array-8	Vedic-8	Percentage Improvement
Path Delay	46.030ns	23.749ns	48.4% (decrease)	29.555ns	17.442ns	40.98% (decrease)
Number of Slice (LUTs)	263 out of 4656 5%	186 out of 4656 3%	31.5% (decrease)	97 out of 4656 2%	44 out of 4656 0%	54.6% (decrease)
Number of bonded IOBs	64 190 33%	64 out of 190 30%	-	32 out of 190 16%	32 out of 190 15%	-

5. CONCLUSION

This paper has conferred a design of vedic multiplier based on urdhva tiryakbyam sutra of vedic mathematics. A unique complex number multiplication multiplier design based on formulas of the ancient Indian Vedic mathematics which is extremely suitable for high speed complex arithmetic circuits that are having wide application in VLSI signal processing is presented. The reduction within delay is attributed to the diminished consumption of area by the designed multiplier that possess quite lesser number of internal blocks. Our results show that the multiplier based on Urdhva Tiryakbhyam sutra is much more efficient than the standard multiplier in the area occupied.

6. REFERENCE

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