Device design methodology to optimize low-frequency Noise in advanced SOI CMOS technology

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ABSTRACT

Device design methodology for SOI is to improve power and reduce low frequency noise generated randomly. An effort to reduce the power consumption of the circuit, the supply voltage can be reduced leading to reduction of dynamic and static power consumption. SOI introduces one of the greatest future generation technologies of this decade. Silicon-on-Insulator transistors are fabricated in a small ~100 nm layer of silicon, located on top of a silicon dioxide layer, called buried oxide. This oxide layer provides full dielectric isolation of the transistor and thus most of the parasitic effects present in bulk silicon transistors are eliminated. The structure of the SOI transistor is depicted and is very similar to that of the bulk transistor. The main difference is the presence of the buried oxide it provides attractive properties to the SOI transistor. Power has become one of the most important paradigms of design convergence for multi gigahertz communication such as optical data links wireless products and microprocessor ASIC or SOC designs. Power consumption has become bottleneck in microprocessor design.

Keywords: *Floating body effect, SOI, kink effect, edge effect*

1.1 SOI Introduction:

Silicon on Insulator is a semiconductor electronic device which is now used as an integrated chip in almost all highly reliable and efficient in digital as well as analog electronic devices. Before the use of SOI in market BULK technology was leading technology in electronic industry, due to following reasons such as latch up, parasitic capacitance and leakage currents in bulk technology fail to continue in developing highly effective devices. The design rules which help in developing SOI technology was extracted from bulk technology by incorporating oxide layer over the silicon substrate, 50% of the problem was solved such as leakage currents, eliminating wells, scaling of the device effect threshold voltage is reduced and latch up problem. SOI, new device architectures allow optimum electrical properties to be obtained for low power and high performance circuits. In SOI the body terminal is either tied to gate or left free for floating called as floating body as when the floating body is considered it has some important features in reducing power consumption and improving the device efficiency as shown in figure 1.1.

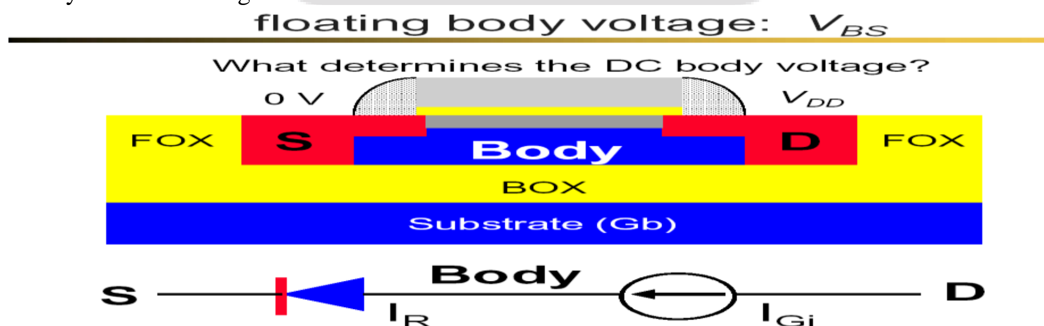


Figure 1.1: Floating body Effect in SOI

Floating body effect (FBE) is the major parasitic effect in SOI-MOSFETs and is a consequence of the complete isolation of the transistor from the substrate. The effect is related to the built-up of a positive charge in the silicon body of the transistor, originating from the holes created by impact ionization.

This charge can not be removed rapidly enough, primarily because no contact with the Si film body is available. There are various consequences of this built-up charge, which are generally referred to as the floating-body effects, such as: kink-effect; negative conductance and transconductance; hysteresis and instabilities, single transistor latch the transistor cannot be turned off by reducing gate voltage, bipolar transistor action, and premature breakdown. The FBE can lead to circuit instabilities, frequency-dependent delay time, and pulse stretching. Many of the negative consequences of the FBE could be eliminated by using a body contact for every MOSFET, but this is generally not an optimum solution. These typical SOI effects can be observed even in the bulk-Si MOSFETs at low temperatures when the substrate becomes semi-insulating and if the substrate contact is left floating.

1.2 SOI Floating Body

In a standard Bulk CMOS process technology, the P-type body of the NMOS Transistor is held at the ground voltage, while in a PMOS Transistor in the Bulk CMOS process technology is fabricated in an N-well, with the Transistor body held at the VDD supply voltage by means of a metal contact to the N-well. In Silicon-On-Insulator process technology, the source, body, and drain regions of transistors are insulated from the substrate. The body of each transistor is typically left unconnected and that results in floating body. The floating body can get freely charged or discharged due to the transients switching and this condition affects threshold voltage Vt and many other device characteristics. The transistor area in SOI process is less because there is no need for metal contacts to Wells used for making MOS transistors.

There are several anomalous electrical behaviours in SOI CMOS devices that arise from these “floating body effects” such as a “kink” in the output. Floating body effects are employed to increase the current output from an SOI CMOS device.

1.3 Floating-Body Effects

When the drain voltage is large enough, the channel electrons can obtain sufficient energy in the high electric field near the drain and to generate electron hole pairs via the impact ionization mechanism. The generated electrons rapidly flow into the drain, and the holes migrate toward the lowest potential region, i.e., the p-type floating body. Then the holes caused at the lowest potential region will be swept into the source since the source or body diode is forward biased.

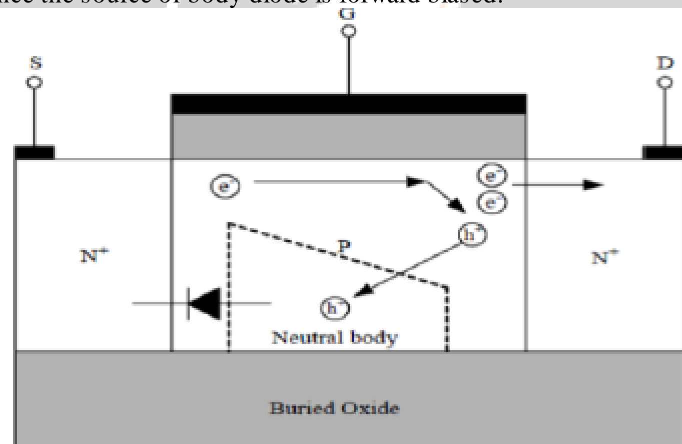


Figure 1.2 Representing FLOATING body effect in PD SOI

There are various consequences of this built up charge, which are generally referred to as the floating-body effects, such as: kink-effect; negative conductance and trans-conductance; hysteresis and instabilities, single transistor latch the transistor cannot be turned off by reducing gate voltage, bipolar transistor action, and premature breakdown. The FBE can lead to circuit instabilities, frequency-dependent delay time, and pulse stretching. Many of the negative consequences of the FBE could be eliminated by using a body contact for every MOSFET, but this is generally not an optimum solution. It should be noted that these typical SOI effects can be observed even in the bulk-Si MOSFETs at low temperatures when the substrate becomes semi-insulating and if the substrate contact is left floating. Considering the MOS portion of the partially-depleted SOI NMOS device, the threshold voltage is subject to the floating body effect. The accumulated holes near the body-emitter junction in the thin-film due to the parasitic bipolar device caused by the floating body increase the body-emitter voltage (VBE). As a result, the threshold voltage is lowered. Considering this effect, the threshold voltage

model (VT) and the conducting current through the font channel ICH under the front gate oxide have been found.
The current conduction mechanisms for the MOS portion and the parasitic bipolar portion of the partially-depleted SOI NMOS device have been checked. The temperature-dependent kink effect model is derived for the device biased in the triode region (VDS_VDSAT) and the saturation region (VDS> VDSAT).

1.4 Triode Region VDS_VDSAT: Figure 1.2 shows the current conduction mechanism of the partially – depleted SOI NMOS device biased in the triode region. In the front channel region near the drain, there is no impact ionization. Therefore, no holes are injected into the floating body. As a result, the body-emitter voltage (VBE) is small. The parasitic bipolar device does not turn on. Under this situation, the floating body can be regarded as two diodes connected back to back. At the body-emitter junction, which is forward biased, the conducting current is IF. At the body-collector junction, which is reverse biased, the conducting current is IR. Considering the impact ionization effect at the body-collector junction, the conducting current magnified by a fact of MB, the conducting current becomes MBIR. Considering the current conduction of the parasitic bipolar device (IF=MBIR), the body-emitter voltage can be obtained

$$V_{BE} = \frac{2kT}{q}\ln[\frac{-I_{reco} + \sqrt{I_{reco}^2 + 4I_{ES}M_B(I_{gen} + I_{diff})}}{2I_{ES}}]$$

1.5 Saturation Region VDS>VDSAT: For the partially-depleted SOI NMOS device biased in the saturation region, the current conduction mechanism due to VDS>VDSAT, the impact ionization in the front channel region near the drain is less. As a result, a large amount of holes due to the front channel impact ionization are injected into the floating body. Consequently, the accumulated holes near the body-emitter junction voltage VBE becomes large. In the saturation region, VBE can be expressed as

$$V_{BE} = V_{BE1} + V_{BE2} - (V_{BE1} + V_{BE2})^{1/n}$$

Where VBE1 is the VBE when recombination current dominates the parasitic bipolar device; VBE2 is the VBE when diffusion current dominates the parasitic bipolar device. The drain current of the partially depleted, SOI NMOS device is composed of the front channel current in the front MOS portion and the collector current in the bottom parasitic bipolar device. The above formulas are the closed-form analytical temperature-dependent kink effect model for the partially-depleted SOI NMOS device. In order to estimate the Floating body voltage, especially its transient characteristics in PD-SOI circuits, a physics-based models consisting of the body capacitance associated with the body region and various current components is considered. The equivalent circuit representation of the PD-SOI NMOSFET is shown in Fig. 1.3. The transient Floating body (node B) potential VB (t) can be determined from the net current and the time-varying body capacitances as follows:

$$\frac{dQ_B(t)}{dt} - I_{ii}(t) - I_{diode}(t) + I_h(t) = 0, C_B(t) = C_{of} \| C_{ch}(t) + C_{js}(t) + C_{jd}(t) + C_{ob}$$

where Iii(t), Idiode(t), and Ih(t) represent the impact ionization current in the body-drain junction, the net electron current component iB(t) and iC(t) into floating region which is the base region of the parasitic npn bipolar transistor, and the out-going hole current from the body-source junction, respectively.

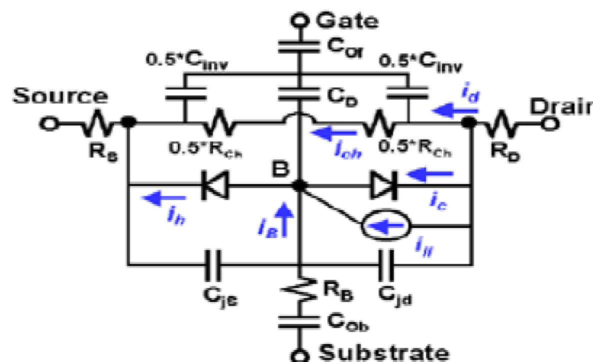


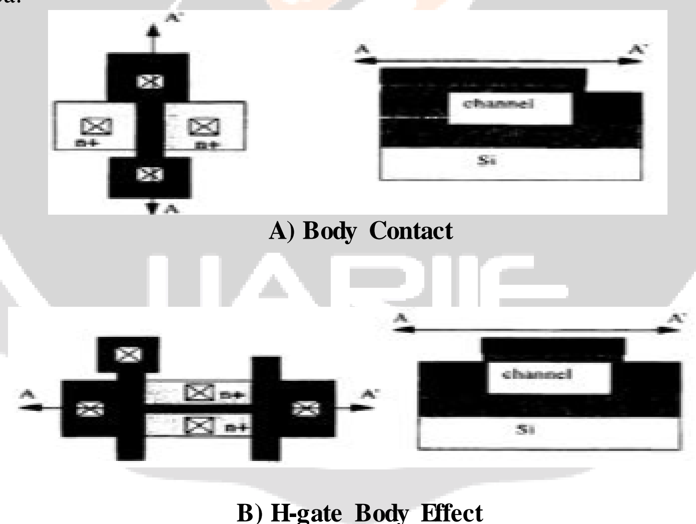
Figure 1.3 Equivalent circuit and floating body current components for the PD-SOI NMOSFET model

1.6 METHODS FOR REDUCING FLOATING BODY EFFECTS

In order to achieve the full potential of SOI technology, it is increasingly important to reduce the floating body effects.

1.7 Body contact

In the digital circuits, the transistor operates as a switch and remains in a steady state most of the times. Modelling switching characteristics with Floating Body effects are slightly complicated, but it can be modelled. Where as in the Analog/Mixed/IO design modelling the behaviour of linear characteristics circuit is very difficult with varying potential of the Floating Body as it changes the output impedance of the device and its Vt-matching to the next device. A Body Contact Transistor can be used as the current source or as any matching transistors designs to eliminate the floating body effect in the SOI technology. However Body Contact has RC delay associated with it, and shows poor transient response due to high capacitance and resistance. Also Body Contacts do not scale with the Gate Length, and requires bigger Transistor size and Low density. Body contacts are used only where needed because they increase the layout area and decrease performance.
Contacting silicon underneath the gate region to the ground effectively suppresses the kink effect as well as the parasitic lateral bipolar effects. Several schemes exist to provide the transistor with body contact. Figure 1.4 (a) shows the normal body contact. It consists of a *P*+ region which is in contact with the P-type silicon underneath the gate. However, in transistors with a large gate width, the presence of single body contact at one end of the channel may not be sufficient to suppress the kink and BJT effects, especially when considering the high resistance of the weakly doped channel region. The H gate MOSFET design is shown in Figure 1.4 (b). It helps to solve this problem, since body contacts are presented at both ends of the channel. However, the efficiency of such a contact scheme depends on channel resistance, which is usually very high in modem processes. In addition, such body contacts occupy a lot of area.

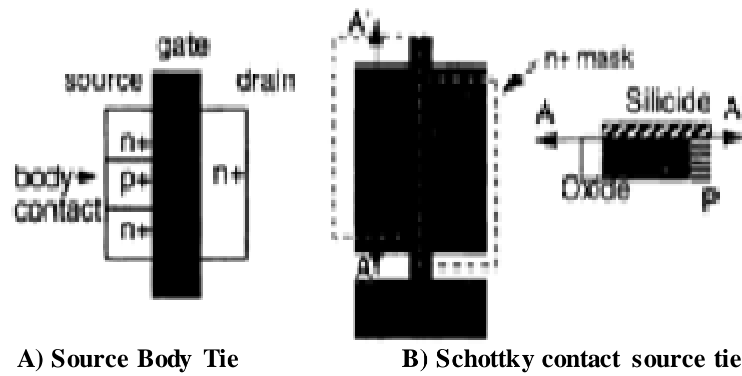


A) Body Contact

B) H-gate Body Effect

Figure 1.4 NMOS Transistor with body contact and H-gate Body Effect

1.8 Source Body Tie Structure: A more compact method, source body tie structure, has been proposed by Omura and Izumi. Figure 1.5 (a), the P+ body ties are created on the side of the N+ source diffusion. If the device width is large, additional P+ regions can be formed in the source such that a P+ N+ P+ N+ structure is introduced. Such a device has the main drawbacks of being asymmetrical source and drain cannot be switched, and the effective channel width is smaller than the width of the active area. An alternative method involving Schottky contact in source drain region has been proposed by Sleight and Mistry as shown in Figure 1.5(b). It provides symmetrical operation. However, increased leakage current associated with Schottky contact degrades device performance.



A) Source Body Tie **B) Schottky contact source tie**

Figure 1.5 Source Body Tie and Schottky contact source tie

These methods are effective in reducing the floating body effects but have either a limited area of applications or they cannot fully fulfil the advantages of the SOI structure. In FDSOI n-MOSFET has lower leakage current than PDSOI n-MOSFET. The leakage current is inversely proportional to the threshold voltage, channel length and gate oxide thickness. The threshold voltage in PD SOI n-MOSFET is more than that of FDSOI n-MOSFET. The main drawback in PDSOI n-MOSFET is kink effect, which is eliminated in FDSOI n-MOSFET. A careful trade-off between these two effects must be achieved in order to optimize the circuit performance.

1.9 Edge Effects

The lateral edges of the SOI MOSFETs represent a parasitic conduction path between the source and the drain. This sidewall transistor operates in parallel with the main transistor, and strong coupling and charge sharing between the front, back, and the edge channels dictate its threshold voltage. Special edgeless devices e.g. H-gate transistor, which has two p+ body contacts that inhibit any conduction path along the sidewalls may be designed, but this is a space-consuming alternative.

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