ENHANCEMENT OF VOLTAGE GAIN AND REDUCTION IN THD BY THIRD ORDER ONE SIXTH HARMONIC INJECTION TECHNIQUE

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ABSTRACT

In this paper, a new inverter topology called switched capacitor model and a PWM technique called Third order one sixth harmonic injection technique (THIM) for enhancing the voltage gain and reduction in Total Harmonic Distortion (THD) is proposed. This topology is designed based on switched-capacitor technique and the number of output levels is determined by the number of switched-capacitor cells. Only one dc voltage source is needed and the problem of capacitor voltage balancing is avoided as well. This structure is not only very simple and easy to be extended to higher level, its gate driver circuits are also simplified because the number of active switches is reduced.

Keyword : - *THD, inverter, voltage gain, third order one sixth harmonic injection, harmonic reduction*

1. INTRODUCTION

With the increasingly higher power quality requirement for numerous industrial applications and renewable energy sources such as photovoltaic, wind and fuel cells, Classical three level inverters have difficulty to meet these requirements of clean non-polluted sinusoidal waveforms and minimal distortion factor. As a result, multilevel inverters have been introduced as an alternative in high power quality situations. For several attractive features such as near sinusoidal staircase output voltage waveforms, reduced dv/dt stresses and operating with lower switching frequency stress etc. multilevel inverters, as an alternative solution, have been receiving much attention. As results, many different topologies and wide variety of control strategies have been proposed. Conventionally, multilevel inverter topologies can be divided into three categories: neutral-point-clamped flying capacitors and the H-bridge cascade. In many industrial applications, these inverters have been playing very important in the terms of high quality ac supplies and motor driver because of their good performance. However, their drawbacks are also apparent. For instance, multiple separated voltage sources are required for the H-bridge cascade topologies. And the problem of voltage balancing among dc link series capacitors exists in both neutral-point-clamped and capacitor-clamped inverters. To overcome these drawbacks, a new multilevel topology based on switched capacitor technique has been applied in many applications in which a multilevel DC-DC convertor and full bridge is connected. In this topology only one DC voltage source is required and many other problems such as voltage balancing, numerous active switches and complex gate driver circuits are avoided as well. The DC-DC conversion sections is the key

point of the whole topology which is designed by connecting multiple SC cells. Consequently the output voltage levels of the proposed inverter could be varied flexibly by employing different number of SC cells.

Switched capacitor multilevel inverter is a combination of a DC-DC converter and full bridge rectifier. The DC-DC conversion section is the key point for these inverters which is designed by connecting multiple switched capacitors cells. Each switched capacitor cell consists of a capacitor, an active switch and two diodes. This topology reduces problems such as voltage balancing, numerous active switches and complex gate driver circuits. Switched capacitor multi level inverters are designed based on the switched-capacitor technique and the number of output levels is determined by the number of switched-capacitor cells. Only one dc voltage source is needed and the problem of capacitor voltage balancing is avoided as well. This structure is not only very simple and easy to be extended to higher level, its gate driver circuits are also simplified because the number of active switches is reduced.

2. CONVENTIONAL METHOD WITH ELEVEN LEVEL CONVERTER

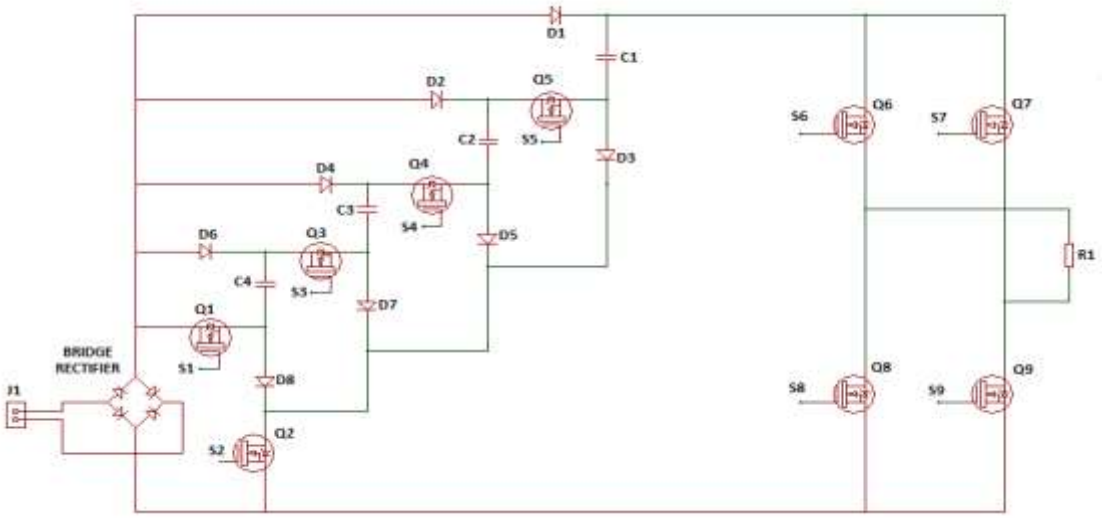

Fig -1: Circuit diagram of existing system with eleven level converter

The Figure 2 shows the circuit diagram of the existing system which consists of 9 MOSFET switches, a power supply and a resistive load. Five MOSFET switches (Q1, Q3, Q4, Q5, Q2) are used at the boosting side of the inverter and four MOSFET switches (Q6, Q7, Q8, Q9) are used at the load side of the inverter. The switches Q1, Q3, Q4, Q5, Q2 are used for the various modes operations of the inverter. The switches on the load side are used to carry out the positive and negative cycles of the output voltage way form of the existing system. The pulses for the various MOSFET switches are given from the gate driver circuits using the SPWM (Sinusoidal Pulse Width Modulation) technique. Disadvantages of existing system are as follows: High harmonic content when implemented with SPWM (Sinusoidal Pulse Width Modulation) technique, Need of boost converter to increase the voltage gain when switches are added to increase the level and more switching losses.

3. PROPOSED SYSTEM WITH THIRTEEN LEVEL INVERTER

The proposed system is implemented with a different PWM technique called 3rd order 1/6th harmonic injection method for the switching sequence of the inverter and the level is increased up to thirteen. With this new technique the switching sequence of the inverter is made more effective compared to SPWM technique. Due to effective switching sequence the THD (Total Harmonic Distortion) also known as distortion factor is reduced to a greater extent. The output waveform will be almost sinusoidal. . The injection of 3rd order 1/6th harmonics is done through the programming in the micro controller.

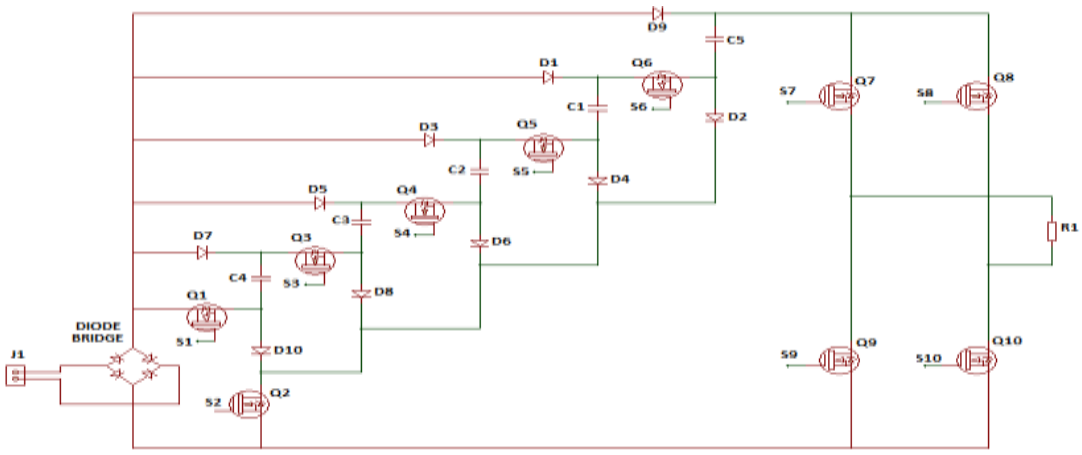

Fig -2: Circuit diagram of proposed system

Figure 2 shows the circuit diagram of the proposed system. It consists of 10 MOSFET switches in which 6 MOSFET switches (Q1, Q2, Q3, Q4,Q5,Q6) are connected in the boosting side of the inverter and 4 MOSFET switches (Q7, Q8, Q9, Q10) are connected at load side of the inverter. The load used is a resistive load. A new PWM technique named 3rd 1/6th harmonic injection technique (THIM) is implemented to give the switching pulses for the MOSFET switches in the inverter.

4. THIRD ORDER ONE SIXTH HARMONIC INJECTION METHOD (THIM)

The third harmonic PWM is implemented in the same manner as sinusoidal PWM. The difference is that the reference AC waveform is not sinusoidal but consists of both a fundamental component and a third harmonic component. As a result, the peak to peak amplitude of the resulting reference function does not exceed the DC supply Vs, but the fundamental component is higher than the available supply Vs. The reference voltage Vref is added with signal having frequency three times of fundamental frequency and the magnitude is 1/6th of the fundamental amplitude.

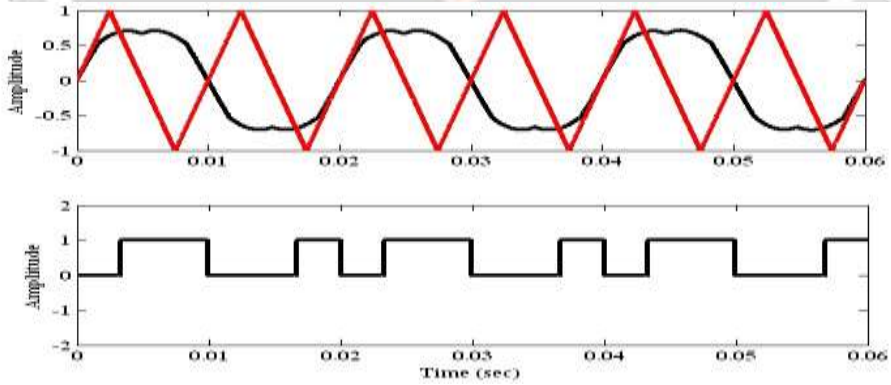

Fig 3: Carrier and reference waveform along with the pulses of Third Harmonic Injection Pulse Width Modulation

Figure 3 shows the carrier and reference waveform along with the pulses of third harmonic injection pulse width modulation. The generation of the phase voltage wave form having no third harmonics can be generated by addition of the third harmonics in the sinusoidal reference waveform. These additions of the various amounts of third, ninth, fifteenth etc. harmonics is used to produce flat-topped phase waveforms which improves the efficiency of the class B inverters. The optimal amount of third harmonic should extent the ratings of all PWM inverters.

Vs	SWITCHING SEQUENC OF 10 SWITCHES									
	Q 1	Q 2	Q 3	Q 4	Q 5	Q 6	Q 7	Q 8	Q 9	Q 10
+Vdc 1	1	0	0	0	0	0	1	0	0	1
+Vdc 2	0	1	0	0	0	0	1	0	0	1
+Vdc 3	0	0	1	0	0	0	1	0	0	1
+Vdc 4	0	0	0	1	0	0	1	0	0	1
+Vdc 5	0	0	0	0	1	0	1	0	0	1
+Vdc 6	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	1	1	0	0	0	0
-Vdc 6	0	0	0	0	0	1	0	1	1	0
-Vdc 5	0	0	0	0	1	0	0	1	1	0
-Vdc 4	0	0	0	1	0	0	0	1	1	0
-Vdc 3	0	0	1	0	0	0	0	1	1	0
-Vdc 2	0	1	0	0	0	0	0	1	1	0
-Vdc 1	1	0	0	0	0	0	0	1	1	0

Table 1: Switching operation

The best modification that can be made to the inverter phase output waveform is assumed a priori to be the addition of a measure of third harmonics.

The desire waveform is of the type

$$y = \sin \omega t + A sin 3\omega t \tag{1}$$

Where A is to be determined for the optimal of y

The optimal injection is obtained by differentiating the above equation (1)

$$\frac{dy}{dt} = sin\omega t + 3Acos3\omega t = 0 \tag{2}$$

The optimum value of A is that value which minimises dy/dt and can be found by differentiating the expression for dy/dt and equating it to be zero as shown in above equation (2). Thus the values of A are

A= -1/3 and A=1/6

The value of dy/dt cannot be greater than unity for this reason the value A=-1/3 is discarded. The required value of A =1/6 and the required waveform is

$$v = sin\theta + \frac{1}{6}sin3\theta \tag{3}$$

Table 1 shows the switching operation and thus the switching strategy for each level is explained below.

4.1 MODE 0

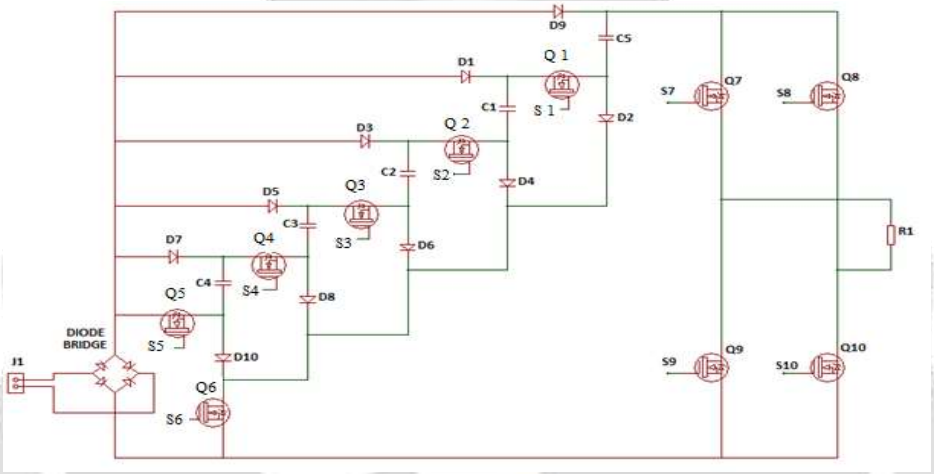

Fig 4: Mode 0 operation of the thirteen level inverter

During this mode switches Q5 and Q6 are ON and diode D10 is conducting. So no output voltage flows to the inverter switches (Q7, Q8, Q9, Q10). During this mode no capacitor in the boosting side of the inverter gets charged. The output voltage is 0.

4.2 MODE 1

In this mode when the input voltage of 24 V is applied the diode D 9 conducts and capacitor C 5 gets harged .The output voltage is +Vdc. To obtain this voltage switches Q7 and Q10 are turned ON.

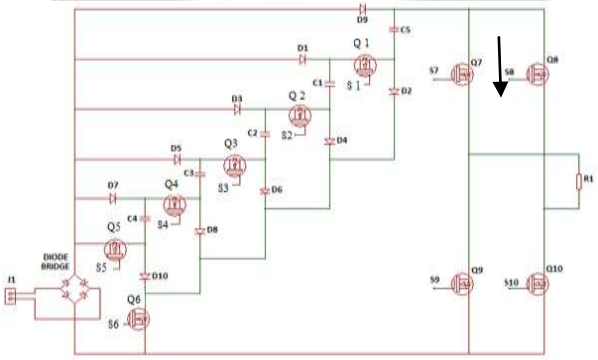

Fig 5: Mode 1 operation of thirteen level inverter

4.3 MODE 2

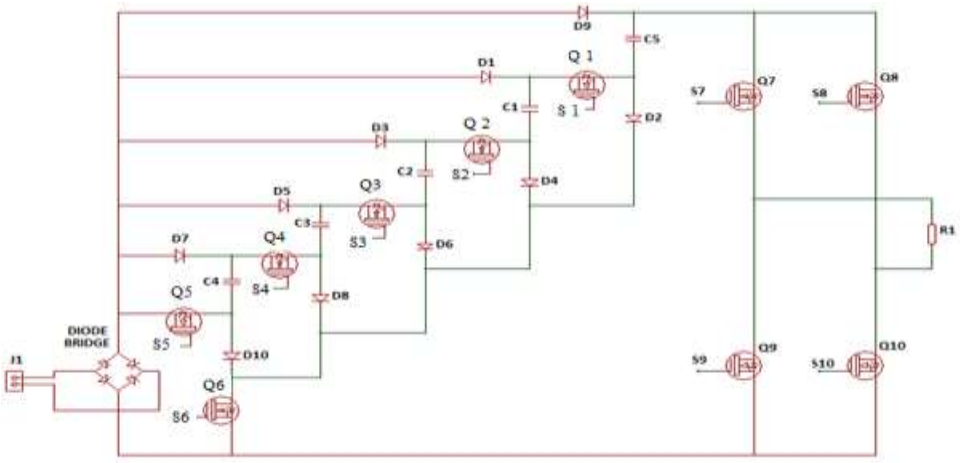

Fig 6: Mode 2 operation of thirteen level inverter

When the input voltage of 24 V dc is applied, diode d1 conducts and capacitor C 1 gets charged. Thus the output voltage becomes +2Vdc.This voltage turns on the switch Q1. To obtain this voltage +2Vdc (48 V), the switches Q7 and Q10 are turned ON.

4.4 MODE 3

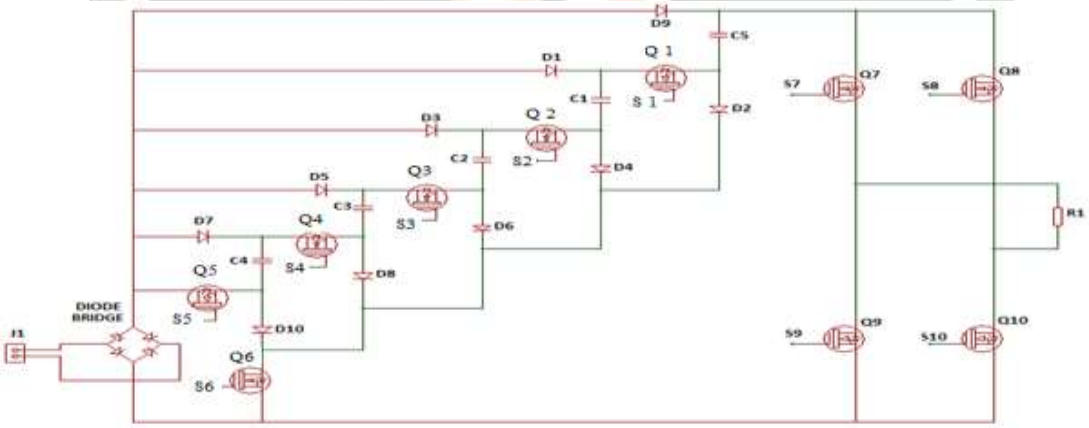

Fig 7: Mode 3 operation of thirteen level inverter

When the supply DC voltage of 24 V is applied, capacitor C 2 gets charged. The output voltage becomes +3Vdc. This voltage turns on the switch Q2. To obtain this voltage +3Vdc (72 V), the switches Q7 and Q10 are turned ON.

4.5 MODE 4

When the 24 V DC input is supplied, the capacitor C 3 gets charged. The output voltage becomes + 4Vdc. This voltage turns ON the switch Q3. To obtain this voltage + 4 Vdc (96 V), the switches Q7 and Q10 are turned ON.

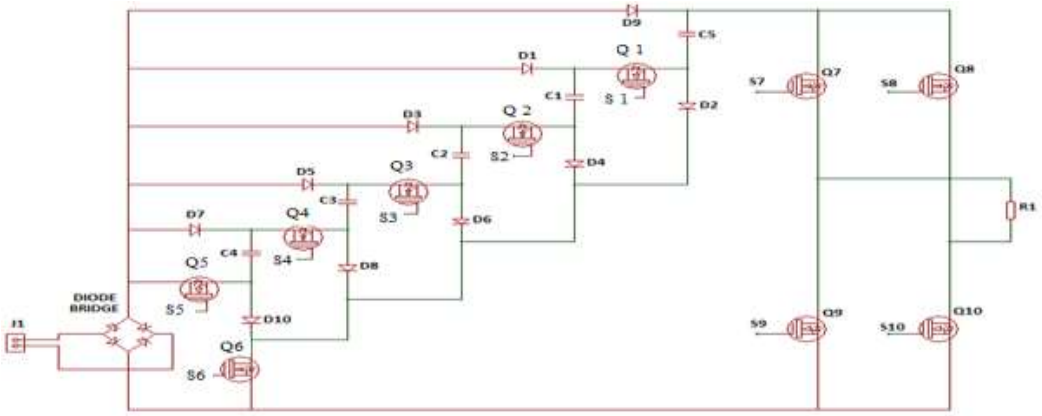

Fig 8: Mode 4 operation of thirteen level inverter

4.6 MODE 5

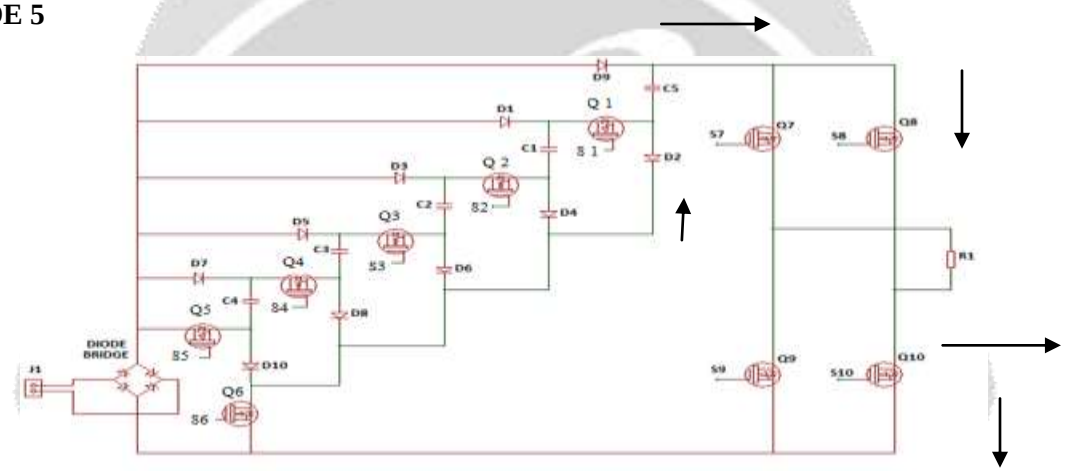

Fig 9: Mode 5 operation of thirteen level inverter

When the input DC supply of 24 V is given capacitor C 4 gets charged. The output voltage becomes +5Vdc. Thus voltage turns ON the switch Q4. When this switch is turned ON, the voltage at the capacitor gets increased to about 120 V (+5Vdc).

4.7 MODE 6

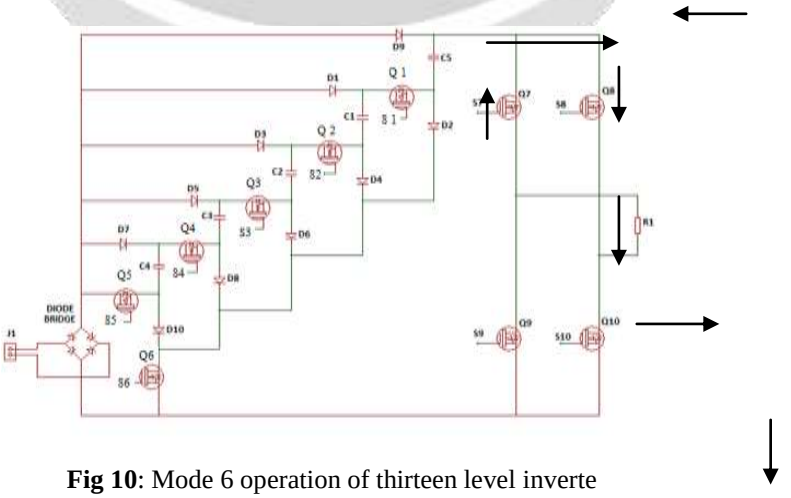

Fig 10: Mode 6 operation of thirteen level inverte

When the input 24 V dc supply is given , the switch Q 5 gets switched ON, the switch Q 6 gets turned OFF .Thus the voltage at the capacitor C 5 becomes 144 V(+6Vdc).

4.8 ADVANTAGES OF THE PROPOSED SYSTEM

- Pure sine wave is achieved
- No complex filter design is required
- Harmonic content is reduced to a greater extent
- Increased voltage gain without the need of boost converter

5 SIMULATION OF 3RD ORDER 1/6TH HARMONIC INJECTION TECHNIQUE

5.1 SIMULATION OF ELEVEN LEVEL INVERTER

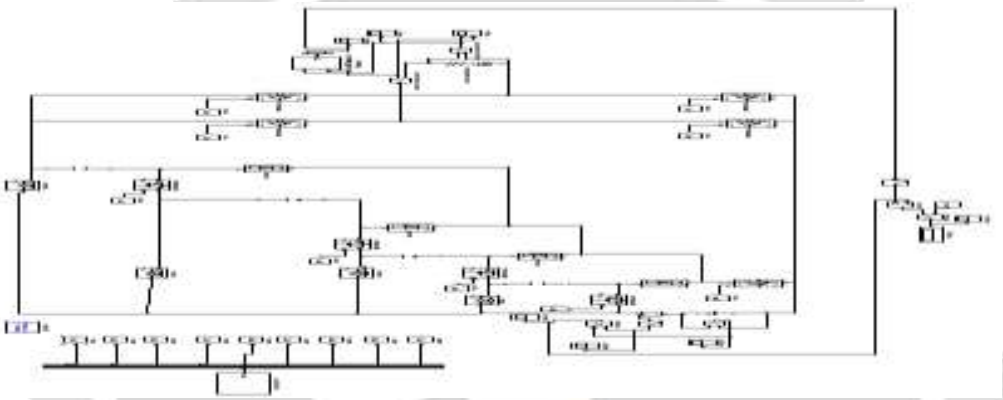

Fig 11: Simulation Circuit Diagram of the Conventional eleven level inverter

Figure 12 consists of DC source of 24V as input and nine switches. Here in order to increase the level we have to go for more number of switches.

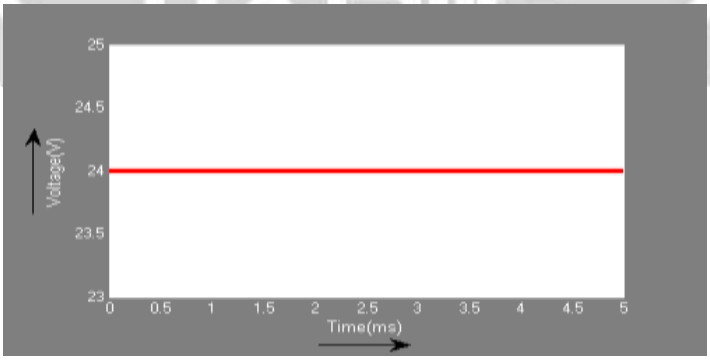

Fig 12: Input voltage waveform of conventional method

Figure 13 shows the input DC voltage of 24 V supplied to the nine switches at the boosting side of the inverter.

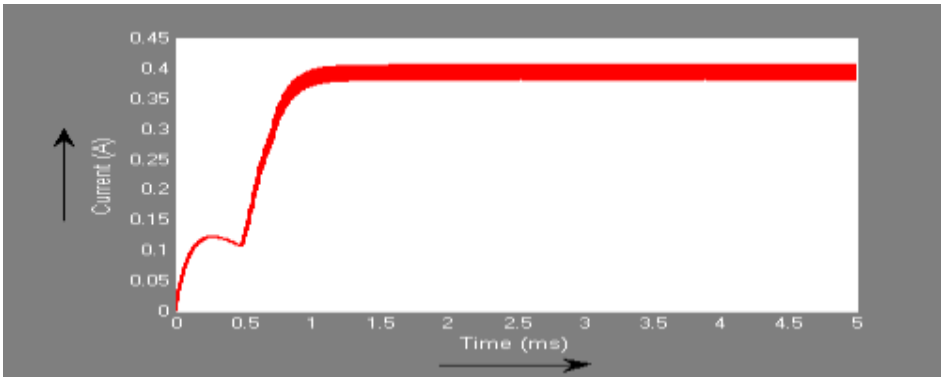

Fig 13: Input current waveform of conventional method

Figure 13 shows the input current of 0.4 A supplied to the conventional eleven-level inverter .

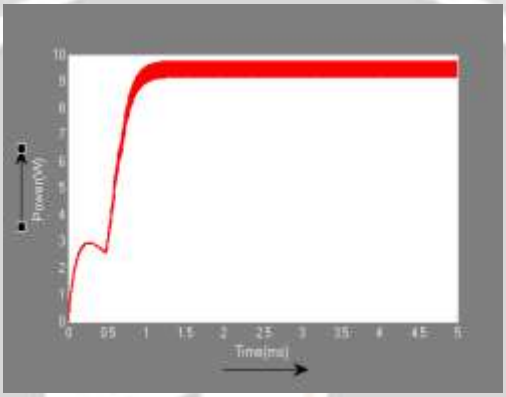

Fig 14: Input power of conventional method

Figure 14 shows the input power rating 9.8 W supplied to the eleven level inverter.

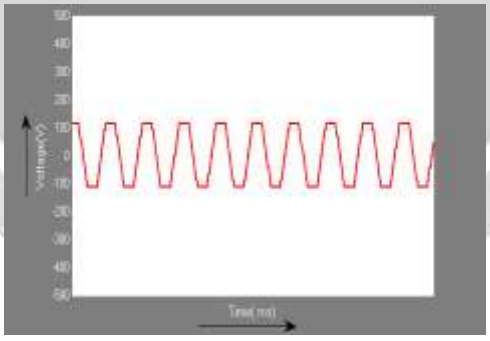

Fig 15: Output voltage waveform of conventional method

Figure 15 shows the output voltage waveform of conventional eleven level inverter. The output voltage is about 110 V.

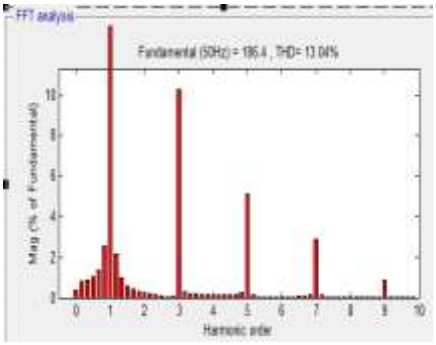

Fig 16: THD of the conventional method

Figure 16 shows the total harmonic distortion of the conventional method and THD% is 13.04%.

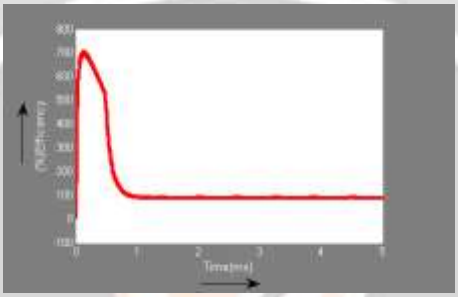

Fig 17: Efficiency of the conventional method

Figure 17 shows the efficiency of the conventional method of about 87.31%.

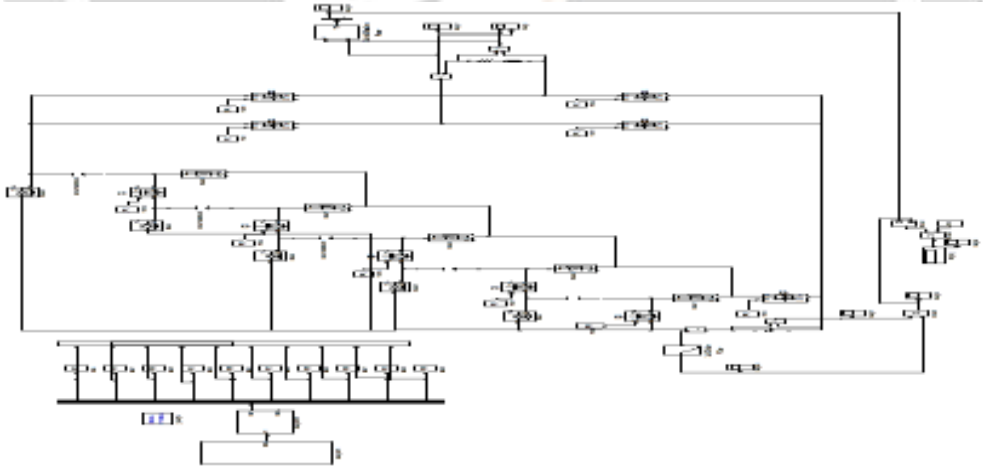

Fig 18: Simulation Circuit Diagram of the proposed thirteen level inverter

5.2 SIMULATION OF THIRTEEN LEVEL INVERTER

24 V DC supply is given to 10 MOSFET switches as shown in the above circuit diagram. A new PWM technique named 3rd order 1/6th harmonic injection is used to provide the gate pulses for the switches in the thirteen level inverter. The harmonic injection block is shown below.

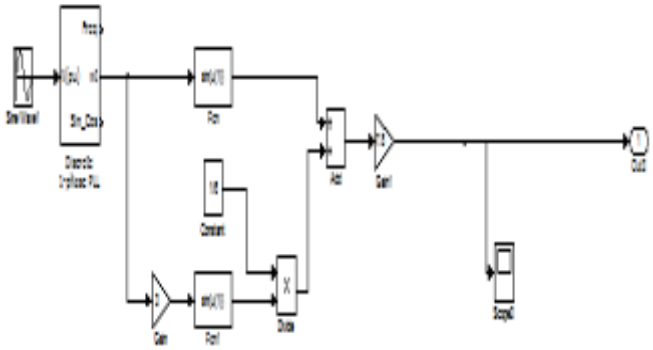

Fig 19: Harmonic injection block of the proposed system

Figure 19 shows the harmonic injection block in which the reference sinusoidal wave $v=v_m \sin(\omega t)$ is injected with the 1/6th 3rd order harmonics by using the formula $v= \sin(\omega t)+1/6\sin(3\omega t)$. The reference wave after the injection of the harmonics is displayed in scope 3 as shown in the above figure. The reference wave is shown in the figure below

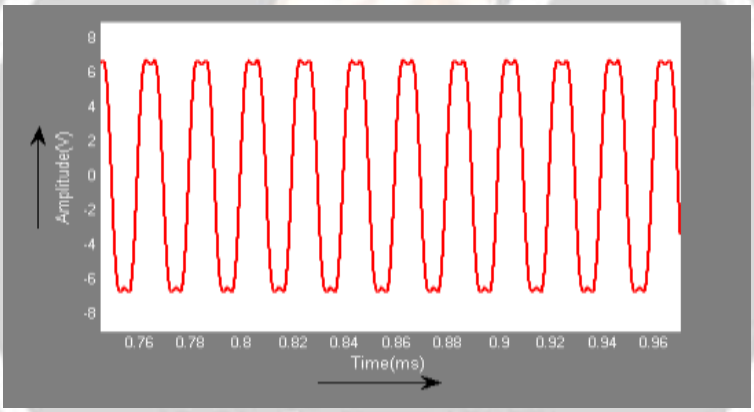

Fig 20: Reference wave after harmonics injection

Figure 20 shows the reference wave after the injection of the 3rd order 1/6th harmonics.

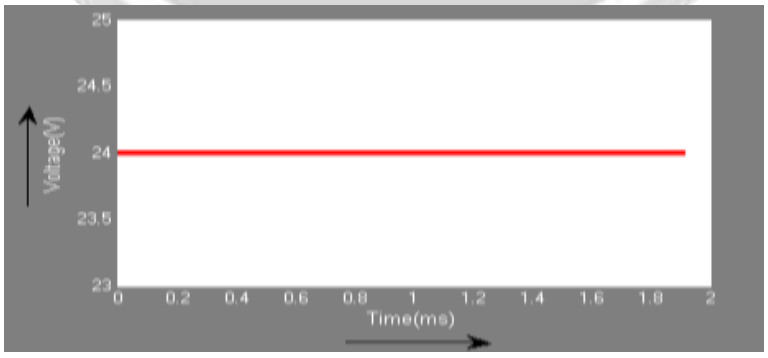

Fig 21: Input voltage waveform of the Proposed System

Figure 21 shows the input voltage of about 24 V DC supplied to the proposed thirteen level inverter.

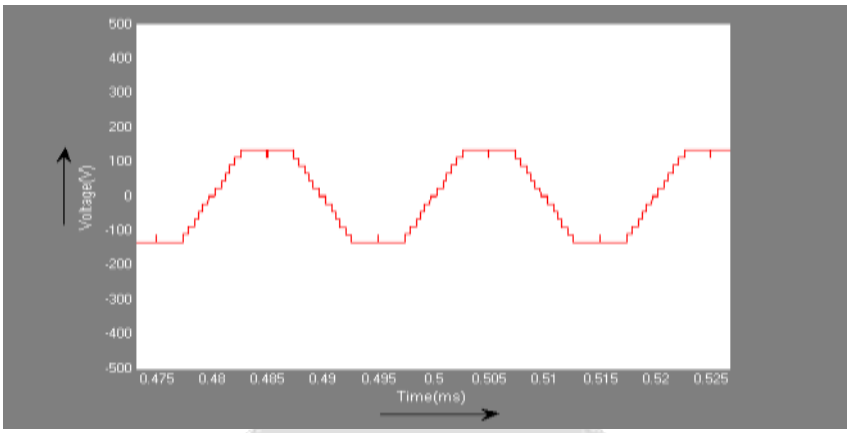

Fig 22: Output voltage waveform of proposed system

Figure 22 shows the output voltage waveform of 13 level inverter. It is a staircase waveform with 13 levels from peak to peak. It is observed that as the level increases the waveform looks like sinusoidal waveform. The voltage gain is increased to 140 V compared to the voltage gain in existing system.

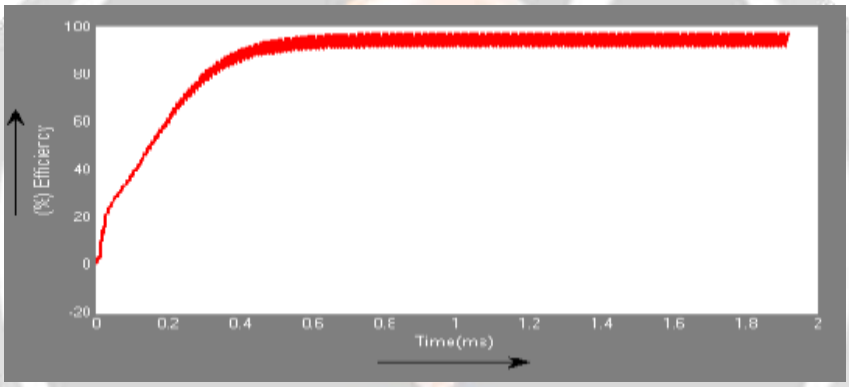

Fig 23: Efficiency of the proposed system

Figure 23 shows the efficiency of the proposed system which is found to be 84%. It is observed that the efficiency of the proposed system is higher than the existing system.

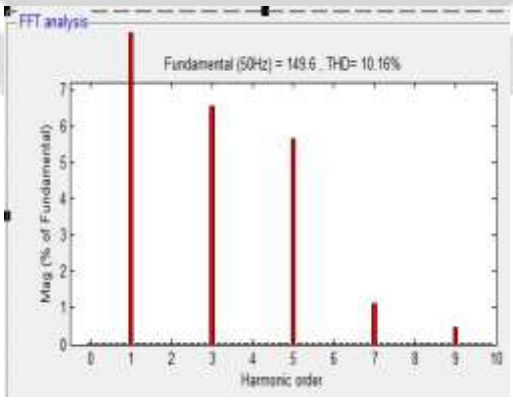

Fig 24: THD of the proposed system

Figure 24 shows the total harmonic distortion of the proposed method and THD % is 10.16%. It is observed that the % THD is reduced to a greater extent compared to the %THD in the existing system.

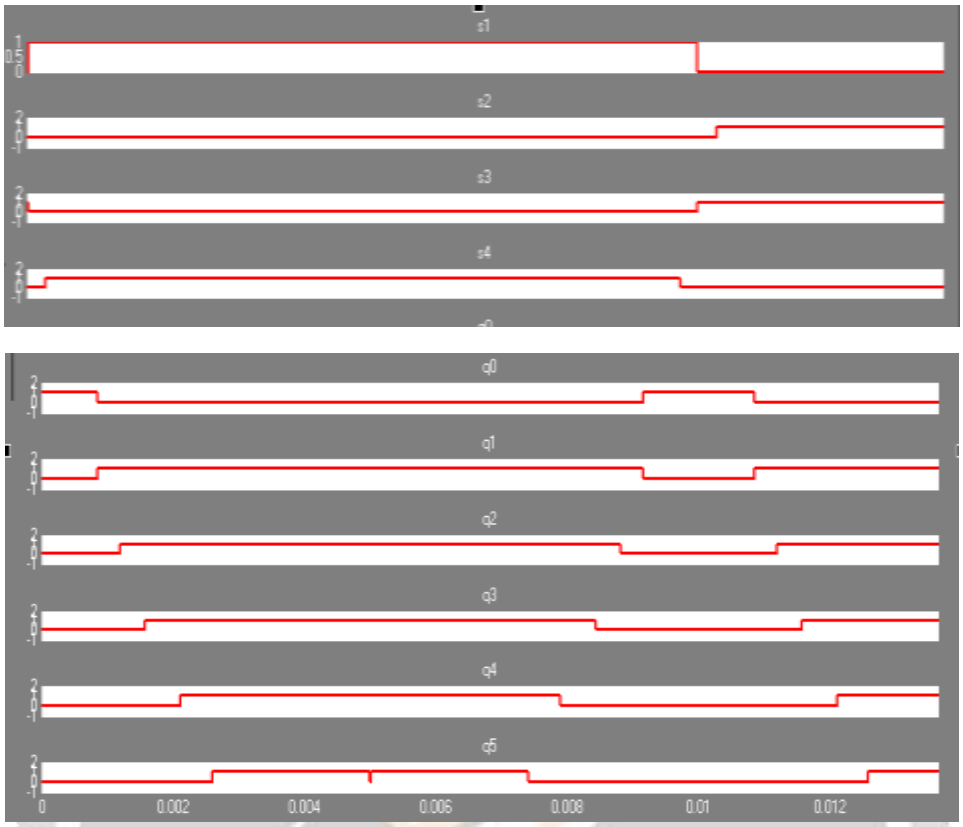

Fig 25: Triggering Pulses

Figure 25 shows the triggering pulses for each MOSFET and the pulses are given by using PWM (Pulse Width Modulation technique). There are 4 gate driver circuits used to supply the triggering pulses to the switches.

6. HARDWARE IMPLEMENTATION OF 3RD ORDER 1/6TH HARMONIC INJECTION TECHNIQUE

The hardware comprises of the following components,

- Power supply.
- Inverter.
- Power MOSFET.
- Isolation circuit.
- 16F877A microcontroller.

Hardware is designed in order to produce 13 different levels of AC output from a single DC source. This is made possible by the different switching mechanisms by using Pulse Width Modulation technique. The gate pulses are produced using gate driver circuits. The control to the entire system is done by using Microcontroller. The dc supply of 5 V and 12 V is given to the gate driver circuit. Thus by increasing the levels we can reduce the harmonics to a greater extent.The power circuit consists of ten MOSFET switches. The output is increased by transformers of different turns ratio and the load used is a resistive load. The Controller circuit consists of microcontroller 16F877A. It is a 40 pin IC with 4 ports of each 8 bit. The ports are used to give the input signal and the output is fetched. A crystal oscillator is connected to the microcontroller which is used to define the speed of the controller. . The gate driver IC used is IR2110. The opto isolator used is TLP250. The supply to the IC's are given using two step down transformers (5 volt and 12 volt).The voltage from the power circuit may damage the microcontroller. So, in order to protect the microcontroller from damage the isolation circuit is connected between the power circuit and

the controller. The output current gain of the pulse is very low, therefore the buffer circuit is connected for current amplification.

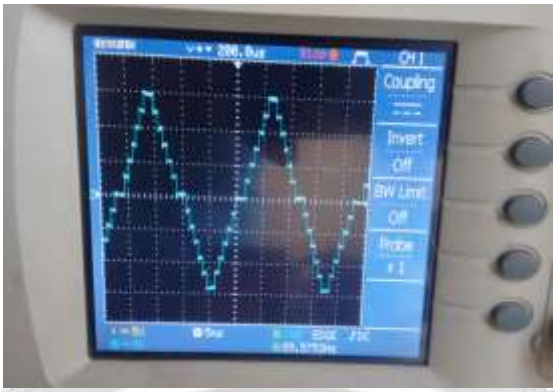

Fig 26: Hardware output voltage waveform

Figure 26 shows the Hardware Result of the proposed 13 level inverter. The output voltage waveform is displayed in the DSO (Digital Storage Oscilloscope).

7. CONCLUSION

In this paper, a novel thirteen level inverter was proposed and compared with conventional eleven level inverter, the proposed inverter can greatly decrease the number of switching devices. Comparing with traditional cascaded multilevel inverter, the number of voltage levels can be further increased by this topology and with the increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology. This project mainly analyzes 13 level inverters. The method of analysis and design is also applicable to other members of the proposed inverter.

8. REFERENCES

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