Effective comparison of various types of Analog to Digital converters based on performance and parameters

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ABSTRACT

The performance of the analog-to-digital converters has become very important in signal processing applications. It provides a link between analog world transducers and digital world signal processing and data handling. Signal processing is very important in many of the system-on-a-chip applications. Analog-to-digital converters (ADCs) are a mixed-signal device that converts analog signals which are real-world signals to digital signals for processing the information. A paper present review study of the most popular type of Analog to Digital Converters like flash, pipelined, sigma-delta and successive approximations. The paper represents the fundamental operating principles of these architectures with the sources of error, so that the user can conveniently choose between various ADCs available for their application. At last comparison between all analog-to-digital converters is also discussed.

Keywords: Flash ADC, Pipelined ADC, Successive Approximation ADC, Sigma Delta ADC

1. INTRODUCTION

In the past few years, the need to design a low voltage, low power, high speed, and wide bandwidth analog-to-digital converter (ADC) has increased exponentially. So, basically Analog-to-Digital Converters (ADC) translate analog electrical signals for data processing purposes. With products matching performance, power, cost, and size needs, Analog Devices offers the industry’s largest A/D converter portfolio. As the world’s leading provider, these data converters enable accurate and reliable conversion performance in a range of applications such as communications, energy, healthcare, instrumentation and measurement, motor and power control, industrial automation, and aerospace/defence. A variety of A/D converter resources are provided to assist the engineer in every project phase, from product selection to circuit design. These are the basic building blocks that provide an interface between an analog world and the digital domain. As it is the main block in mixed-signal applications, it becomes a basic need in data-processing applications and limits the performance of the overall system.

In this paper we present a number of A/D converter architectures. We discuss different architecture of ADCs that include Flash, Pipeline, Sigma-Delta and Successive Approximation ADCs.

2. ADC Architecture

Currently, there exists a variety of ADCs with different architectures like Flash ADC, pipelined ADC etc, accuracies power consumptions, specifications, sampling rates, resolutions and temperature ranges. These ADCs are used in various different applications according to the characteristics of ADCs.

Since the performance resolution, sampling rate and power consumption of an ADC is basically determined by its architecture, one single ADC type cannot cover all applications. For instance, flash (parallel) ADCs can be used in high speed and low resolution applications. Because of its parallel architecture, all conversions are done in one cycle with many comparators. Whereas, a successive approximation ADC can be used in low-speed and high-resolution applications since the conversions are done in many cycles with only one comparator. That is why, it is important to select a proper ADC for each particular application.

3. Types of ADCs

Among the various types of ADC architectures, there are four most popular ADC architectures currently used. These are as follows:
1) Flash ADC  
2) Pipelined ADC  
3) Sigma delta ADC  
4) Successive approximation ADC

3.1 FLASH ADC

A flash ADC is also known as a direct-conversion ADC is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors. The modern implementations show that capacitive voltage division is also possible. The output of these comparators is generally fed into a digital encoder, which converts the inputs into a binary value (the collected outputs from the comparators can be thought of as a unary value). The flash ADC is known for its fastest speed when compared to other ADC architectures. Therefore, it is used for high-speed and very large bandwidth applications such as high-density disk drives, radar processing, digital oscilloscopes, and list goes on.

The flash ADC is also known as the parallel ADC because of its parallel architecture.

![Block Diagram of Flash ADC](image)

The above figure i.e. Fig.1 represents a typical flash ADC block diagram. This architecture needs $2^n - 1$ comparators for an n-bit ADC. For e.g., a set of 255 comparators are used for 8-bit flash ADC. Each comparator has a reference voltage that is provided by an external reference source. These reference voltages are equally spaced by VLSB from the largest reference voltage to the smallest reference voltage. An input or precisely analog input is connected to all comparators so that each comparator output is produced in one cycle. The digital output of the set of comparators is changed into a binary code through the encoder.

3.1.1 Design Considerations and Implications

The flash ADC basically have high speed conversion because of it’s parallel structure. As resolution increases flash ADC needs large number of comparators. For e.g., a 8-bit flash ADC needs 255 comparators, while 10-bit flash ADC need 1023 comparators. The increase in comparator will increase die size and power consumption. The above thing represents technique for reducing circuit complexity for encoder design.

3.1.2 Error Sources in Flash ADC

- Metastability

When a digital output of a comparator is ambiguous i.e. neither a one nor a zero, the output is defined as metastable. Metastability can be reduced by allowing more time for regeneration. Gray-code encoding can be used to improve metastability (A Gray-code is an encoding of numbers so that adjacent numbers have a single
digit differing by 1). Gray-code encoding allows only one bit in the output to change at a time. The comparator outputs are first converted to gray-code encoding and then later decoded to binary.

Another problem occurs when a metastable output drives two distinct circuits. It is possible for one circuit to declare the input a "1" while assumes it's a "0". This can create major errors. To avoid this, solution is only one circuit should sense a potentially metastable output.

- **Sparkle Codes**

Generally, output of the comparator is thermometer code (Unary coding, or the unary numeral system and also sometimes called thermometer code), such as 00111111. Errors may cause an output like 0011011. The spurious "0" in the result sequence is called a sparkle. The sparkles can be due to imperfect input settling or comparator timing mismatch. The magnitude of the error can be quite large and can be avoided by employing an input track-and-hold in front of the ADC along with an encoding technique that suppresses sparkle codes.

- **Clock Jitter**

Jitter in sampling rates decrease Signal to Noise ratio (SNR) in Analog to Digital Converter. This becomes noticeable for high analog input frequencies. To achieve accurate results, it is critical to provide the ADC with a low-jitter, sampling clock source.

- **Input Signal-Frequency Dependence**

When the input signal changes before all the comparators have completed their tasks, the ADC's performance is adversely impacted. The most serious impact is a drop-off in signal-to-noise ratio (SNR) plus distortion (SINAD) as the frequency of the analog input frequency increases. Measuring spurious-free dynamic range (SFDR) is another good way to observe converter performance. The "effective bits" achieved by the ADC is a function of input frequency; it can be improved by adding a track-and-hold (T/H) circuit in front of the ADC. The T/H circuit allows dramatic improvement, especially when input frequencies approach the Nyquist frequency, as shown in Figure 2. Parts without T/H show a significant drop-off in SFDR.

(Figure 2) - Spurious – free dynamic range as a function of input frequency.
3.2 Pipelined ADC

The pipelined analog-to-digital converter that recently became the most used and known ADC architecture for sampling rates of few mega samples per second (Msps) up to 100Msps. Compared to the two-step flash ADC which has just 2 stages, pipelined ADC’s have multiple cascades stages. Pipeline ADC uses two or more steps of sub ranging. First, a coarse conversion is done. For the second step, the difference to the input signal is determined with a digital to analog converter (DAC). This difference is then fine-tuned, and the results are combined in a last step. This can be considered a refinement of the successive-approximation ADC wherein the feedback reference signal consists of the interim conversion of a whole range of bits rather than just the next-most-significant bit.

(Figure 3)- Block diagram of Pipelined ADC

A pipeline ADC computes input voltage in a number of successive stages(cascading). The pipelined ADC architecture is implemented using at least two or more low resolution flash ADCs as shown in Figure 3. Each stage has a S/H circuit to hold the amplified residue from the previous stage. Then, the input is fed to the low resolution flash ADC to generate a segmented binary output. Like the sub-ranging ADC, the segmented output is changed to an analog signal and is subtracted from the input. This remnant is amplified in an amplified to send to the next stage. The segmented binary outputs from each stage are time-aligned with a shift register. The final binary output is obtained after passing through digital error correction logic.

(Figure 4)- Pipeline ADC Transfer Curve
3.2.1 Design Considerations and Implications

In Pipelined architecture it is highly likely to achieve higher resolutions than flash converters containing a similar number of comparators. All this is done with a drawback of increasing the total conversion time from one cycle to \( n \) cycles. But since each stage samples and holds its input, \( n \) conversions can be carried out at a time simultaneously. The total throughput can therefore be equal to the throughput of a flash converter, i.e. one conversion per cycle. The contrast is that for the pipelined converter, latency equal to \( n \) cycles is introduced. The power consumption in Pipelined ADC is higher than that of flash converter. Another drawback of the pipelined architecture is that the conversion process generally requires a clock with a fixed period. Rapid conversion of varying non-periodic signals on a traditional pipelined converter can be difficult because the pipeline typically runs at a set periodic rate.

3.2.2 Error Sources in Pipelined ADC

- **Overlapping**
  
  The following condition should be met to correct for overlapping errors:
  
  \[
  N \times R + K > M
  \]

  where \( N \) is the number of stages, \( R \) is the coarse resolution of subsequent stages in the ADC circuit, \( K \) is the fine resolution of the final ADC stage, and \( M \) is the pipeline ADC's overall resolution. Pipeline ADCs include digital error-correction circuitry which operates in between each stages. Some pipeline quantizers have a calibration unit that compensates for unwanted side effects such as capacitor mismatch or temperature drift in the multiplying DAC.

- **Other Difficulties in Pipeline ADC**
  
  Pipeline latency, caused by the number of stages through which the input signal must pass. Sensitivity to process imperfections that cause nonlinearities in gain, offset, and other parameters. Complex reference circuitry and biasing schemes. Critical latch timing, needed for synchronization of all outputs. Greater sensitivity to board layout, compared with other architectures.

(Figure 5) - Stage Operations Mode in Pipeline ADC
3.3 Successive Approximation ADC

A simple way of addressing the digital ramp ADC’s shortcomings is the so-called successive approximation ADC. Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are frequently the architecture of choice for medium-to-high-resolution applications with sample rates under 5 megasamples per second (MSPs). The key point in this design is a very special counter circuit known as successive approximation register. Resolution for SAR ADCs most commonly ranges from 8 to 16 bits, and they provide low power consumption as well as a small form factor. This combination of features makes these ADCs ideal for a wide variety of applications, such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition.

Successive Approximation Register ADC is a proper choice for low power applications. SAR ADC operates on a successive approximation algorithm to convert analog input to a digital code successively. On basic terms it can be said that, one bit is determined in each clock cycle by using a binary search algorithm. In this arrangement track/hold circuit is used to hold the analog input voltage ($V_{IN}$). The binary search algorithm is implemented by N-bits register. The block diagram is shown in Figure 7.

Initially the value of register is set to mid scale i.e. MSB set to “1” and all the other bits are set to “0”. The output of DAC ($V_{DAC}$) becomes half the reference voltage $V_{REF}/2$, where $V_{REF}$ is the reference voltage of ADC. The comparator will compare the input voltage $V_{IN}$ with $V_{DAC}$. If $V_{IN}$ is larger than $V_{DAC}$, the comparator output will be set to “1”, and the MSB of the N-bit register remains at ‘1’. If the input voltage $V_{IN}$ is less than $V_{DAC}$ then the comparator output becomes “0”. The SAR control logic will alter the MSB of the register to ‘0’, set the next bit to “1” and perform comparison again. The operation of 4-bit SAR ADC is shown in figure.
This process continues till LSB and once this process is completed the N-bit digital word is available in the register.

![Diagram of 4-bit SAR ADC operation]

(Figure 8) - A 4-bit SAR ADC operation

3.3.1 Design Considerations and Implications
A SAR converter using a single comparator is possible to apprehend a high-resolution ADC. To achieve M-bit resolution, M comparison cycles are required when compared to p cycles for a pipelined converter and 1 cycle for a flash converter. Since a successive-approximations converter uses a fairly simple architecture employing a single SAR, comparator, and DAC, and the conversion is not complete until all weights have been tested, only one conversion is processed during M comparison cycles. For this reason, SAR converters are more often used in higher resolution and lower speed applications. This feature makes the SAR architecture ideal for converting a series of time-independent signals. For a resolution of M bits, the successive approximation architecture is at least M times slower than the full-flash configurations, but it offers several advantages. The comparator offset voltage does not affect the overall linearity of the converter because it can be represented as a voltage source in series with Sample and hold output, indicating that offset voltage simply adds to analog input and hence appears as an offset in the overall characteristics. Consequently, the comparator can be designed for high speed operation in high resolution systems. This architecture does not require an explicit subtractor which is an important advantage for high resolution applications. The circuit complexity and power dissipation are in general less than that of the other architectures.

3.3.2 Error Sources in Successive Approximation ADC
The different sources of error and drawbacks are: The serial nature of SAR architecture limits its speed. The settling time of the DAC, has to settle within the resolution of the overall converter, for example, ½ LSB. Comparator noise causes performance degradation of the ADC because of the lack of gain in the ADC architecture. One can put a preamplifier before the comparator to reduce this noise, but at the expense of burning more power in the preamplifier.
3.4 Sigma Delta ADC

The Σ–Δ ADC is a staple in today’s signal acquisition and processing system designs. An SD-ADC has a modulator and a digital filter (also known as decimation filter). A modulator converts the input analog signal into digital bit streams (1s and 0s). One can observe a bit, either 1'b1 or 1'b0 coming at every clock edge of the modulator. The decimation filter receives the input bit streams and, depending on the over sampling ratio (OSR) value, it gives one N-bit digital output per OSR clock edge. For example, if we consider OSR to be 64, then the Filter gives one N-bit output for every 64 clock edges (64 data outputs of the modulator)

Here N is the resolution of the SD ADC.

The sigma-delta architecture takes a rudimentarily different approach from the other architectures. Sigma-delta converters offer high integration, high resolution, and low cost, making them a good ADC choice for different applications such as weighing scales and process control. Sigma-delta (Σ–Δ) converters have comparatively simple structures. Block diagram of a Sigma Delta ADC It consists of two main blocks. One is the Sigma-delta modulator that includes an integrator, a comparator, and a single-bit DAC. The other is a digital filter that changes the Sigma-delta output to binary code with filtering. The output of the 1-bit DAC is subtracted from the input signal, integrated, and then converted to a 1-bit binary output. This single bit again goes to the DAC to be processed. This closed-loop process is performed at a very high oversampled rate.
3.4.1 Design Considerations and Implications

• Noise Shaping
The main advantageous keynote feature of sigma-delta architecture is the capability of its noise shaping, a phenomenon by which most of the low frequency noise is effectively raised up to higher frequencies and out of the band of interest. As a result, the sigma-delta architecture has been very popular for designing low-bandwidth high resolution ADCs for precision measurement.

• Oversampling
Delta-sigma ADCs use sample rates that are of large multiples, for instance, 128 times the sample rate sufficient for a given signal. For example, to sample a 25 kHz signal, a sample rate greater than the Nyquist rate (that is, > 50 KHz) would be adequate. However, a delta-sigma ADC using an oversample factor of 128 samples the signal at 6 MHz. This approach has several benefits, such as better antialiasing and higher resolution. In the frequency domain, sampling a signal effectively modulates the input signal spectrum with carrier frequencies that are multiples of the sample rate Fs (that is, 0, Fs, 2Fs, 3 Fs, and so on). To recover the signal the sampling rate require must be greater than the Nyquist rate (Fs > 2Fmax). The oversampling property of sigma delta ADC will provide better antialiasing as shown in Figure.

3.4.2 Error Sources in Sigma Delta ADC
A Major limitation of Sigma delta architecture is its latency, which is substantially greater than all other types of architecture. Because of this latency issues, oversampling sigma-delta converters are not often used in multiplexed signal applications. To avoid the interference between multiplexed signals, a delay of at least equal to the decimator's total delay must occur between conversions. These characteristics can be improved in more complex and seasoned sigma-delta ADC designs by using multiple integrator stages and/or multi-bit DACs.
4. Architectural Trade-offs

(Figure 12)- Architectural trade-offs

5. Comparison of different types of ADC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Flash</th>
<th>Pipeline</th>
<th>Successive Approximation</th>
<th>Sigma-Delta</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion methods</td>
<td>For N bits ADC $2^N - 1$ comparators are required, meaning a increase in factor by 2 for each bit.</td>
<td>Small parallel structure, each stage work on few bits.</td>
<td>Binary search algorithm, internal circuitry runs at a high speed.</td>
<td>Comparator senses the difference and the integrator sums the comparator’s output with analog input signal, oversampling ADC rejection programmable data output.</td>
</tr>
<tr>
<td>Encoding methods</td>
<td>Thermometer code encoding</td>
<td>Digital Correction Logic</td>
<td>Successive Approximation</td>
<td>Over-sampling Modulator, Digital Decimation Filter</td>
</tr>
<tr>
<td>Conversion Time</td>
<td>Conversion time does not change with increase in resolution.</td>
<td>Increases linearly with increase in resolution.</td>
<td>Increases linearly with increase in resolution.</td>
<td>Trade-off between data output rate and noise free resolution.</td>
</tr>
<tr>
<td>Size</td>
<td>$2^N - 1$ comparators, die</td>
<td>Die, increases</td>
<td>Die, increases</td>
<td>Core die size will not</td>
</tr>
<tr>
<td></td>
<td>Size and power increases exponentially with resolution.</td>
<td>Linearly with increase in resolution.</td>
<td>Linearly with increase in resolution.</td>
<td>Substantially change with increase in resolution.</td>
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</tr>
<tr>
<td>Resolution</td>
<td>Component matching typically limits resolution to 8-bits.</td>
<td>Component matching requirements double with every bit increase in resolution.</td>
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</tr>
<tr>
<td>Selection of this architecture</td>
<td>Ultra-High Speed when power consumption not primary concern</td>
<td>High speeds, few Msps to 100+ Msps, 8 bits to 16 bits resolution, lower power consumption than flash</td>
<td>Medium to high resolution (8 to 16-bit), low power consumption, small size</td>
<td>High resolution, low to medium speed, no precision external components, digital filter reduces anti-aliasing requirements</td>
</tr>
<tr>
<td>Disadvantages</td>
<td>Sparkle codes / metastability, high power consumption, large size, expensive.</td>
<td>Parallelism increases throughput at the expense of power and latency</td>
<td>Speed limited to ~5 Msps. May require anti-aliasing filter</td>
<td>Higher order (4th order or higher) - multibit ADC and multibit feedback DAC</td>
</tr>
</tbody>
</table>

5. Conclusion

Generally, a typical ideal ADC has a great many bits for very fine resolution, it can also sample at lightning-fast speeds, and recover from steps instantly. It is unfortunate that it doesn’t exist in the real world. It is obvious that, any of these attributes may be improved upon by additional circuit complexity, either in terms of increased component count and/or special circuit designs specifically made to run at higher clock speeds. Many different ADC technologies, though, have their own pro’s and con’s. In this paper various types of ADCs like Flash ADC, Pipeline ADC, Successive approximation ADC and sigma delta ADC have been discussed with their architectures and working principal. The design constraints and sources of errors for all architectures have been highlighted to draw a fair comparison of all architectures. At last comparison between all ADC architecture by considering different parameter is also presented.

References

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