EFFICIENT MODULAR ADDERS BASED ON REVERSIBLE CIRCUITS

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ABSTRACT

Reversible logic is a computing paradigm that has attracted significant attention in recent years due to its properties that lead to ultra-low power and reliable circuits. Reversible circuits are fundamental, for example, for quantum computing. Since addition is a fundamental operation, designing efficient adders is a cornerstone in the research of reversible circuits. Residue Number Systems (RNS) has been as a powerful tool to provide parallel and fault-tolerant implementations of computations where additions and multiplications are dominant. For the first time in the literature, the combination of RNS and reversible logic is used. The parallelism of RNS is leveraged to increase the performance of reversible computational circuits. Being the most fundamental part in any RNS, the implementation of different adders, namely ripple carry adder, carry save adder, carry look ahead adder, Kogge stone adder and Han Carlson Adder, using reversible logic. Analysis and comparison with different adders for modular addition are designed using reversible gates with minimum overhead in comparison to regular Brunt Kung modulo-adders.

1. INTRODUCTION

Researchers in academia and industry believe that Moore's law is ending, and even newly delivered deep-sub micron transistors are not significantly more efficient than their previous generations. Therefore, new computing paradigms should be investigated in order to overcome the predicted performance wall which will be reached in 2020.

1.1 Reversibility

There are two major, closely related types of reversibility that are of particular interest for this purpose: physical reversibility and logical reversibility. A process is said to be physically reversible if it results in no increase in physical entropy; it is isentropic. There is a style of circuit design ideally exhibiting this property that is referred to as charge recovery logic, adiabatic circuits, or adiabatic computing.

1.1.1 Physical reversibility

Landauer's principle (and indeed, the second law of thermodynamics itself) can also be understood to be a direct logical consequence of the underlying reversibility of physics, as is reflected in the general Hamiltonian formulation of mechanics, and in the unitary time-evolution operator of quantum mechanics more specifically.

1.1.2 Logical reversibility

To implement reversible computation, estimate its cost, and to judge its limits, it can be formalized in terms of gate-level circuits. A simplified model of such circuits is one in which inputs are consumed (however, note that real logic gates as implemented e.g. in CMOS do not do this). In this modeling framework, an inverter (logic gate) (NOT) gate is reversible because it can be undone.

2. EXISTING SYSTEM

2.1 Residue Number System

A residue numeral system (RNS) is a numeral system representing integers by their values modulo several pair-wise co-prime integers called the moduli. This representation is allowed by the Chinese remainder theorem, which asserts that, if N is the product of the moduli, there is, in an interval of length N, exactly one integer having any given set of modular values.A residue numeral system is defined by a set of k integers, called the moduli, which are generally supposed to be pairwise coprime (that is, any two of them have a greatest common divisor equal to one), referred to as the moduli.

2.2 BLOCK DIAGRAM OF EXISTING SYSTEM

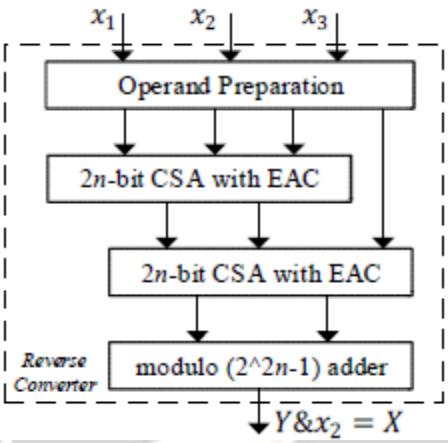

Fig -1 The full reverse converter for the moduli set {2n-1, 2n+k, 2n+1}

A full hardware design of RNS with moduli set {2n-1, 2n+k, 2n+1} is reported, and herein forward and reverse converters for this moduli set are depicted in Figure 3.1 and 3.2, respectively. It can be observed that CSAs and carry-propagate modulo 2n-1 adders are the components required to implement a full RNS architecture, since arithmetic in a channel also requires modulo adders and multipliers. Thus, to have an efficient modular adder is fundamental for RNS-based application

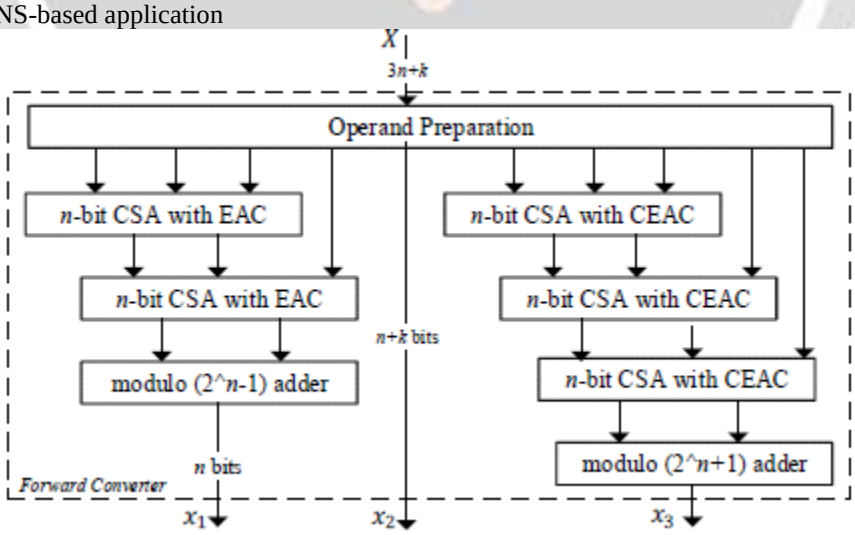

Fig -2 The forward converter for the moduli set {2n-1, 2n+k, 2n+1}

2.2.1 Modular addition using universal gates

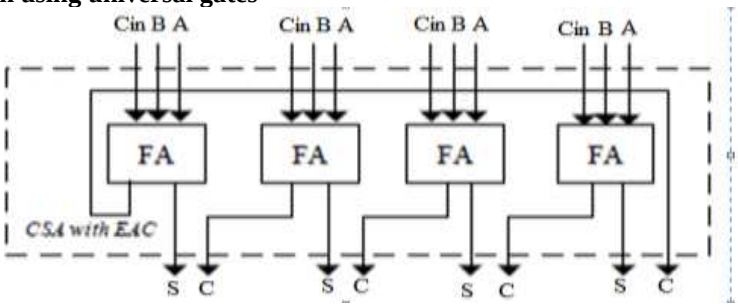

Fig -3 CSA with EAC structure

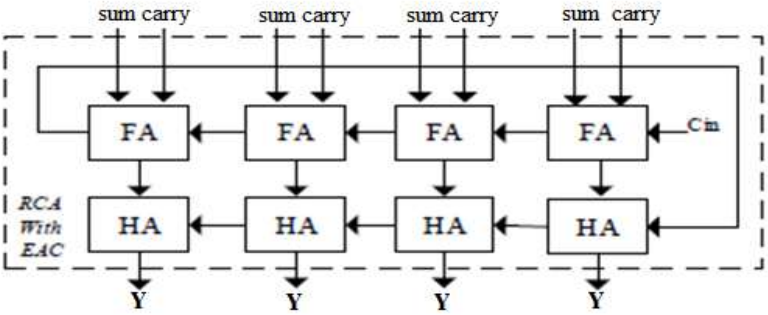

Fig -4 Modulo 2n-1 adder based on ripple-carry method

The CSA with EAC consists of independent full adders (FAs) which just combine the three inputs into two carry-save output vectors, as shown in Figure. 3.3. Its delay is just the delay of a single FA, while the overall area linearly depends on the width of the operands. End-around carry is complemented.

3 PROPOSED SYSTEM

3.3.1 Reversible circuit

Reversibility in computing implies that no information about the computational states can ever be lost, it can be recovering any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility.

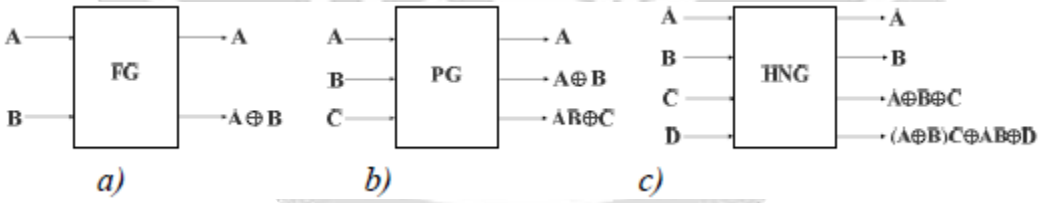

Fig -4 The reversible gates: a) Feynman; b) Peres and c) HNG

3.3.2 Modular adders using reversible circuits

The CSA is a 3-to-2 compression unit that is very popular for regular arithmetic as well as in RNS architectures due to its speed and cost.

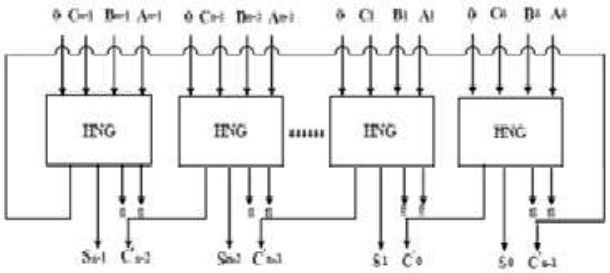

Fig -5 HNG Structure

Similar to CSA, FAs can be realized with HNG gates. Besides, the Peres reversible gate can be used to implement a HA, where the third input bit is set to zero, as shown in Figure.3.7.

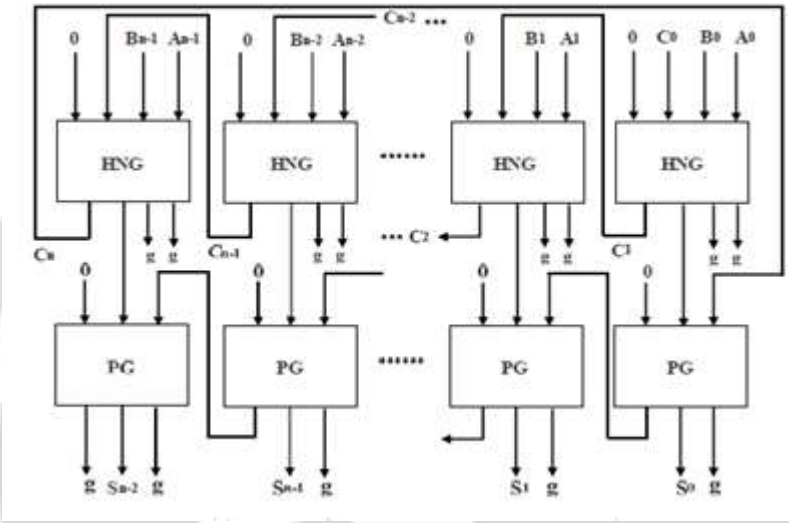

Fig -6 CSA structure using reversible gates

The regular Brent-Kung adder into a modulo 2n-1 adder, by inserting a row of black cells to add the carry-out, i.e. the end-around carry's as shown in Figure. 3.9.

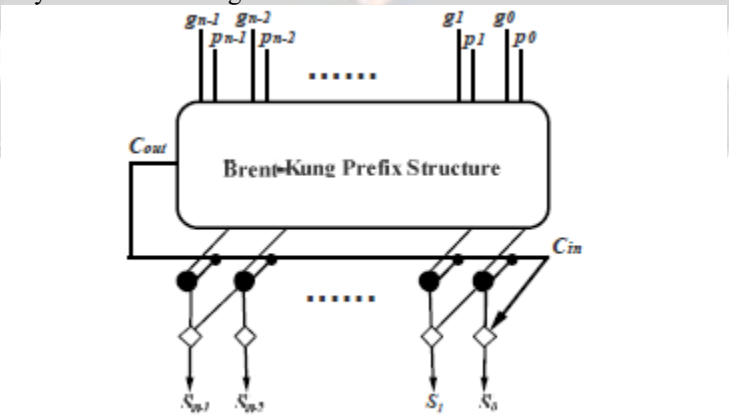

Fig -7 The modulo 2n-1 Brent-Kung prefix adder architecture

4. RESULTS AND IMPLEMENTATION

4.1 Modular Adders Using Universal Gates

4.1.1 Simulation results:

The simulation output of the modulo adders using universal gates is shown below:

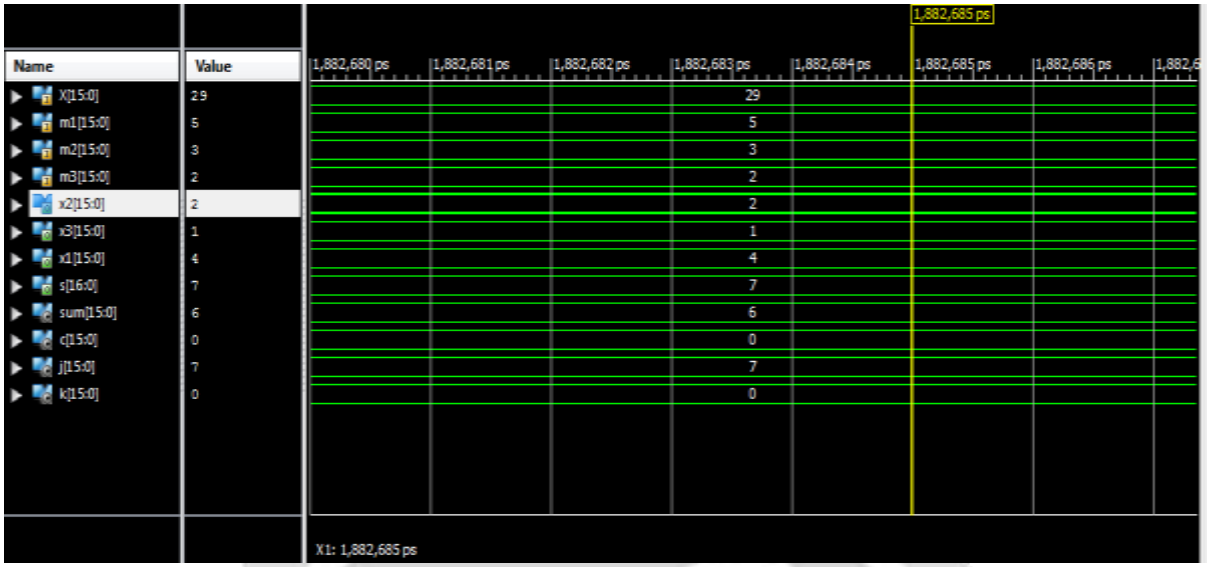

Fig -8 Simulation output for modulo adders using universal gates

4.1.2 Implementation of reversible gates:

The simulation output of the reversible gates is shown in figure 5.6

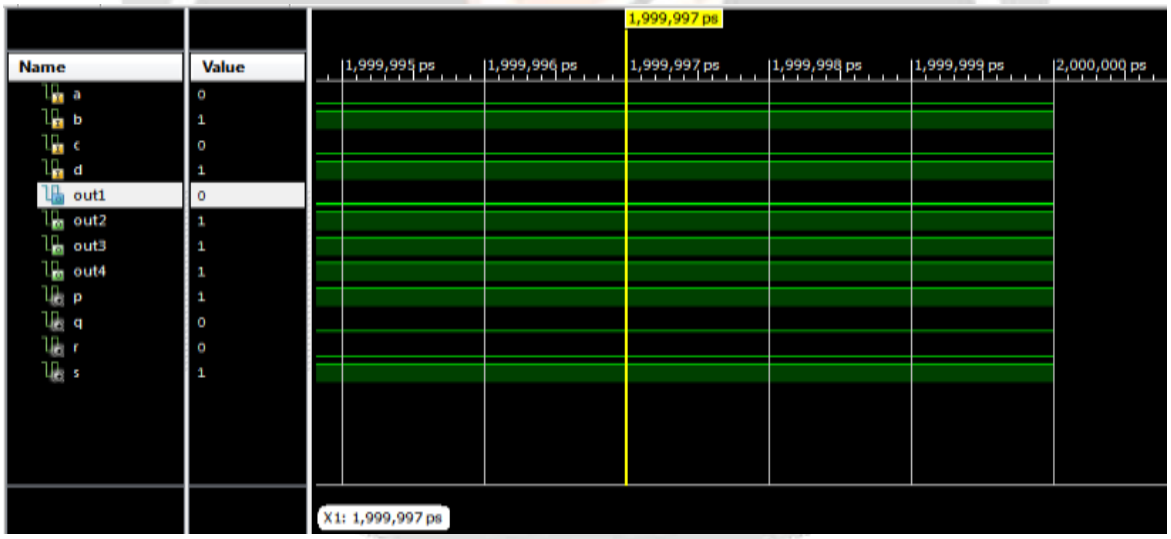

Fig -9 Simulation output for modulo adders using universal gates

4.1.3 Implementation of peres gate:

The simulation output of the peres gates are shown in figure 5.7

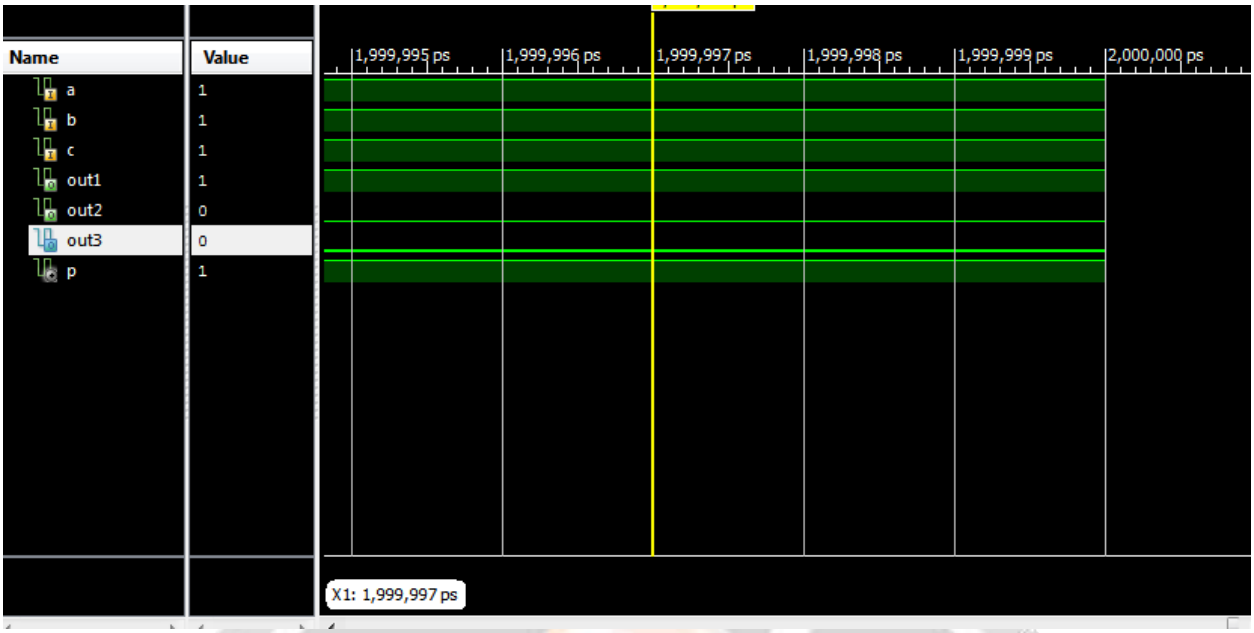

Fig -10 Simulation output for modulo adders using peres gates

4.1.4 Modular adders using reversible gates:

The simulation output of the modulo adders using reversible gates is shown in figure 5.8

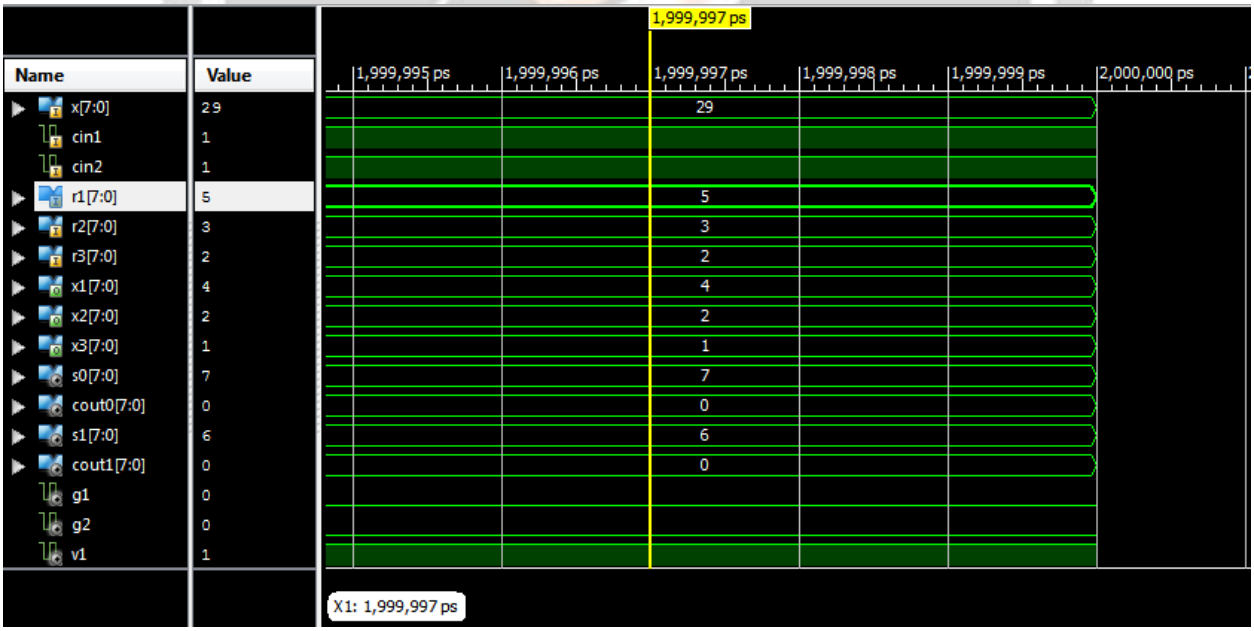

Fig -11 Simulation output for modulo adders using reversible gates

4. CONCLUSION

From the result and analysis, we conclude that modulo addition using reversible gates consume low power than the universal gates and timing delay also gets reduced by using reversible gates. Thus future's VLSI deals with reversible gates.

Table -1 Performance of universal and reversible gates

DESCRIPTION	AREA ANALYSIS	TIMING REPORT	POWER ANALYSIS
UNIVERSAL GATES-MODULO ADDER	59 LUT's	12.596ns	328.27mW
REVERSIBLE GATES-MODULO ADDER	245 LUT's	12.47ns	144.06mw