FAST EFFICIENT VOLTAGE LEVEL SHIFTER FOR DUAL SUPPLY APPLICATIONS

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ABSTRACT

This brief presents a fast and power-efficient voltage level shifting circuit capable of converting extremely low levels of input voltages into high output voltage levels. The efficiency of the proposed circuit is due to the fact that not only the strength of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit. Post layout simulation results of the proposed circuit in a 0.18-µm technology demonstrate a total energy per transition of 157 fJ, a static power dissipation of 0.3 nW, and a propagation delay of 30 ns for input frequency of 1 MHz, low supply voltage level of VDDL=0.4V, and high supply voltage level of VDDH=1.8V.

Keyword—*Level converter, propagation delay, subthreshold operation, voltage level shifter*.

1.INTRODUCTION

One of the most effective ways to reduce dynamic and short-circuit power consumption of digital circuits is lowering the value of the power supply voltage. On the other hand, reducing the supply voltage increases the propagation delay of the circuits. Moreover, less headroom in analog circuits decreases signal swings and therefore increases the sensitivity to noise. Hence, in moderate-speed mixed-signal circuits or in digital circuits where different parts operate at different speeds, dual-supply architectures are introduced in which a low voltage is supplied for the blocks on the noncritical paths while a high supply voltage is applied to the analog and the high-speed digital blocks. In a system with dual supply voltages, level-shifting circuits are needed to convert the lower logic levels into the higher ones to provide correct voltage levels for the next digital blocks. In order to alleviate the degradation of the overall performance of the circuit, the required level shifters must be designed with minimum propagation delay, power consumption, and silicon area. In addition, in order to have more power saving in the low-supply blocks, the employed level shifters must be able to convert the extremely low values of VDDL to even lower than the threshold voltage of the input transistors. Hence, in this brief, a fast and power-efficient voltage level shifter is proposed, which is able to convert extremely low values of the input voltages.

Circuit designers are faced with the challenge of developing systems with increasing functionality and complexity while under demanding power and time-to-market constraints. Such systems often require voltage level translation devices to allow interfacing between integrated circuit devices built from different process technologies. Thus voltage level shifters play an important role in widely used VLSI systems.

2.EXISTING SYSTEM

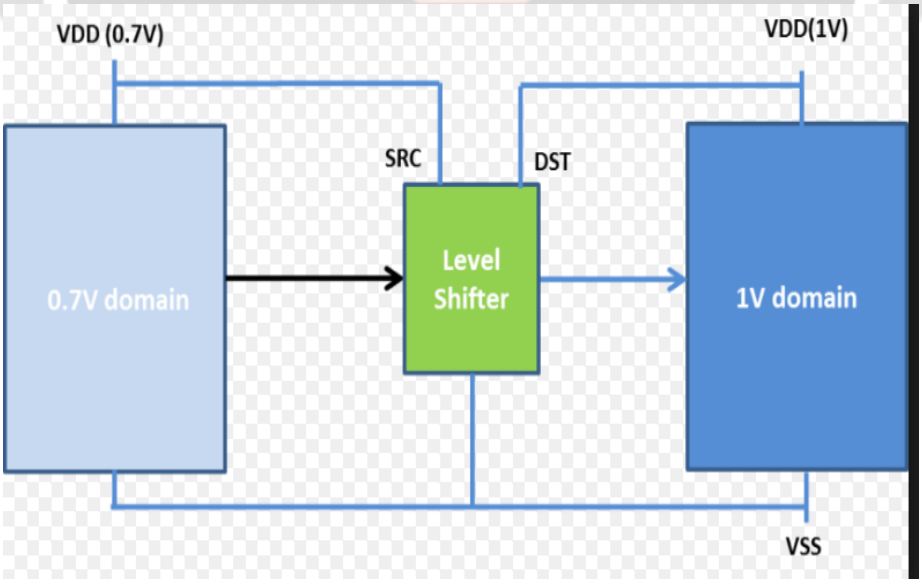
One of the most effective ways to reduce dynamic and short-circuit power consumption of digital circuits is lowering the value of the power supply voltage. On the other hand, reducing the supply voltage increases the propagation delay of the circuits. Moreover, less headroom in analog circuits decreases signal swings and therefore increases the sensitivity to noise.

When the voltage difference between VDDL and VDDH is high and particularly when the input voltage is in subthreshold range, this circuit will no longer be able to convert the voltage levels. This is because the currents of the pull-down transistors are smaller than those of the pull-up devices.

3.PROPOSED SYSTEM

Dual-supply architectures are introduced in which a low voltage is supplied for the blocks on the non critical paths while a high supply voltage is applied to the analog and the high-speed digital blocks. In a system with dual supply voltages, level-shifting circuits are needed to convert the lower logic levels into the higher ones to provide correct voltage levels for the next digital blocks. In order to alleviate the degradation of the overall performance of the circuit, the required level shifters must be designed with minimum propagation delay, power consumption, and silicon area In addition, in order to have more power saving in the low-supply blocks, the employed level shifters must be able to convert the extremely low values of VDDL to even lower than the threshold voltage of the input transistors. Hence, in this brief, a fast and power-efficient voltage level shifter is proposed, which is able to convert extremely low values of the input voltages.

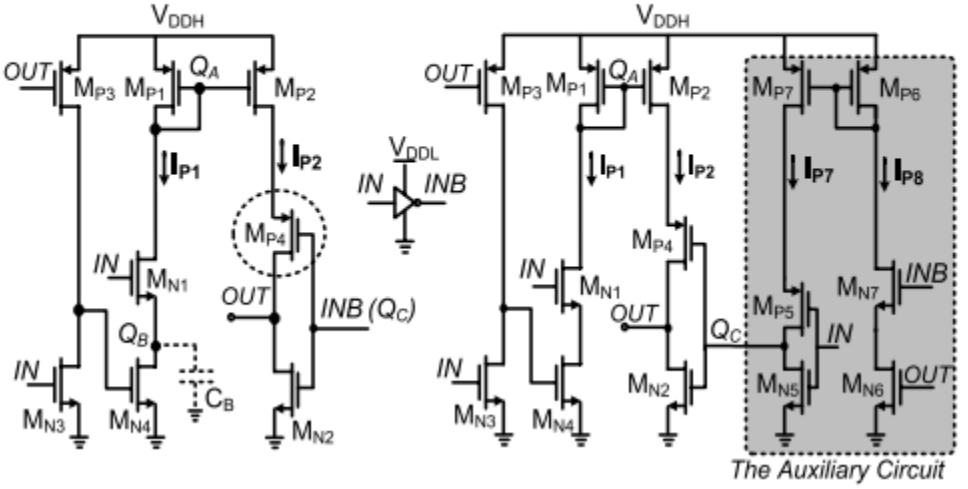
4.1.BLOCK DIAGRAM



Figure(1) – Block Diagram

4.2.PROPOSED SYSTEM BLOCK DIAGRAM

Transistor	M_{N1},M_{N3},M_{N4},M_{N6}, M_{N7},M_{P3},M_{P4},M_{P5},M_{P6}	M_{N5},M_{P7}	M_{P1}	M_{N2},M_{P2}
W/L	0.4μm/0.18μm	2μm/0.18μm	0.4μm/5μm	1μm/0.18μm

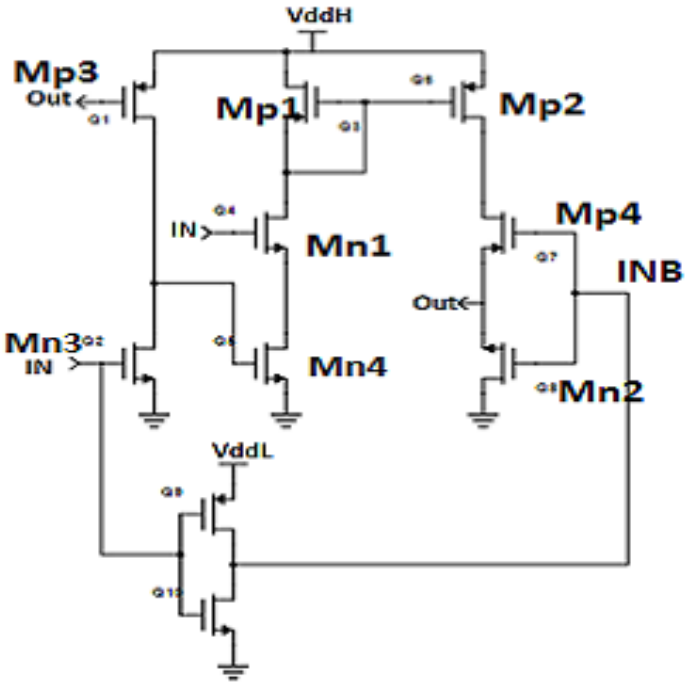


Figure(2a) - ***Principle of the Proposed level shifter.***

Figure(2b) - ***Schematic of proposed level shifter***

.5.EXISTING LEVEL SHIFTER IMPLEMENTATION

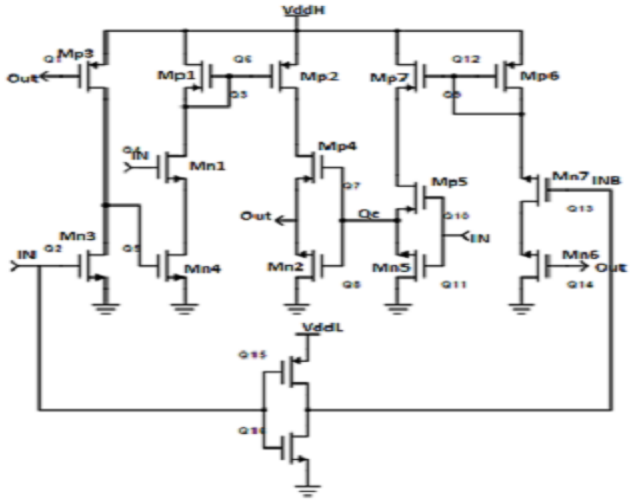
In this section, circuit configuration and advantages of two level converters recently reported will be briefly explained.. When the input signal becomes high transistor Mn1turns on and nmos transistor Mn4 turns on because the overdrive voltage of Mp3 larger than the Mn3. Therefore transition current flows Mp1, Mn1, and Mn4 and this current is mirrored to Mp2 and tries to pull up the output node. Finally the output is pulled up and the transistor Mp3 turned off consequently nmos transistor Mn4 pull down by the nmos transistor Mn3, means no static current flows through Mp1, Mn1, and Mn4. If the input is low and INB is high, the nmos transistor Mn2 conducts and pulls down the output node at the same time nmos transistor Mn1 off and no static current flows. This means that current of Mp2 is not completely close to zero weak contention exist. Further reduce the value of current another device Mp4 is used



Figure(3) – Existing level shifter implementation

6.EXTENSION OF LEVEL SHIFTER WITH AUXILIARY CIRCUIT

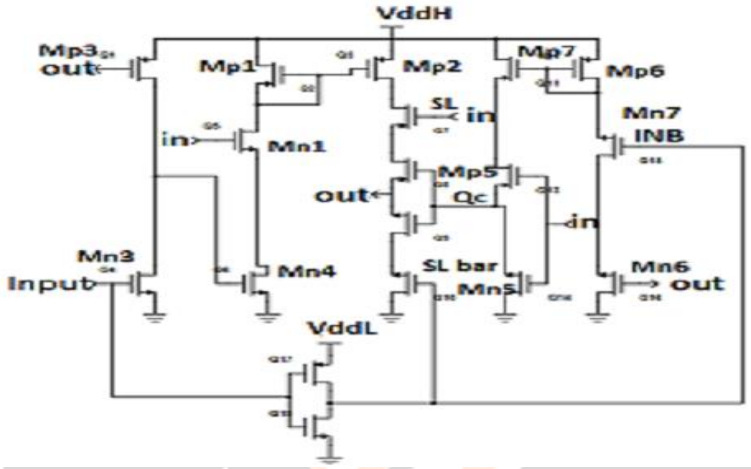
In order to further reduction of power and delay as an extension of voltage level shifter with auxiliary circuit is used, shown in Fig.2. Auxiliary circuit turns only high to low transition of input signal and to pull up the node Qc to a value larger than VddL. Transistor Mn6, Mn7 and Mp6 are turned on and nmos transistor Mn5 turned off, therefore transition current flows through Mn6, Mn7, Mp6 are mirrors to Mp7 and pull up the node QC.The strength of pull-up devices is significantly reduced when the pull down device is pulling down the output node, but the strength of pull down device is also increased using a low power auxiliary circuit



Figure(4) – Extension of level shifter with auxiliary circuit

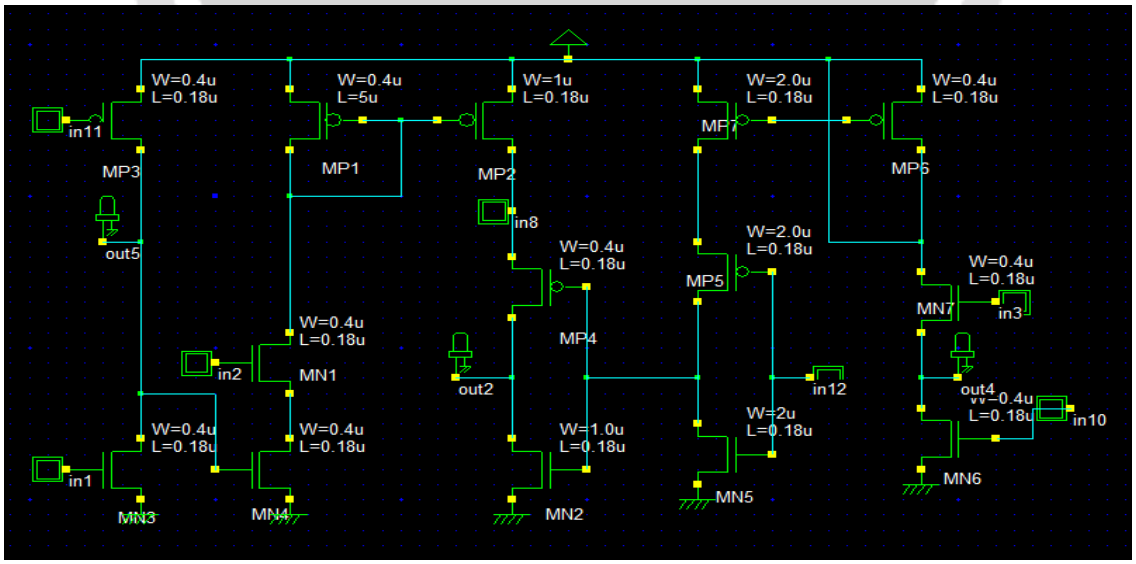
7.PROPOSED VOLTAGE LEVEL SHIFTER CIRCUIT

A new power optimized proposed voltage level shifter is introduced. Here the power gating technology is implemented for power optimization. Power gating is the circuit design technique that has been most widely used in industrial products, means connecting sleep transistor to combination of pull up pull down network to reduce the subthreshold leakage current. A sleep transistor is separating the pull up network from Vdd and pull down network from Vss.Sleep transistor SL separates transistor Mp4 from Vdd and SL bar separates nmos transistor Mn5 from Vss. During active mode SL=0, sleep transistor turns on and provide low resistance in the conduction path. Circuit cut off from its power supply in sleep mode SL=1 by means of current switch path.



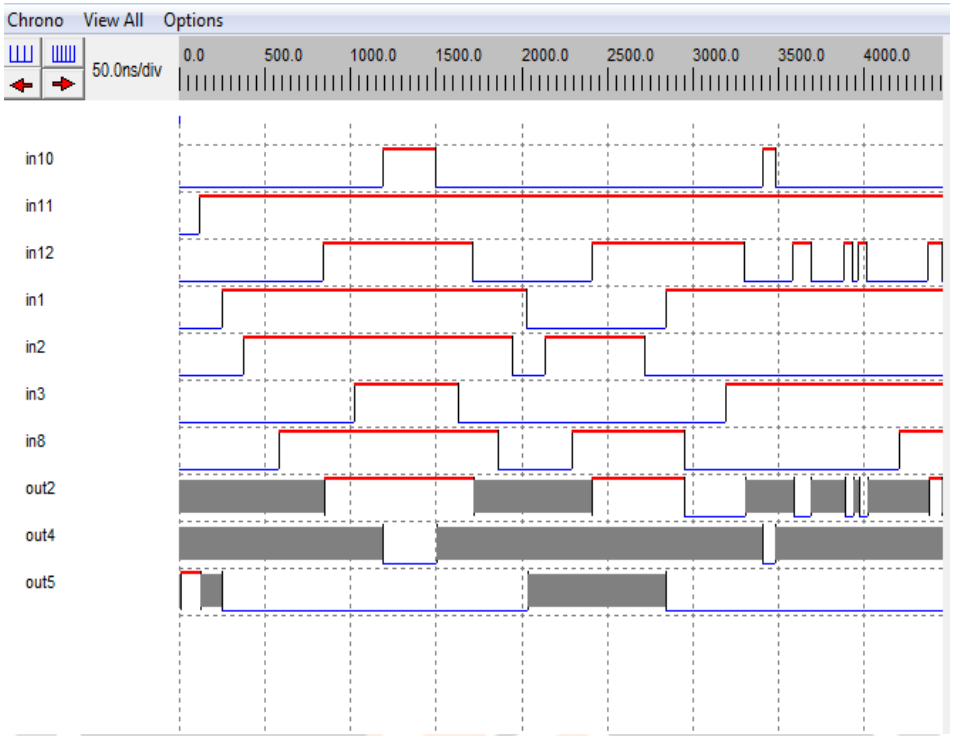
Figure(5) – Proposed voltage level shifter circuit

8.1.DESIGN OF PROPOSED LEVEL SHIFTER



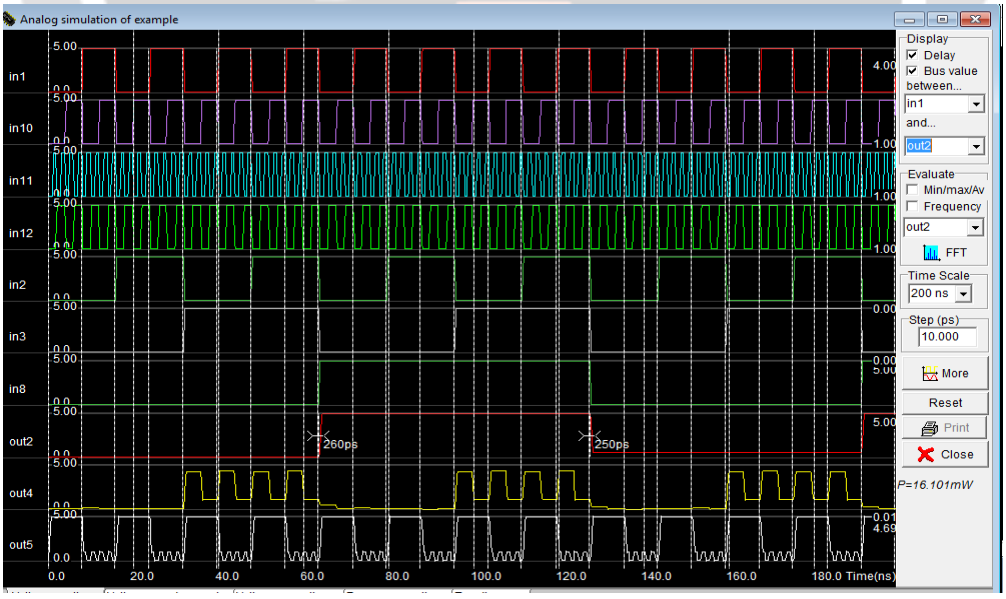
Figure(6) – Design of proposed level shifter

8.2.OUTPUT OF PROPOSED LEVEL SHIFTER



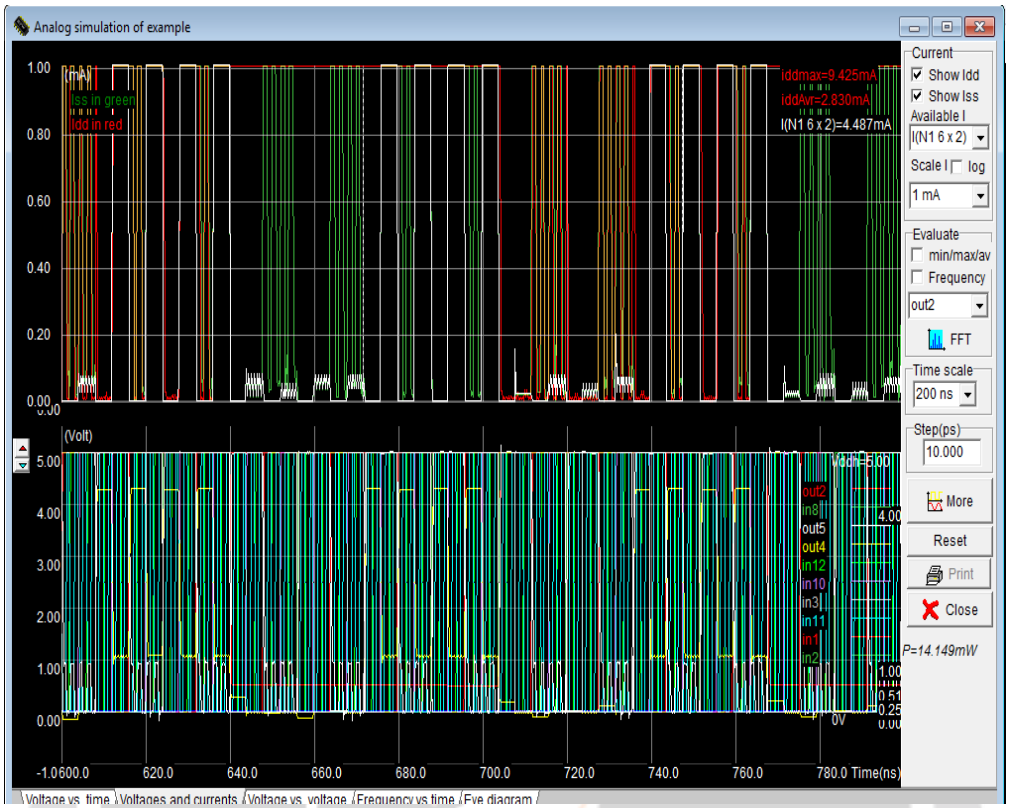
Figure(7) – Output of proposed level shifter

9.1.OUTPUT OF VOLTAGE VERSUS VOLTAGE



Figure(8) –Output of voltage versus voltage

9.2.OUTPUT OF VOLTAGE VERSUS CURRENT



Figure(9) – Output of voltage versus current

10.SIMULATION RESULTS OF THE PROPOSED CIRCUIT

Frequency	$V_{DDL,min}$ (V)	Power (μW)	Delay (ns)
5 MHz	0.38	0.98	45
10 MHz	0.41	1.68	24.3
20 MHz	0.44	2.77	13.65
50 MHz	0.49	5.72	5.81
100 MHz	0.54	10.2	2.86
200 MHz	0.6	17.66	1.46
500 MHz	0.72	44	0.63
1 GHz	0.9	95	0.34

Table(1) – Simulation results of the proposed circuit

11.ADVANTAGES

- *High speed.*
- *No contention.*
- *Power consumption is reduced.*
- *Reduces area ,propagation delay and noise.*

12.APPLICATIONS

- *Shift a signal voltage range from one voltage domain to another.*
- *Widely used in modern system –on-chips to tradeoff energy and speed.*

13.CONCLUSION

In this brief, a fast and low-power voltage level-shifting architecture was proposed which is able to convert extremely low-input voltages. The efficiency of the proposed circuit is due to the fact that not

only the current of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased. Post layout simulation results verifies the efficiency of the proposed circuit compared with other works, especially from power consumption viewpoint.

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