FPGA BASED DIGITAL DOOR LOCK SYSTEM

Rachita Dahake
PG student
Department of Electronics Engineering
Priyadarshini College of Engineering

Dr. Mrs. A.P Khandait
Assistant Professor
Department of VLSI
Priyadarshini College of Engineering

Abstract

Security is a major issue everywhere today. Everyone wants a home, a factory,a bank, and so on. Housing security is becoming more and more important as access to services increases day by day. Here in this paper, we try to present the research done on various methods of locking doors that have been used in homes, offices, shops, factories etc. This study will also shed light on the pros andcons of various door lock systems. and technologies used in various systems. The study will include the traditional door lock system, RFID-based system, touch-based systems, Bluetooth and GSM based technology and various other technologies used in secure door locksystems. Technological advancement in each passing day can help us to meet various technologies that can be applied to a door lock system. Since safety is a major concern for most people right now, we feel that research conducted on a variety of topics related to the topic canhelp people choose the best technology for their upcoming projects or make changes to past projects and use a successful department. locking systems for their needs.

INTRODUCTION

FPGA based Digital Door Lock System is based on Altera's Cyclone-ii FPGA. This system allows user/owner to lock/unlock door by simply entering pre-defined alphanumeric password with the help of 4x4 alphanumeric matrix keypad. This system is battery powered and can be usedanywhere portably.

With the help of multi colour LEDs and buzzer system is more interact --table with user/owner. On every key press of keypad FPGA signals buzzer and signal LED in order to indicate to user that the key is successfully pressed/entered. For more interaction few LEDs were used which indicates various things such as system heartbeat signal, lock/unlock status, mode of operation, etc.
For locking/unlocking of the door, an electromagnetic solenoid lock is used which locks and unlocks the door electrically on receiving signal from FPGA. All of these input/output devices are connected to few IOs of FPGA. The keypad used in the system is a 4x4 sized alphanumeric matrix keypad which is connected to FPGA via eight IO lines.

The FPGA used is Altera's Cyclone-ii EP2C5T144C8 which is a low cost, low power FPGA from Intel Altera. This FPGA consists of 4608 Logic Elements (Logic Blocks based on Logic Gates), 119808 RAM bits, 2x PLLs, and 158 IO lines/pins. For FPGA pin planning, configurations, synthesis, analysis, and hardware description a Quartus-II 13.0 Web Edition software tool is used. For complete hardware description a VHDL (Very High-Speed Integrated Circuit Hardware Description Language) is used. It also uses one of the internal PLL (Phase Lock Loop) to increase the clock from 50MHz (on- board osc. chip) up-to 400MHz (internal signals).

SOFTWARE USED

- Intel Quartus-ii(forFPGAVHDL coding)
- Pulse View (for digital signalanalysis)
- Proteus ISIS (for circuitdiagram)

HARDWARE USED

- EP2C5T144C8ALTERACyclone-ii FPGA
- 4x4 Keypad

- Small Buzzer
- Red & Green LEDs (6)
- Relay
- 5v 2A DC SMPS
- 10 KOhm Resistors (4)
- 100 Ohm Resistors (4)
- BC547 Transistor

LITERATURE SURVEY

S. Umbarkar et al. [1] use electronic door lock system using Arduino Platform using three different modes namely keypad, Bluetooth and GSM modules. These three modules work with a 4-character password with a keypad matrix. A Bluetooth module was used to establish a connection between a smart phone and a door lock Bluetooth kit and password to unlock the door. The GSM module was used to enter passwords on his cell phone via text message to unlock or unlock the door. It also sent a text message about this module in the event of three failed attempts to enter the password and used the buzzer as an unauthorized login warning. Servo Motor was used to represent the actions of locking and opening the door. The 16X2 LCD display was used to display / interact with the person trying to lock / unlock the door such as "Enter Password", "Incorrect

Password", in other words, reflects the current state of model usage. Mei-Chuan Tseng et al. [2] suggested how to monitor the door opening function using a single wrist-worn sensor. It can monitor the movement of the upper limb of a person while performing the activities of daily life. It had three subtitles from the complete movement of the door opening which includes holding, rotating and opening the door. the proposed system can detect and identify these signals. The data collection phase includes a 3-axis accelerometer collection and a gyroscope data sensor worn on the wrist.. Sriharsha B S et al. [3] designed and implemented a security system using Arduino, 16x2 LCD, 4x4 keypad matrix and Piezo buzzer that can be used for various applications such as bank locks, BIOS locks on computers, security departments, etc. This program contains a pre-defined password entered by the user each time they want to open a door. The user is instructed to enter a password to unlock the door read by Arduino. The door will open for a period of time allowing user access if the entered password matches the previously defined password. If the entered password is incorrect, a beep sound is generated to alert you to login. The proposed system was developed in an Arduino kit that included ATMega.

METHODOLOGY

FPGA based VGA signal generator is a hardware VGA driver based on Field Programmable Gate Array (FPGA). This driver is implemented on Altera's Cyclone-ii FPGA (EP2C5T144C8). As shown in circuit diagram, out of 152 I/Os only 20 I/Os are used to generate 18-bit RGB VGA signal. This driver generates a VGA signal of industrial standard resolution of 640x480 at 60Hz frame rate.

The EP2C5T144C8 Cyclone-ii FPGA based board used in this project consists of on-board flash memory to hold PLB (Programmable Logic Block) configurations, SM (Switch Matrix) configurations, and LUTs (Look-Up Tables). It also consists of on-board 3.3v voltage regulator, and crystal oscillator chip which generates 50MHz stable frequency which is feed into Pin_17 of FPGA. As per the VGA industrial standard resolution of 640x480 (@60Hz) thepixel clock frequency is 25.175MHz which is approximately half of on-board oscillator's output clock frequency. To convert this 50MHz clock at Pin_17 of FPGA into 25MHz internalclock an inverted input D-flipflop (or T-flipflop) RTL is described in VHDL to divide this clock by 2 (i.e., 50MHz/2 = 25MHz)

As shown in above block diagram, the system consists of Altera's Cyclone-ii FPGA and various input and output devicessuch as LEDs, buzzer, electro-magnetic solenoid lock, 4x4 Keypad, etc. The EP2C5T144C8 is the backbone of complete system. It is responsible for complete systematic operations and behaviour of the system. The EP2C5T144C8 FPGA is a hardware configurable digital logic device which is powerful enough to handle and execute multiple IO devices concurrently completely based on described hardware (RTL). All

the output devices such as LEDs, buzzer, and solenoid lock are connected to this FPGA device via few of its IO pins. The IO pins for this output devices are configured as output (sourcing) 24mA, 3.3v compatibility which is enough to drive/control devices like 3/5mm LEDs. The LEDs are connected to few configured output pins of FPGA via 100Ohm resistors. The sourcing current and voltage capacity on any pin of FPGA is limited to 24mA, 3.3v which is not enough to driver/control output devices such as buzzer, and solenoid lock because these devices require more voltage and current probably around 5-12v, 200mA-1000mA. In order to drive such output devices (buzzer, solenoid lock) a driver circuit is used which consists of a single resistor (100Ohm), a NPN type BJT transistor (BC547/2N2222), and a general purpose PN-Junction diode (1N4007). The FPGA signals/outputs to particular configured output pin which is connected to base of BJT BC547 via 100Ohm resistor. The NPN BJT BC547 is configured as Common Emitter configuration which requires very less current and voltage level on its base in order to conduct current through its collector-emitter path. Between this collector and emitter path an output device (buzzer, solenoid lock) is connected via +vcc (5v-12v) to collector of BJT. In case of inductive/electro- magnetic devices such as solenoid-lock, relay, etc. a flyback protection diode is required. Whenever FPGA signals totransistor-based driver circuit it switches this el1ectro-magnetic output devicebetween on-off state. Such state switchingcauses this inductive device to release/discharge its stored energy (in form of magnetic flux) back into electric spikes which causes huge reverse current and voltage spikes for very short time period (uS to mS). This small time period voltage current spikes can go above

(always) operating voltage of driver circuit (5v-12v) which is enough to damage the transistor and connected FPGA. In order to minimize and reduce such revers voltage spikes a PN-junction diode 1N4007 is connected in reverse bias with the output device. This diode is also called as fly-back protection diode. However, for devices like buzzer it is not really required. As devices like buzzer doesn't generates any reverse current/voltage spikes. The 4x4 alphanumeric keypad is connected to eight IO pins of FPGA. Out of these eight IO pins 4 are configured as output were other

4 are configured as input. The 4 output configured pins are used to driver 4 ROWs of keypad. Another 4 input configured pins are used to read 4 COLs of keypad. For COLs pull-down purpose 4x 10KOhm resistors are used which are connected between COL pins and GND. In order to detect any key press FPGA continuously scans (Set/Reset) ROW pins of keypad while reading and checking states from all COL pins of keypad in loop. The complete hardware design is programmed/modelled in VHDL (Very High-Speed Integrated Circuit Hardware Description Language) with structural and behavioural approaches. For synthesis, fitting, configurations, testing, generation, and programming a Quartus II (version 13.0) Web Edition software tool is used.

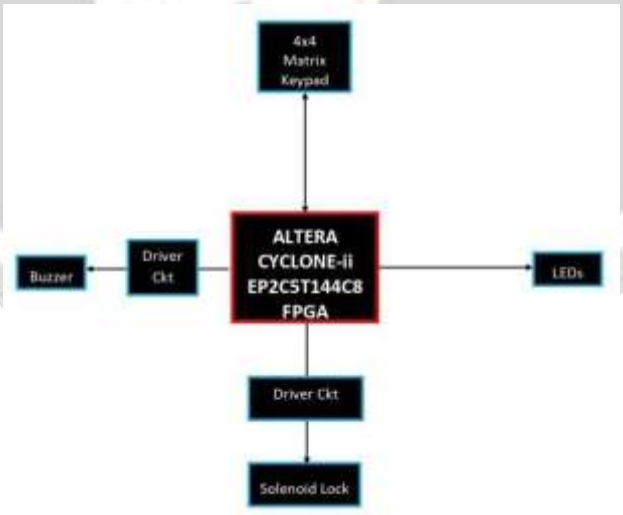

Fig.1 Block Diagram

APPLICATIONS

- FPGA based Digital Door Lock System is a portable battery based door locking system which can be used for home security purpose.
- It can also be used in automobiles for door locking.

OBJECTIVE

Objective of this project is to build and test an ALTERA Cyclone-ii EP2C5T144C8 FPGA based digital pass- key door locking/unlocking security system.
For locking and unlocking of door, a electro-magnetic solenoid lock is used and for indication purpose few LEDs and buzzer is also used.

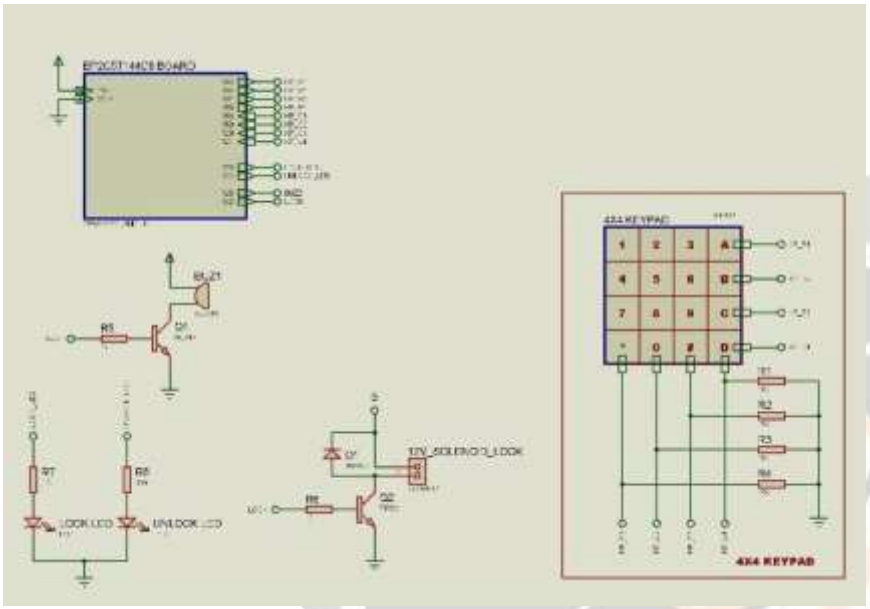

Fig.2 Circuit Diagram

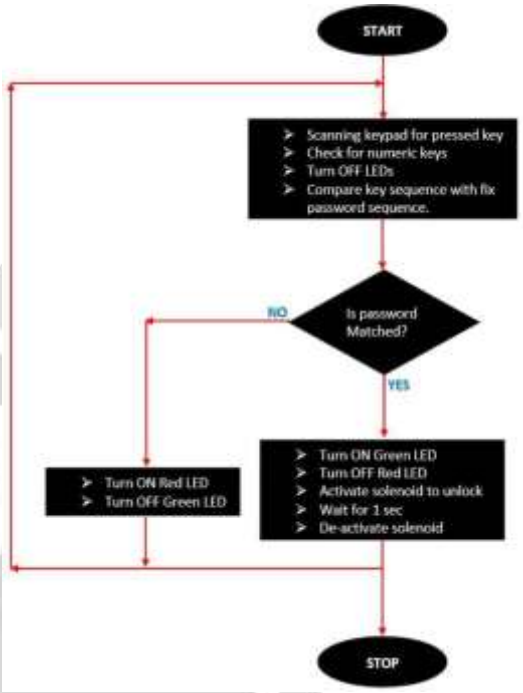

Fig.3 Flow Chart

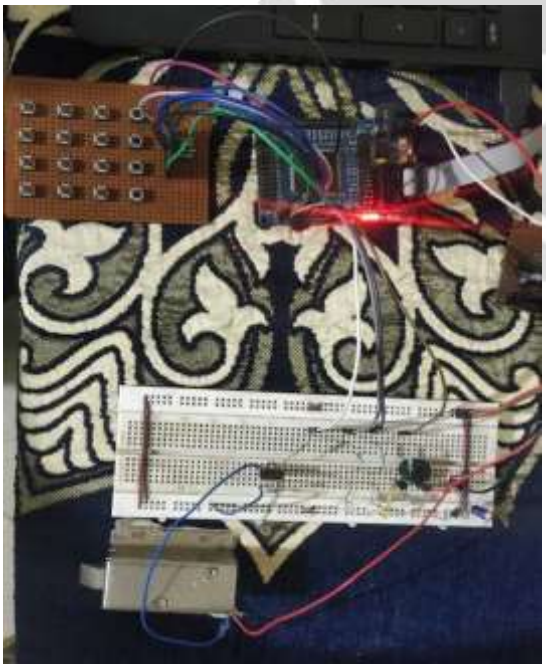

Fig.4 OUTPUT

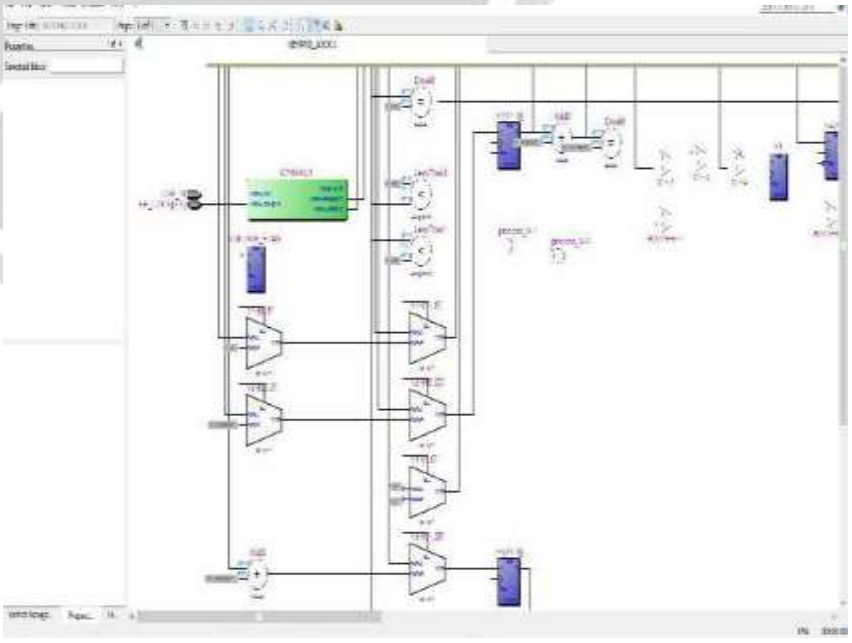

Fig.5 Schematic Part

PROJECT OUTPUT

REFERENCE

- https://www.researchgate.net/publication/336253923_Microcontroller_Based_Dig ital_Door_Lock_Security_System_Using_ Keypad
- https://www.researchgate.net/publication/361265944_Password- Based_Smart_Door_Locking_System
- https://www.ijraset.com/research- paper/paper-on-door-lock-security- systems https://www.researchgate.net/publication/362751143_Design_and_implementation_of_a_combinational_l ock_state_system_using_VHDL
- https://www.academia.edu/4816163/FP GA_Based_Implementation_of_Electroni c_Safe_Lock
- Reference manual,2011,Digilent Nexys2 Board Refference Manual, Digilent Inc., Pullman, WA99163,Doc: 502-134
- Santosh Gautam,2013,FPGA: Based Security login System, retrieved from http://www.academia.edu/3717086/FPGA_Based_Security_login_System