FPGA BASED IMPLEMENTATION OF NEW HYBRID CONFIGURATION 31 LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES FOR REDUCED THD

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ABSTRACT

Application of multilevel inverters for higher voltage goals in industries has become more popular. In this study, new structures for symmetric, asymmetric and hybrid multilevel inverter are recommended. The proposed structure is used in high-voltage levels. The proposed structure can generate a great number of voltage levels with minimum number of power electronic components such as Insulated Gate Bipolar Transistors (IGBT) and gate drivers. For proposed asymmetric and hybrid inverter, new methods for determination of DC voltage sources values are presented. Comparison of the results of various multilevel inverters is presented to reflect the merits of the recommended structures. The operations of the proposed multilevel inverter structures are verified with the experimental and simulation results of an asymmetric 31-level. Fundamental frequency-switching method is applied to the new topologies to trigger the power switches for controlling the voltage levels generated on the output. Verification of the analytical results is performed using MATLAB/SIMULINK software.

Keyword: *IGBT, gate drivers, multilevel inverter, hybrid level, MATLAB/SIMULINK.*

1. INTRODUCTION

A power inverter, or inverter, is an electrical power converter that changes Direct Current (DC) to Alternating Current (AC). Solid-state inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large utility high applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. But in normal inverters the THD is much higher. The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple DC voltage sources. The commutation of the power switches aggregate these multiple DC sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency Pulse width modulation (PWM).

2. LITERATURE REVIEW

Ueda .F. et al, (1995), proposed a technique of parallel connection of power devices by using current sharing reactors for pulse width modulated (PWM) inverters is reported. The proposed technique not only increases the current capacity but also decreases the output harmonic contents. The output voltage waveforms of the proposed inverter have certain voltage levels during their half cycles, thus it is anticipated that it will be difficult to analyze the output waveforms. For such waveforms, a frequency analysis approach is described, whose results are verified by experiments. Vorperian .V. et al, (1990) , a new proposed a circuit-oriented approach to the analysis of pulse width modulation (PWM) converters is presented. This method relies on the identification of a three-terminal nonlinear device, called the PWM switch, which consists of only the active and passive switches in a PWM converter. Once the invariant properties of the PWM switch are determined, its average equivalent circuit model can be derived. This model is versatile enough to easily account for storage-time modulation of bipolar junction transistor(s) (BJTs); the DC- and small-signal characteristics of a large class of PWM converters can then be contained by a simply replacing the PWM switch with its equivalent circuit model. Lai.J. S. et al, (1996), proposed a multilevel voltage source converters are emerging as a new breed of power converter options for high-power applications. The multilevel voltage source converters typically synthesize the staircase voltage wave from several levels of DC capacitor voltages. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The techniques to balance the voltage between different levels normally involve voltage clamping or capacitor charge control. There are several ways of implementing voltage balance in multilevel converters. Peng F. Z et al, (1997), proposed a cascade multilevel inverter is proposed for static VAR compensation/generation applications. The new cascade M-level inverter consists of (M-1)/2 single-phase full bridges in which each bridge has its own separate DC source. This inverter can generate almost sinusoidal waveform voltage with only one time switching per cycle. It can eliminate the need for transformers in multi pulse inverters. A prototype static VAR generator (SVG) system using 11-level cascade inverter (21-level line-to-line voltage waveform) has been built. The output voltage waveform is equivalent to that of a 60-pulse inverter. Tolbert L. M. et al, (1999), proposed a multilevel power converters as an application for high-power and/or high-voltage electric motor drives. Multilevel converters: (1) can generate near-sinusoidal voltages with only fundamental frequency switching; (2) have almost no electromagnetic interference or common-mode voltage; and (3) are suitable for large volt ampere-rated motor drives and high voltages. The cascade inverter is a natural fit for large automotive all-electric drives because it uses several levels of DC voltage sources, which would be available from batteries or fuel cells. The back-to-back diode-clamped converter is ideal where a source of AC voltage is available, such as in a hybrid electric vehicle.

2.1 Cascaded H-Bridge inverter

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 3.1. Each Separate DC Source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the AC output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources. Multilevel cascaded inverters have been proposed for such applications as static VAR generation, an interface with renewable energy sources, and for battery-based applications. Peng has demonstrated a prototype multilevel cascaded static VAR generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system. The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected. Peng and Joos have also shown that a cascade inverter can be directly connected in series with the electrical system for static VAR compensation. Cascaded inverters are ideal for connecting renewable energy sources with an AC grid, because of the need for separate DC sources, which is the case in applications such as photovoltaic or fuel cells. Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultra-capacitors are well suited to serve as SDCSs. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an AC supply. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking. Cascade topology that uses multiple DC levels, which instead of being

identical in value are multiples of each other. It also uses a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform.

2.2 Multi carrier technique

The most common and popular technique of digital Pure-sine wave generation is pulse width modulation The PWM technique involves generation of a digital waveform, for which the duty cycle is modulated such that the average voltage of the waveform corresponds to a pure sine wave. The simplest way of producing the PWM signal is through comparison of a low-power reference sine wave with a triangle wave. Multicarrier PWM methods uses high switching frequency carrier waves in comparison to the reference waves to generate a sinusoidal output wave. The Figure shows multicarrier PWM waveform for cascaded multilevel inverter. In general inverter with m-level, m-1 carrier with same frequency f_c and same peak to peak amplitude Ac are disposed. The reference or modulation waveform has peak to peak amplitude A_r and frequency f_r.

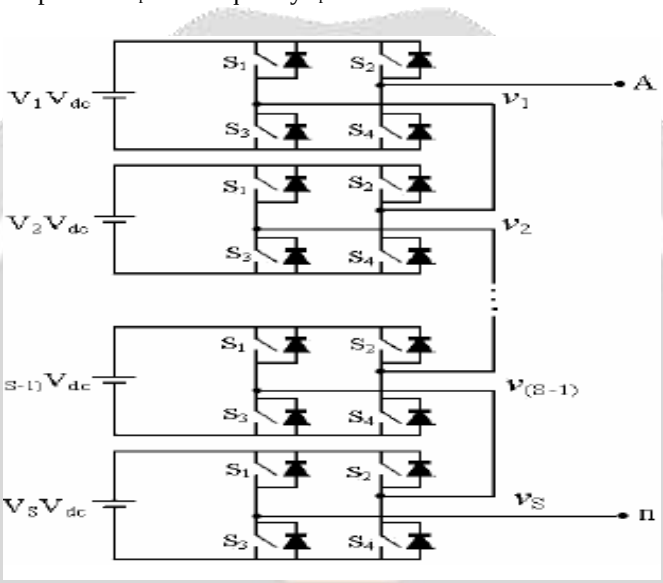

Fig - 1: Single-Phase Structure of a Multilevel Cascaded H-Bridges Inverter

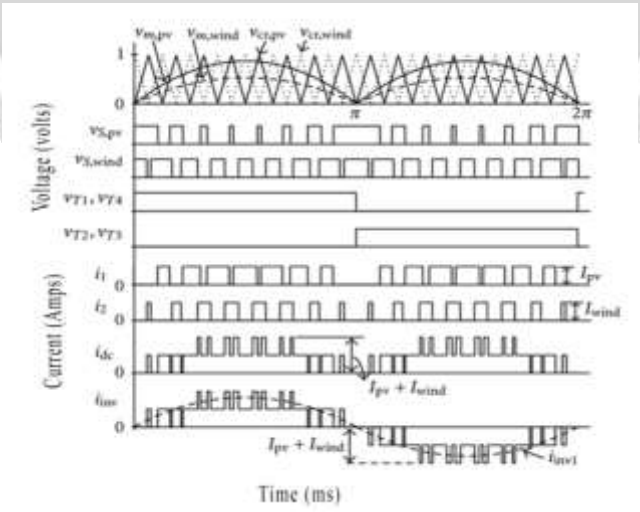

Fig - 2: Multi Carrier Modulations

The reference waveform is compared with carrier signals and if it is greater than a carrier signal then switch/device correspond to that carrier is switched on and if the reference is less than carrier signals then device correspond to

carrier is switched off. The Sinusoidal pulse width modulation is commonly used in Industrial application. The frequency of reference signal f_r determines the inverter output frequency f_o and its peak amplitude A_r controls the modulated index M and then in turn the RMS output voltage V_o. Here the modulation index is defined as the ratio of amplitude of reference signal to the amplitude of carrier signal. The RMS output voltage can be varied by varying the modulation index M. If δ is the width of each pulse then RMS output voltage can be found from $V_o = V_s\sqrt{((p\delta)/(\pi))}$. In this thesis multi carrier pulse width modulation technique is used to generate the fifteen level output voltage. Seven equal amplitude carrier triangular signals with offset are compared with the sinusoidal reference signal. The carrier signal frequency is 10 kHz and the modulation index is 0.8.

3. PROPOSED SYSTEM

3.1 Proposed symmetric multilevel inverter

The basic unit for the proposed symmetric multilevel inverter is shown in Figure 3.In this circuit, when the switch S is turned off, the current flows from the diode, but when the switch S is turned on, the diode is reverse biased and the current flows from dc voltage source (V) which is connected in series with switch S. Hence, using this method the output voltage is controlled. This method is the base of the proposed multilevel inverter. This basic circuit can generate five levels in output voltage and Table 1gives the values of output voltages (V_o) for different states of S, T_1 … and T_4 switches. The values of output voltages (V_o) for different states of S1, S2… Sn, T1 … and T4 switch. Note that there are several different switching patterns for generating the zero level. The number of output voltage levels and the total number of switches in the recommended symmetric multilevel inverter are obtained.

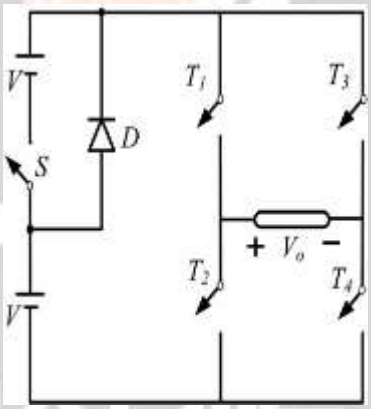

Fig – 3: Basic Circuit of the Proposed Multilevel Inverter

Table -1 ON Switches Look-Up Table for Proposed Multilevel Inverter

State	Switches states					Output voltage
	S	T1	T2	T3	T4	
1	0	1	0	1	0	0
2	0	1	0	0	1	V
3	0	0	1	1	0	-V
4	1	1	0	0	1	2V
5	1	0	1	1	0	-2V

3.2 Proposed hybrid multilevel inverter

The switches of the full-bridge converter in the proposed symmetric and asymmetric structures have to withstand voltage equal to the sum of all the dc voltage sources and it is restricted in the high-voltage levels. Therefore a three-level inverter is used in series with the proposed symmetric and asymmetric topologies. Here the MOSFET based full bridge inverter circuit is cascaded for this thirty one level inverter. Three switches also connected with this H-Bridge inverter circuit. The snubber circuit (RC) is connected across all the switches for protecting the switching

devices from dv/dt and di/dt ratings. Spartan 3E is used for generating the PWM signals for both the H bridge inverter circuit and the bidirectional switching devices. By using the VLSI the program will be developed for generating the PWM signals. In this thesis the maximum output power level of the inverter is 10W; the maximum output voltage level of the inverter is 72 volts. For this power rating we can use lamp or small size motors. The voltage levels of the thirteen levels are (V_{dc}, $6V_{dc}/7$, $5V_{dc}/7$, $4V_{dc}/7$, $3V_{dc}/7$, $2V_{dc}/7$, $V_{dc}/7$,0, $-V_{dc}/7$, $-2V_{dc}/7$, $-3V_{dc}/7$, $-4V_{dc}/7$, $-5V_{dc}/7$, $-6V_{dc}/7$, $-V_{dc}$) From the DC supply. The voltage levels of the three sources are different. So this method of configuration is called as asymmetrical multilevel inverter. The inverter level is decided by both the modulation index and the applied DC voltage level of the inverter. By adjusting the different voltage level also we can able to increase the number of levels of the inverter. A FPGA controller is used for generating the PWM signals the inverter circuit. The switching devices used in this single phase inverter are MOSFET (IRF840). The power handling capacity of the inverter is low because the hardware is developed in a prototype. The output voltage of the two proposed hybrid multilevel inverters can be evaluated by,

$$V_o = V_{o1} + V_{o2} \quad (1)$$

For the proposed hybrid topologies, the voltage of the full-bridge converter can be determined for two goals.

- To generate a large number of levels in the output voltage waveform.
- To reduce using switches with high-voltage capability and reduction of the blocking voltage on the switches of the full-bridge converter. In addition, for the recommended hybrid structure based on the asymmetric structure, the value of V_f and the number of output voltage levels are given by the following equations

$$V_f = (V_{o1,max}) + V_1 \quad (2)$$

Using this method leads to halving of the blocking voltage on the switches of the full-bridge converter. Consequently, the proposed hybrid topologies will be suitable for high-voltage applications.

3.3 31-level inverter

The proposed single-phase thirty one-level inverter was developed from the seven-level inverter. It comprises a Single phase conventional H-bridge inverter, three switches, and three voltage sources. This H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, for inverters of the same number of levels. Proper switching of the inverter can produce fifteen output-voltage levels (V_{dc}, $6V_{dc}/7$, $5V_{dc}/7$, $4V_{dc}/7$, $3V_{dc}/7$, $2V_{dc}/7$, $V_{dc}/7$,0, $-V_{dc}/7$, $-2V_{dc}/7$, $-3V_{dc}/7$, $-4V_{dc}/7$, $-5V_{dc}/7$, $-6V_{dc}/7$, $-V_{dc}$) from the DC supply voltage. 31 level inverter switching operation is tabulated in table 2,

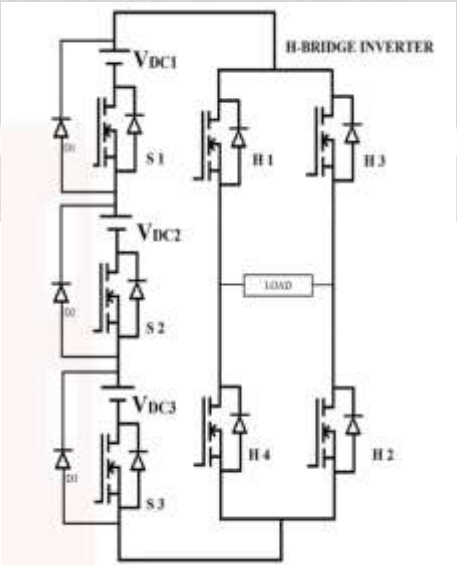

Fig - 4: 31 Level Inverter Circuit Diagram

- The proposed inverter's operation can be divided into fifteen switching states; the required thirty one levels of output voltage were generated as follows.
- Maximum positive output (V_{dc}): H1 is ON; connecting the load positive terminal to V_{dc}, and H2 is ON, connecting the load negative terminal to ground. The switches S1, S2, S3 are ON the voltage applied to the load terminals is V_{dc}.
- 6/7 positive output (6 V_{dc}/7): H1 is ON; connecting the load positive terminal to V_{dc}, and H2 is ON, connecting the load negative terminal to ground. The switches S1, S2, S3 are ON the voltage applied to the load terminals is $6V_{dc}/7$.
- 5/7 Positive output ($5V_{dc}/7$): H1 is ON; connecting the load positive terminal to Vdc, and H2 is ON, connecting the load negative terminal to ground. The switches S1, S3 are ON the voltage applied to the load terminals is 5Vdc/7.
- 4/7 Positive output (4Vdc/7): H1 is ON; connecting the load positive terminal to Vdc, and H2 is ON, connecting the load negative terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is 4Vdc/7.

Table – 2 Switching Operations of 31 Level Inverter

Voltage Level	S_1	S_2	S_3	H_1	H_2	H_3	H_4
V_{dc}	ON	ON	ON	ON	ON	OFF	OFF
$6V_{dc}/7$	ON	ON	ON	ON	ON	OFF	OFF
$5V_{dc}/7$	ON	ON	OFF	ON	ON	OFF	OFF
$4V_{dc}/7$	ON	OFF	ON	ON	ON	OFF	OFF
$3V_{dc}/7$	ON	OFF	OFF	ON	ON	OFF	OFF
$2V_{dc}/7$	OFF	ON	OFF	ON	ON	OFF	OFF
$V_{dc}/7$	OFF	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF
$-V_{dc}/7$	OFF	OFF	OFF	OFF	OFF	ON	ON
$-2V_{dc}/7$	OFF	ON	OFF	OFF	OFF	ON	ON
$-3V_{dc}/7$	ON	OFF	OFF	OFF	OFF	ON	ON
$-4V_{dc}/7$	ON	OFF	ON	OFF	OFF	ON	ON
$-5V_{dc}/7$	ON	ON	OFF	OFF	OFF	ON	ON
$-6V_{dc}/7$	ON	ON	ON	OFF	OFF	ON	ON
$-V_{dc}$	ON	ON	ON	OFF	OFF	ON	ON

- 3/7Positive output (3Vdc/7): H1 is ON; connecting the load positive terminal to Vdc, and H2 is ON, connecting the load negative terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is $3V_{dc}/7$.
- 2/7 Positive output (2Vdc/7): H1 is ON; connecting the load positive terminal to V_{dc}, and H2 is ON, connecting the load negative terminal to ground. The switches S2 is ON and S1, S3 is OFF. The voltage applied to the load terminals is 2Vdc/7.
- 1/7 Positive output (1Vdc/7): H1 is ON; connecting the load positive terminal to V_{dc}, and H2 is ON, connecting the load negative terminal to ground. The switches S3 is ON and S1, S2 is OFF. The voltage applied to the load terminals is $1V_{dc}/7$.
- Zero output: All the switches S1, S2, S3, H1, H2, H3, and H4 are in OFF position.
- 1/7 Negative output ($-1V_{dc}/7$): H3 is ON; connecting the load positive terminal to V_{dc}, and H4 is ON, connecting the load negative terminal to ground. The switches S3 is ON and S1, S2 is OFF. The voltage applied to the load terminals is $-1V_{dc}/7$.
- 2/7 Negative output ($-2V_{dc}/7$): H3 is ON, connecting the load positive terminal to V_{dc}, and H4 is ON, connecting the load negative terminal to ground. The switches S2 is ON and S1, S3 is OFF. The voltage applied to the load terminals is -2Vdc/7.

- 3/7 Negative output (-3V_{dc}/7): H3 is ON, connecting the load positive terminal to V_{dc}, and H4 is ON, connecting the load negative terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is -3V_{dc}/7.
- 4/7 Negative output (-4V_{dc}/7): H3 is ON, connecting the load positive terminal to V_{dc}, and H4 is ON, connecting the load negative terminal to ground. The switches S1 is ON and S2, S3 is OFF. The voltage applied to the load terminals is -4V_{dc}/7.
- 5/7 Negative output (-5V_{dc}/7): H3 is ON, connecting the load positive terminal to V_{dc}, and H4 is ON, connecting the load negative terminal to ground the switches S1, S3 are ON the voltage applied to the load terminals is -5V_{dc}/7.
- 6/7 Negative output (-6V_{dc}/7): H3 is ON, connecting the load positive terminal to V_{dc}, and H4 is ON, connecting the load negative terminal to ground. The switches S1, S2, S3 are ON the voltage applied to the load terminals is –6V_{dc}/7.
- Maximum Negative output (-V_{dc}): H3 is ON; connecting the load positive terminal to V_{dc}, and H4 is ON, connecting the load negative terminal to ground. The switches S1, S2, S3 are ON the voltage applied to the load terminals is –V_{dc}.

3.4 Calculation of Total Harmonic Distortion

For calculation of the Total Harmonic Distortion (THD) in the proposed multilevel inverter, the amplitude of the harmonics in the output voltage waveforms of the inverter must be calculated. For this case, sing Fourier analysis to calculate the amplitude of these harmonics. Based on Figure 4.6, the amplitude of the nth-harmonic in the 11-level output b11n can be obtained as:

$$b_{11n} = \frac{2}{n\pi}\sum_{k=0}^{4}\left[\cos\left(n\sin^{-1}\left(\frac{k}{5M}\right)\right)\right] - \cos\left(n\pi - n\sin^{-1}\left(\frac{k}{5M}\right)\right) \qquad (3)$$

IV CONCLUSION

In this proposed system multilevel inverters offer improved output waveforms and lower THD. A novel PWM switching scheme for the proposed multilevel inverter. In this thesis only one reference signal and is compared with a triangular wave signal to generate the PWM signals. Here there are three different DC voltage levels are used in this multi-level inverters. So this method of configuration is known as asymmetrical cascaded inverter. It was shown that the proposed topologies need fewer numbers of IGBTs and gate drivers. The following table 3 shows the comparison of 15 and 31 level inverters.

Table - 3 Comparison of the Calculation THD

The Number of Output Voltage Levels	THD [%]
11-level	6.57
15-level	5.38
31-level	4.38

These factors reduce the installation area, circuit size and cost. It was shown that the value of the blocked voltage by the switches of the proposed asymmetric structure is less than the other asymmetric structures. The simulation and experimental results for a 31-level asymmetric inverter was presented and a THD value of a 15-level and a 31 level multilevel inverter was compared. The THD value of a thirty one level inverter is 4.38% and fifteen level inverter THD value is 5.38%.

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