.

Fast FPGA Routing Approach Using Stochestic Architecture

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ABSTRACT

In this thesis I am going to reconfigure the hardware and connect each an every block in FPGA for improve FPGA performance much faster and try to overcome power consumption issue using Stochestic Architecture. In this Architecture will connect each un-routed blocks , by providing nearest routing path related to the CLB configuration .For this configuration use wire or microcell over these connection, so it perform much accurate and remove un-wanted connections inside the Routing connection.

Design Fast FPGA performance, so I want to make Routing connection maximum shortest path and connect all switch or block connection using Cross-bar Algorithm, so make routing more accurate, improve connection of block ratio, reduce area, Time, power according to the configuration .I try to reduce clock delay and frequency, so ultimately performance of FPGA also increase and perform much faster, and finally Dump on FPGA Hardware.

Keyword: - Global Detailed Routing **,** Computer-aided design (CAD), Field programmable gate array (FPGA) architecture, Stochestic, FPGA routing.

1. INTRODUCTION

The appearance of FPGAs, in recent years, has resulted in enormous possibilities for the implementation of sophisticated algorithms of high complexity, in a variety of important applications, by using low-cost, very efficient, high-speed, reconfigurable hardware. However, research effort towards the applications of FPGAs for higher-order statistics computations has not yet been reported.

The objective of this project is to design an FPGA based reconfigurable processor for the computation of higher order cross moments. A high-level design approach is adopted to realize the matrix multiplier based algorithm for the computation of higher order cross moments in hardware i.e. FPGA. These advantages, which are attributable to the user-programmability of FPGAs , provide a faster time-to-market and less pressure on designers, because multiple design iterations can be done quickly and inexpensively.

However, user-programmability also has drawbacks: the logic density and speed performance of FPGAs is considerably lower than those of the alternatives. While developments over the last few years have shown significant improvements in FPGAs, much research is still needed before the best FPGA designs are discovered.

1.1 FPGA ARCHITECTURE

FPGA Architecture depicts a basic island-style FPGA. Each LB has a capacity, which represents the number of lookup tables (LUTs) and flip-flops that can be contained therein. LBs connect to wire segments through programmable switches in the connection blocks (CBs). Wire segments connect to other wire segments using programmable switches in the SBs. Connections between LBs are made by turning on the appropriate switches in the SBs and CBs.

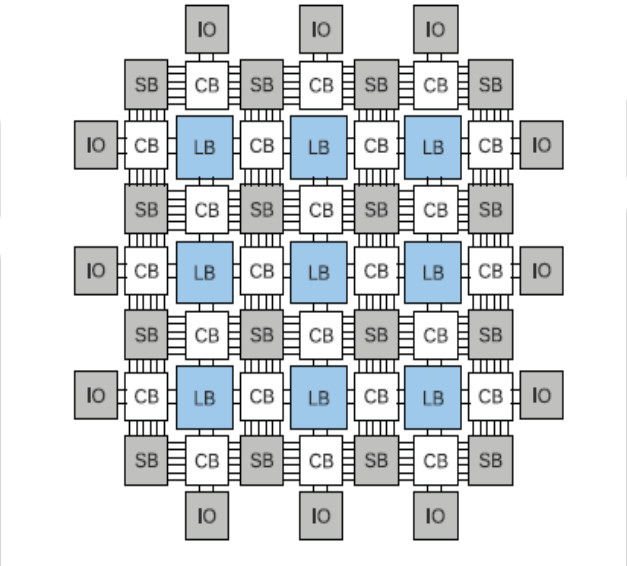

Fig -1: FPGA Architecture

1.2 COMPARITION OF SWITCH BLOCKS

In each Switch Block, each incoming track can be connected to three outgoing tracks. The topology of each block, however is different. The difference between the blocks is exactly which three outgoing tracks each incoming track can be connected. In Disjoint block, the switch pattern is “symmetric”, in that if all the tracks are numbered as shown in Figure , each track numbered ‘i’ can be connected to any outgoing track also numbered.

This means that the routing fabric is divided into “domains”; if a wire is implemented using track ‘i’, all segments that implement that wire are restricted to track ‘i’. For example, an incoming signal to switch block at track 1 can only connect to track 1 in adjacent channels. This partitions the routing fabric into W subsets, and thus results in reduced routability compared to other switch blocks.

In the Universal block, the focus is on maximizing the number of simultaneous connections that can be made using the block . The Wilton switch block is same as Disjoint, except that each diagonal connection has been rotated by one track . This reduces the domains problem and results in many more routing choices for each connection.

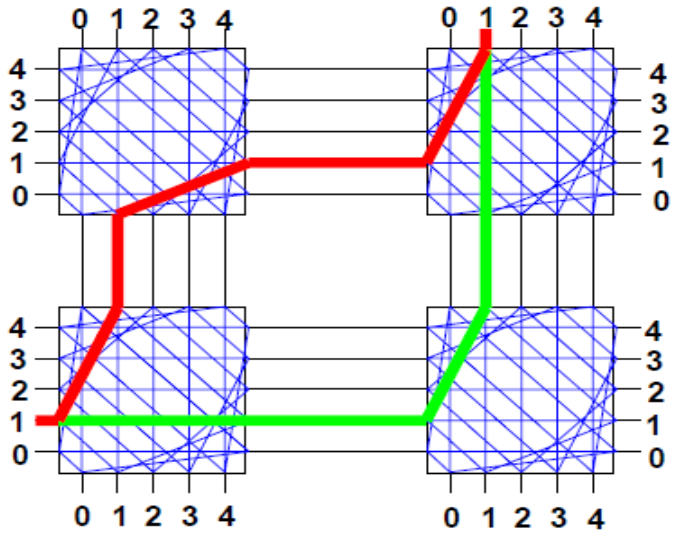

Fig -2: : Two Possible Routes of a Wire using Disjoint block

1.3 SIGNIFICANCE OF ROUTING

In current FPGAs, the most of the tile area is devoted to routing resources and most of the delay of circuits implemented on FPGAs is due to routing. Various routing architecture features such as Fs, Fc, I, the connection blocks, and the switch blocks have a significant impact on the performance and the achievable logic density. In addition, the routing buffers and the programmable connections are also an important factor in determining an FPGA's speed and logic density . Thus, the development of better routing architectures is critical.

1.4 FPGA CAD(Computer Aided Design Tool) FLOW

Designing with FPGAs is much the same as with any other technology. The Computer Aided Design (CAD) software provided by the FPGA vendor (or a third party) is used to convert the given digital circuit (schematic or a high level description in VHDL or Verilog) into a stream of bits, which is then used to program the FPGA. A typical CAD flow employed by most commercial FPGA tools .

A circuit description (normally in high level hardware description language) is first converted to a netlist of basic gates using a process called Synthesis. This netlist of gates is then passed through a technology independent logic optimization process to reduce the number of gates.

Each logic block is then assigned a physical location on the FPGA during the Placement. Finally the required connections are made using the programmable vertical and horizontal channels during the Routing phase.

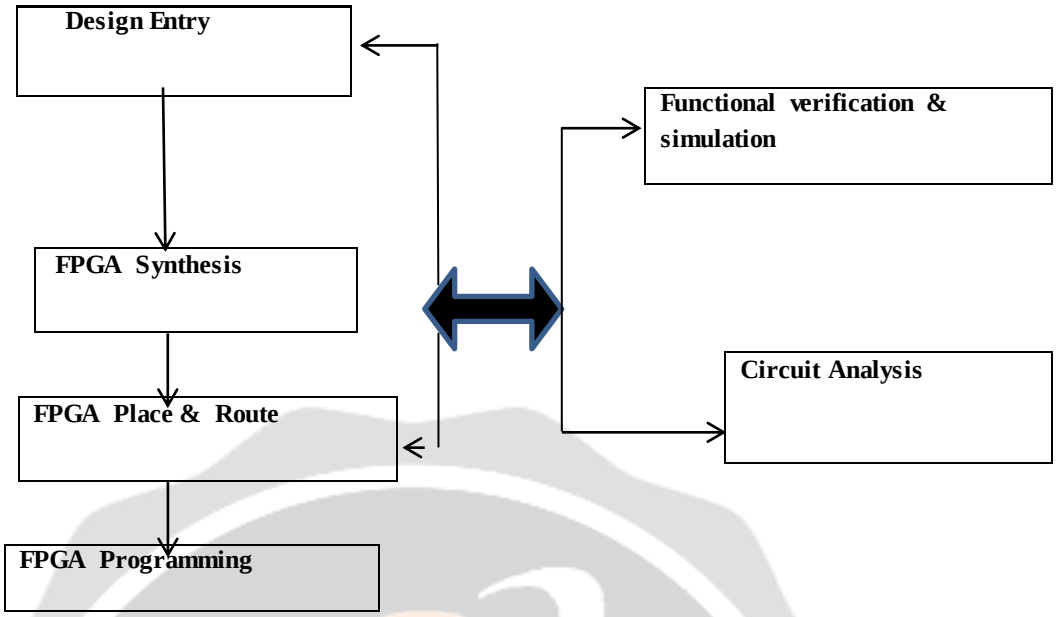

Fig -3: Typical CAD Flow

2. STOCHESTIC ARCHITECTURE

- In Proposed work Design and Implement Effective Architecture for FPGA using Verilog HDL.
- In Routing use Globle route connection between each node and Design Architecture for same Routing signal .
- Using Stochastic model try to design each node and expand each un-routed connection between the Routing blocks , with use of wire and micro cell.
- Select specific track for same and Establish connection using Routing and wire .and also update it on Route and connection .
- Design Route is specific and it match the output High .

Using this mode make multiple connection on different node and it will be also execute and operate all signal at same . It is the main Advantage of this model compare to other research .So multiple connection make Routing connection Reliable and it make system to accelerate for fast performance .The developed methods are tested referring to an architectural template that exposes most degrees of freedom that may be experienced in modern embedded systems.

The main aim is to optimize multi-processor systems, arbitrarily interconnected by means of custom-tuned communication structures . IP cores that can be used as building blocks , Memories, interconnect modules, I/O peripherals. Within the project a library of IPs has been collected and integrated, in order to allow the prototyping of almost completely arbitrarily heterogeneous architectures.

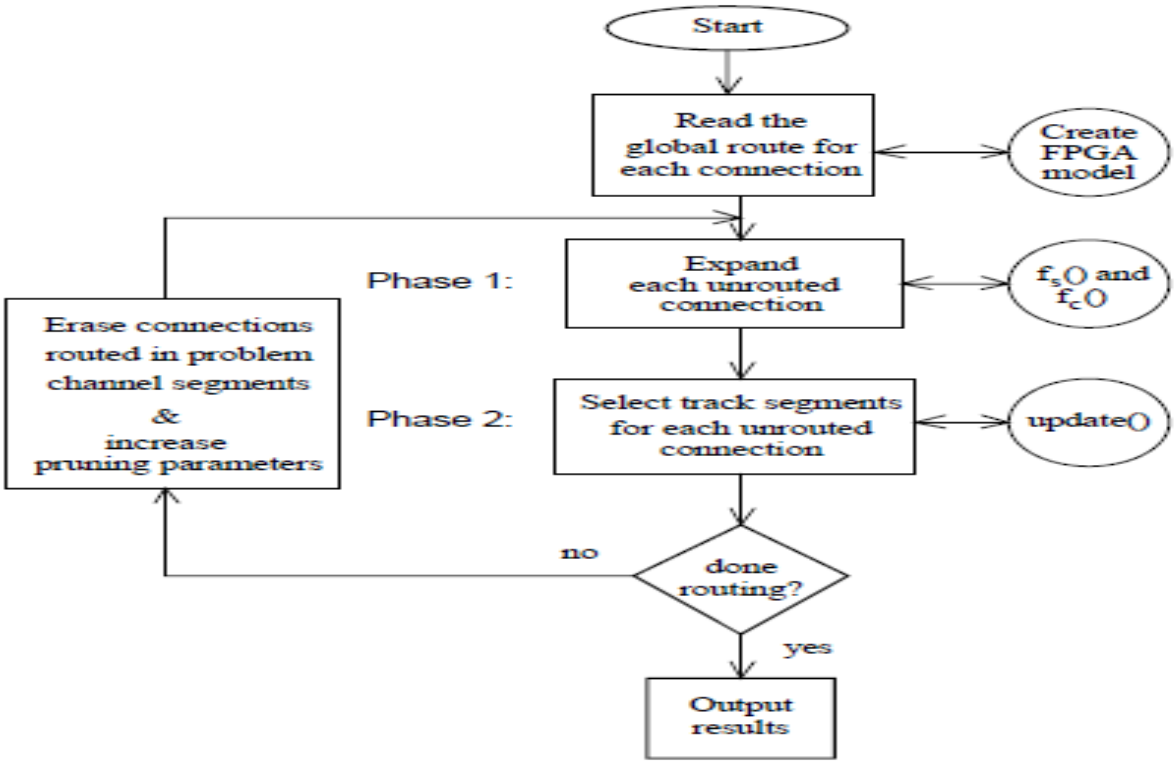

Fig -4: Stochestic Architecture Flow

3. Results

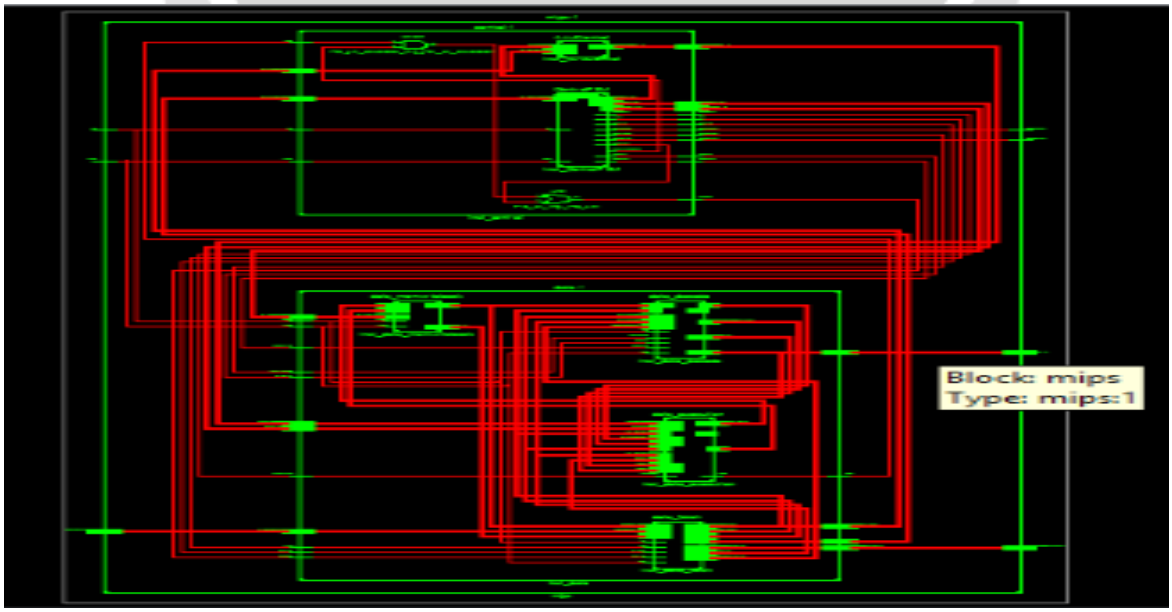

Fig -5: MIPS code RTL Synthesis

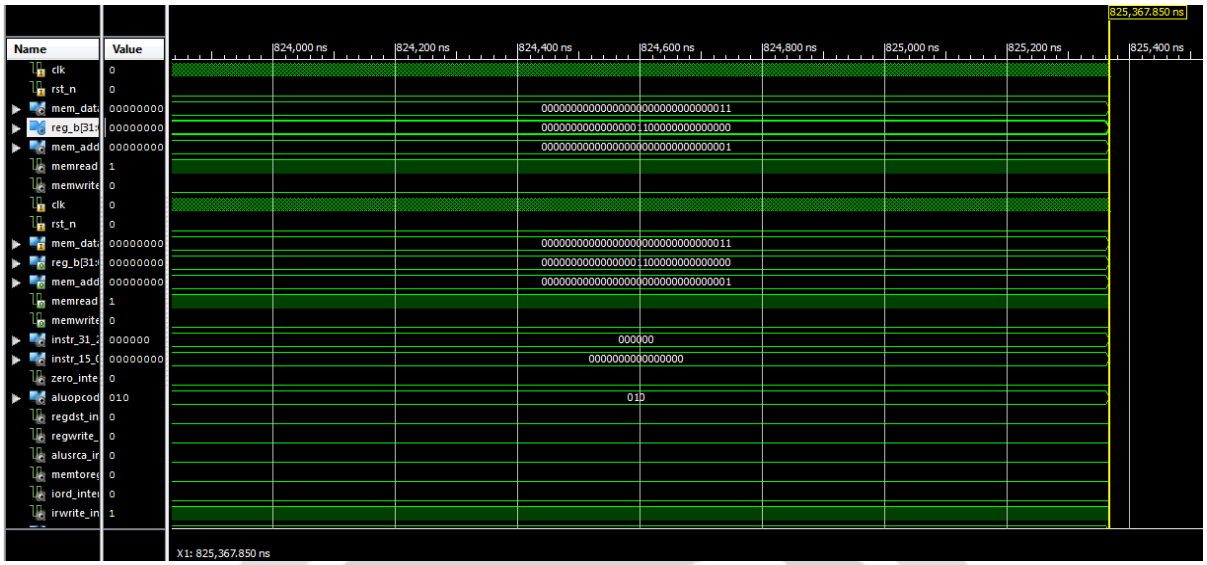

Fig -5: MIPS Simmulation Result

Device utilization summary			
Number of Slices	1334	4656	28%
Number of Slice Flip Flops	1235	9312	13%
Number of 4 input LUTs	1496	9312	16%
Number of IOs	100		
Number of bonded IOBs	100	234	43%
Number of GCLKs	1	24	4%

Table 1: Device Utilization Summary

4. CONCLUSIONS

The main focus of this thesis has been the study of FPGA routing architectures with regard to the tradeoff among routability, area and speed performance.The 8-bit Fast FPGA Routing Stochestic Architecture for Design any logic approach using HDL,so the ssystem get minimum and nearest to CLB configuration.The Routing Verification and Testing are shown in the simulation Result.So using fast FPGA Routing design DSP and mathematical processes in different application. Theoretical methods have also been applied to study this issue, using a stochastic modelling approach that predicts, based on combinational analysis, the effect of flexibility on routability. The results of the work in the thesis provide new insights into the design of FPGA routing algorithms and routing architectures.

5. REFERENCES

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