HIGH SPEED AND LOW COMPLEXITY CARRY SKIP ADDER USING REVERSIBLE GATES

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ABSTRACT

In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrementation schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. Then the proposed structure is implemented using reversible logic such as toffoli gate which reduces the complexity by the garbage values, were it increases the speed thus the area, power and delay of the proposed structure is compared with conventional structure.

Keywords: *Carry skip adder (CSKA), High performance, Hybrid variable latency adders, Reversible logics*

1 INTRODUCTION

Adders are a key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. Binary adders are one of the most essential logic elements within a digital system. In addition, binary adders are also helpful in units other than Arithmetic Logic Units (ALU) such as multipliers, dividers and memory addressing. Therefore, binary addition is essential that any improvement in binary addition can result in a performance boost for any computing system and, hence, help improve the performance of the entire system. Achieving higher speeds at lower supply voltages for the computational blocks, with the adder as one the main components, could be crucial in the design of high-speed, yet energy efficient, processors. There are many adder families with different delays, power consumptions, and area usages. Examples include ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adder (PPAs). The descriptions of each of these adder architectures along with their characteristics.

II RELATED WORK

The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1 multiplexers, which can be placed into one or more level structures. The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder.In addition, to lower the propagation delay of the adder, in each stage, the carry look-ahead logics were utilized. Again, it had a complex layout as well as large power consumption and area usage. The figure 1 shows that conventional structure of CSKA which consist of

2:1 multiplexer. In addition, the design approach, whichwas presented only for the 32-bit adder,were not general to be applied for structures with different bits lengths.

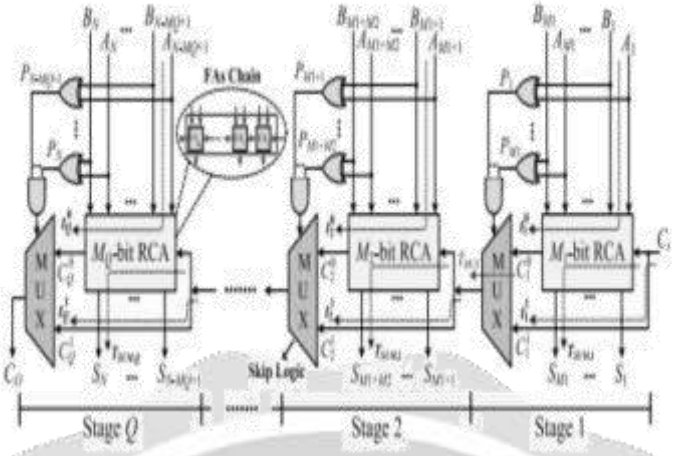


Fig-1: Conventional structure of CSKA

The goal of this method is to decrease the critical path delay by considering a non integer ratio of the skip time to the ripple time on contrary to most of the previous works, which considered an integer ratio.In all of the works reviewed so far, the focus was on the speed, while the power consumption and area usage of the CSKAs were not considered. The carry skip adder has higher speed than conventional one. CSKA reveal reduction in power consumption compared with latest works in these field having reasonably high speed. In addition to the chain of FAs in each stage, there is a carry skip logic. For an RCA that contains N cascaded FAs, the worst propagation delay of the summation of two N-bit numbers, A and B, belongs to the case where all the FAs are in the propagation mode. It means that the worst case delay belongs to the case where,

$$Pi = Ai \oplus Bi = 1 \text{ for } i = 1, \ldots, N \qquad 1.1$$

where Pi is the propagation signal related to Ai and Bi. The equation 1.1 shows that the delay of the RCA is linearly related to N [1]. In the CSKA, the carry skip logic detects this situation, and makes the carry ready for the next stage without waiting for the operation of the FA chain to be completed.

The structure is based on combining the concatenation and the incrementation schemes with the Conv-CSKA structure. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates. The gates, which consist of fewer transistors have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one.

The power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).Now, we describe the internal structure of the proposed CI-CSKA. The adder contains two N bits inputs, A and B, and Q stages.

Extension of conventional CSKA shown in figure 1 and which consists of incrementation block, RCA block, skip logic (AOI or OAI invert). Each stage consists of an RCA block with the size of Mj (j = 1, . . . , Q). In this structure, the carry input of all the RCA blocks, except for the first block which is Ci , is zero (concatenation of the RCA blocks). Therefore, all the blocks execute their jobs simultaneously. when the first block computes the summation of its corresponding input bits (i.e., SM1, . . . , S1), and C1, the other blocks simultaneously compute the intermediate results [i.e., {ZK j+Mj , . . . , ZK j+2, ZK j+1} is given by equation 1.1

$$Kj=\sum_{r=1}^{j-1} Mr(j=2,...,Q)] \qquad 1.2$$

In these proposed structure, the first stage has only one block which is RCA. The stages 2 to Q consist of two blocks of RCA and incrementations. The incrementation block uses the intermediate results generated by the RCA block and the carry output of the previous stage to calculate the final summation of the stage. The internal structure of the incrementation block, which contains a chain of half-adders. In addition, note that, to

reduce the delay considerably, for computing the carry output of the stage, the carry output of the incrementation block is not used.

III. PROPOSED STRUCTURE

In this section, first, the structure of a generic variable latency adder, which may be used with the voltage scaling relying on adaptive clock stretching, is described. Then, a hybrid variable latency CSKA structure based on the CI-CSKA structure

PROPOSED HYBRID VARIABLE LATENCY CSKA STRUCTURE

The proposed hybrid variable latency CSKA structure is in where an Mp-bit modified PPA is used for the pth stage (nucleus stage). Since the nucleus stage, which has the largest size (and delay) among the stages, is present in both SLP1 and SLP2, replacing it by the PPA reduces the delay of the longest off critical paths.

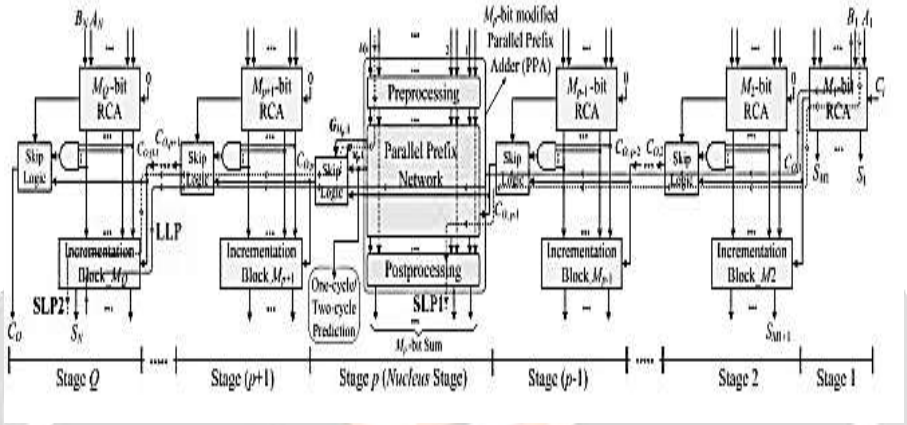


Fig-2: Structure of the proposed hybrid variable latency CSKA.

The figure 2 shows th at structure of the hybrid variable latency CSKA and which consists of PPA, RCA blocks, incrementation block and skip logics.One the advantages of the this adder compared with other prefix adders is that in this structure, using forward paths, the longest carry is calculated sooner compared with the intermediate carries, which are computed by backward paths. In addition, the fan-out of adder is less than other parallel adders, it has a simple and regular layout.

The power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).Now, we describe the internal structure of the proposed CI-CSKA. The adder contains two N bits inputs, A and B, and Q stages.

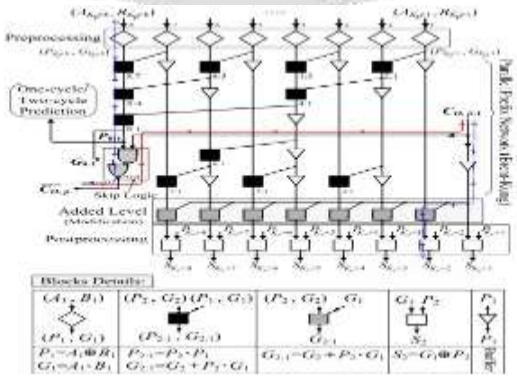


Fig-3: Internal structure of the pth stage of the proposed hybrid variable latency CSKA

The internal structure of the stage p, including the modified PPA and skip logic. In the next level, using Brent–Kung parallel prefix network, the longest carry (i.e., G8:1) of the prefix network along with P8:1, which is the product of the all propagate signals of the inputs, are calculated sooner than other intermediate signals in this network. It should be mentioned that all of these operations are performed in parallel with other stages. Finally, in the postprocessing level, the output sums of this stage are calculated.

IV PROPOSED STRUCTURE USING REVERSIBLE GATES

REVERSIBLE LOGIC

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Reversible logic supports the process of running the system both forward and backward. The reversible logic design attracting more interest due to its low power consumption and low complexity. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, toffoli gate, New Gate sayem gate and peres gate etc.

BUILDING BLOCKS OF TOFFOLI GATE

Toffoli gate (CCNOT gate ,controlled-controlled- not) is a universal reversible logic gate ,named its inventor ,Tommaso Toffoli.

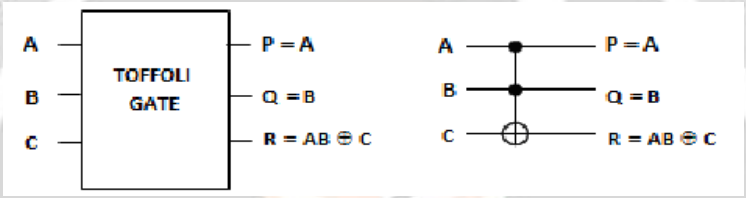
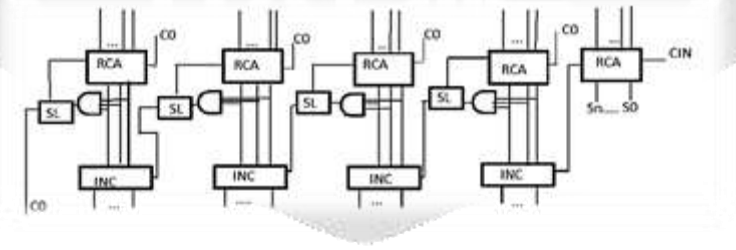


Fig-4: Toffoli gate

The figure 4 shows that 3*3 Toffoli gate which consists of input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB □ C. Where the output P and Q are the garbage values. If the first two bits are set , it flips the third bit. Toffoli gate which consist of 3 inputs and output bits. It can be also described as mapping bits {a,b,c}to {a,b,c XOR (a AND b)}.

PROPOSED BLOCK DIAGRAM USING REVERSIBLE GATES



Stage N…… .... stage 1

Fig-5 : Carry skip adder using reversible gates

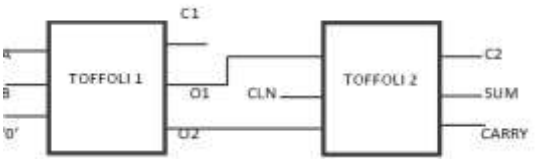


Fig-6: Full adder design using toffoli gates

The carry skip adder is are implemented using reversible gates where it increases speed by garbage values instead using parallel prefix adder. Here the block of RCA and incrementation blocks are implemented with toffoli gates shown in figure 5. Thus the speed is achieved by reducing the

garbage values. The PPA is eliminated because the PPA consumes more area and power. In these reason all the blocks in CSKA replaced by toffoli logics. The carry skip adder is are implemented using reversible gates where it increases speed by garbage values instead using parallel prefix adder..The figure 6 shows the full adder design using toffoli gates. Thus the speed is achieved by reducing the garbage values.

IV RESULTS AND DISCUSSION

The analysis of the high speed carry skip adder using xillinx ISE ,where it consist of number of macro cells used, registers, pinsand functional block inputs.

TABLE-1: Utilisation table

	Area	Delay	Pin used	Pterm used	Power
Existing	27	3.5	39	54	24
Proposed	20	3.5	37	59	23

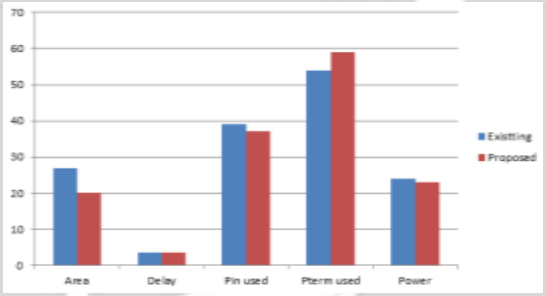


Chart-1: Utilization summary

The device utilization summary shown in figure 6 and it consists of pin used, area, pterm used, power and delay.

V CONCLUSION AND FUTURE ENHANCEMENT

A FPGA architecture is presented for computing addition. The architecture is based on the application of arithmetic. This paper presents the primitive reversible gates such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple-valued reversible gates having similar properties. Then the complexity is reduced by use of reversible gates .The increase in high speed, power area and delay is obtained by comparing the existing and the proposed system.

FUTURE ENHANCEMENT

In our project the implementation of 8 ,16 and 32 bit of existing and proposed structure is used. The proposed architecture convert into 128 bits adder to analyse power,area and delay.

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