IMPLEMENTATION AND DESIGN OF BCD ADDER USING QUBIT GATES FOR QUANTUM APPLICATIONS

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ABSTRACT

*Reversible Logic is an emerging technology, it has hellocious applications in various fields. Reversible logic implementation reduces loss of entropy because of bit manipulations. In this work we present a novel design of reversible 2 DIGIT BCD ADDER using INTEGRATED QUBIT GATES. The reversible BCD adder is designed from 2*2 control V, Control V+, CNOT, MTSG,FREDKIN,FEYMAN ,INTEGRATED QUBIT GATES .The design of proposed reversible adder- requires minimum quantum cost ,delay by maintaining ancilla inputs and garbage outputs.*

Keyword *Reversible Logic, Integrated QUBIT GATES, Ancilla, Garbage, Control v, Control v+*

1. Introduction

Reversible Logic is an emerging technology; it has hellocious applications in various fields, such as Nano computing, DNA Computing QCA (Quantum Cellular Automata), Optical Computing etc.., Limitations of CMOS in Deep sub Micron Regime Leads to failure of Moore‟s law, leads to development of Reversible circuits. These are more immune to Information loss, this Information loss is in the form of energy dissipated for every bit change. Reversibility concept is an idea from Launder, there is a minimum amount of energy required to change one bit of information, known as the Landauer‟s limit kT ln2 (0.69315).At25 °C, energy loss for one bit change is 0.0178 ev .Bennett showed that loss is negligible if we implement reversible logic. So the primary goal of reversible computing is to minimize energy loss in computing devices and promote speed and density. We present VHDL representation in this paper. In section II we represents Basic terminology of reversible logic and basic gates in Reversible logic in Section III we present Creating VHDL Library .In section IV we represent Proposed Work using Prior Works , In section V conclusion

II. Terminology and Gates

Reversible Function: The multiple output Boolean function G(x1; x2; xn) of n Boolean variables is called reversible if: The number of inputs is equal to the number of outputs, any output pattern has an only one input representation.

Basic Gates in reversible logic

The reversible gates used in this work are NOT gate, CNOT gate, Toffoli gate and Peres gate Each reversible gate has the quantum cost and the delay associated with it. The NOT gate and the CNOT gate have the quantum cost of 1 and delay of 1 Δ; Control V control V + are the basic gates ,by using these gates many gates using reversible logic were designed to meet the requirement ,This work uses gates like peres gate, Toffoli gate, Fredkin gate and MTSG gate.

Feynman gate:

This gate uses one CNOT Gate with quantum cost 1, Details of CNOT gate and Quantum Representation in fig2

Control V and Control V+:
The controlled-V gate is shown in Fig. 3 In the controlled-V gate, when the control input A=0 then the qubit B will pass through the controlled part unchanged, i.e., Q=B. When A=1 then the unitary operation V

$V=\frac{i+1}{2}\begin{bmatrix}1 & -i\\ -i & 1\end{bmatrix}$ is applied to the input B, i.e., Q=V (B). The controlled-V + gate is shown in Fig4. In the controlled-V + gate when the control input A =0 then the qubit B will pass through the controlled part unchanged, i.e., we will have Q=B. When A=1 then the unitary operation $V^{+} = V^{-1}$ is applied to the input B, i.e., Q=V +(B).The V and V + quantum gates have the following properties:

Toffoli Gate [TG]:
Quantum representation of Toffoli gates uses 5 basic gates so its quantum cost is 5.Quantum Representation of Toffoli Gate in Fig 5

Peres Gate [PG]:
Quantum representation of Peres gates uses 4 basic gates so its quantum cost is 4.Quantum Representation is as shown in Fig 6.By providing a constant input i.e. c=0,This Gate acts as **Half adder.**

Integrates Qubit Gates:
These are two bit quantum gates allow minimized construction of locally reversible logic structures.

Fredkin Gate using IQ Gates [FG]:
By using IQ Representation for Fredkin Gate Reduces quantum cost to 5.Quantum Representation of Fredkin gate is in Fig7

MTSG Gate:
MTSG Gate is modified TG Gate. It is 4*4 GATE, by proving a constant input to i.e. D=0, the above gate acts as Full Adder in classical logic. Quantum Representation of MTSG gate in fig 8 MTSG gate is obtained by cascading two peres GATES

Creation of Qubit Library:
For the effective representation of reversible logic structures using reversible logic using integrated qubit gates is achieved by creation of library called "QUBIT".By using VHDL-93

Steps in Creating Qubit Library:
Basic Unit in Quantum Computation is QUBIT ,Spins of Qubit is represented in Blosch Sphere Has Multiple states includes 0,1,v,V,p,P,U.Where p,P,V,v are outputs from Control V+, control V gates respectively.

Table I: Integrated Qubit Gates Spin Operation LOOK UP TABLE

Qubit	Description
0	Logic „0"
1	Logic „1"
v	V transformation with „0"input
V	V transformation with „1"input
p	V+ transformation with „0"input
P	V +transformation with „1"input
U	Qubit is in an Unknown State

Fig: 1 Quantum Representation of QNOT.

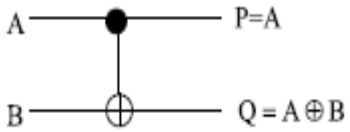


Fig: 2 Quantum Representation of Feynman Gate

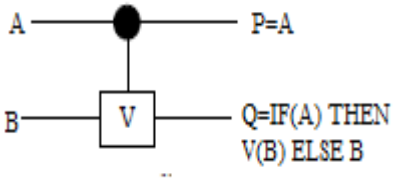


Fig: 3 Quantum Representation of Control v

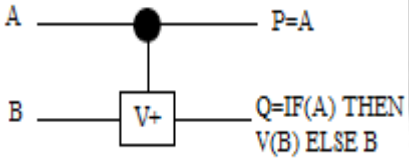


Fig: 4 Quantum representation of control V+

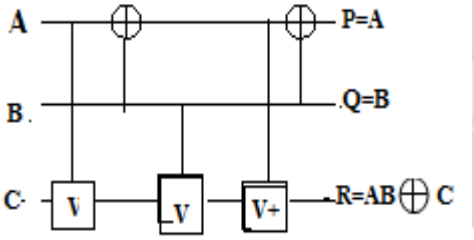


Fig: 5 Quantum Representation of Toffoli Gate

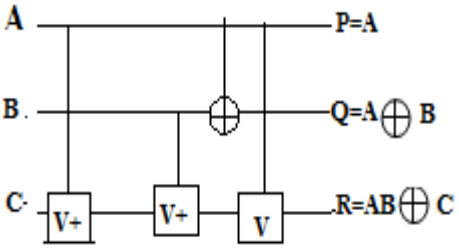
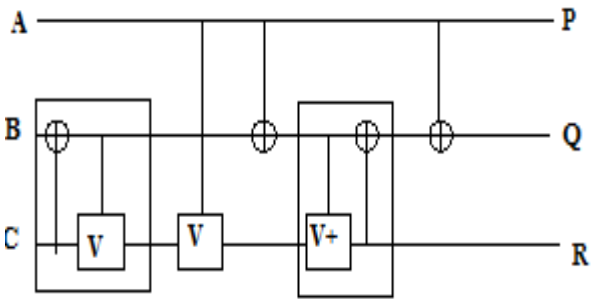
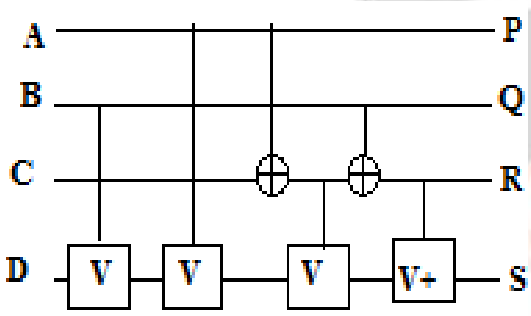


Fig: 6 Quantum Representation Of Peres Gate



P=A,Q= ⊕AC,R= C⊕AB
Fig: 7 Quantum representation of Fredkin Gate using IQ Gates;



P=A, Q=A⊕B, R=A⊕B⊕C,S= (A⊕B) C⊕AB⊕D
Fig: 8 Quantum Representation of MTSG Gate

Binary Addition:
BCD numbers are represented in 4 bit format, Inputs to the binary adder are in range of 0-9, and 4bit binary addition in reversible phenomenon can be done by using reversible parallel adder using 4 MTSG gates .By providing 1 constant input to MTSG .MTSG Gate Operates like a full adder along with 2 garbage outputs

Overflow Detector:
The maximum range is 1111 for a 4 bit ranged Binary Numbers i.e. 15 in Decimal format, so the numbers from 10 to 15 are not valid BCD numbers and they can detected by using a4 where X1,X2,X3 outputs of parallel adder .and a4 is its carry .If OF ="1"indicates that numbers are not in range of BCD ,So number „6" is added to sum from TG gate.TG Gate is used to get overflow output by FG gate Another FG is used to restore modified outputs

Overflow Removal Circuit: This uses Peres, Fredkin, MTSG gates for processing it takes control input from detection circuit

BCD ADDER:
The design of reversible BCD adder, the primary concern is to keep the number gates and number of garbage outputs as minimum as possible. As the number of gates is reduced, therefore delay will also be reduced. Garbage output is another important criterion. Circuits with less number of garbage outputs are always desirable. By using above 3 steps 1 Digit BCD Adder is designed. In Fig 9 Decimal addition using reversible logic is represented

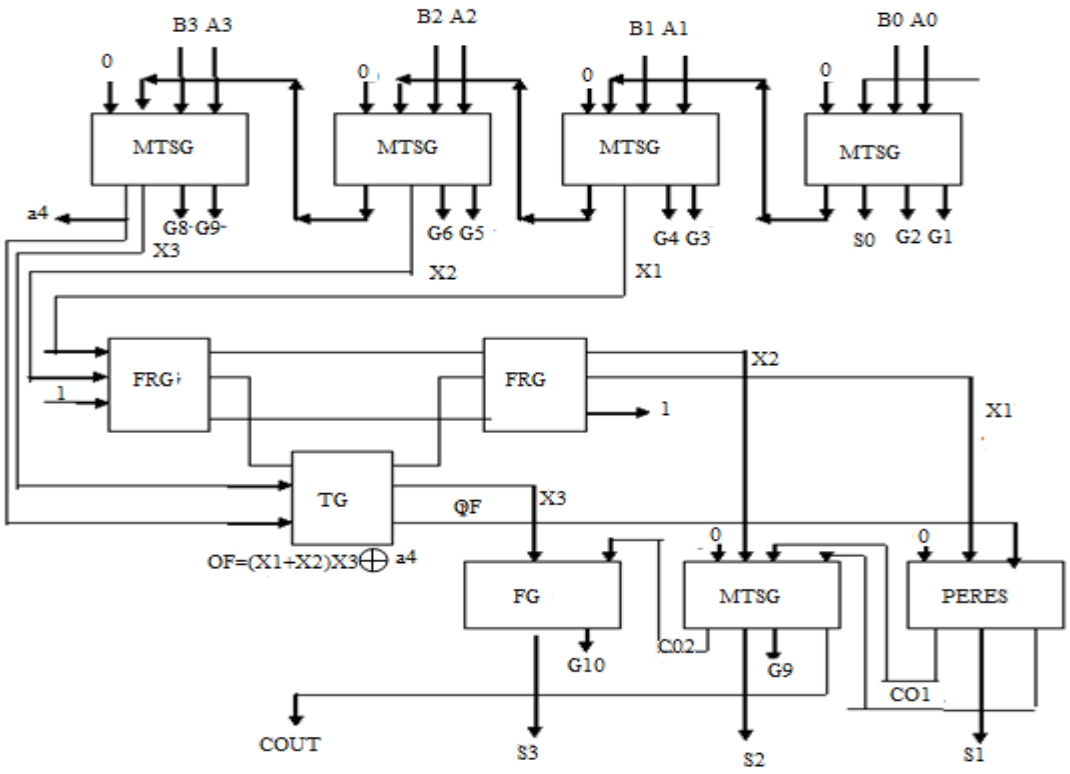


Fig: 9 Digit BCD ADDER

PROPOSED 2 DIGIT BCD ADDER

By using two BCD adders we can design two digits BCD added. We have to take two 8 bits as input and by giving 4 LSB of two inputs to 1 digit BCD Adder, this circuit produce BCD SUM, carry, by giving carry to i/p of next 1 digit bcd adder along with 1st four MSB to this we will get resultant BCD SUM., By combining outputs of 2, 1 bit BDC adders we will get 2 digit BCD adder Output.

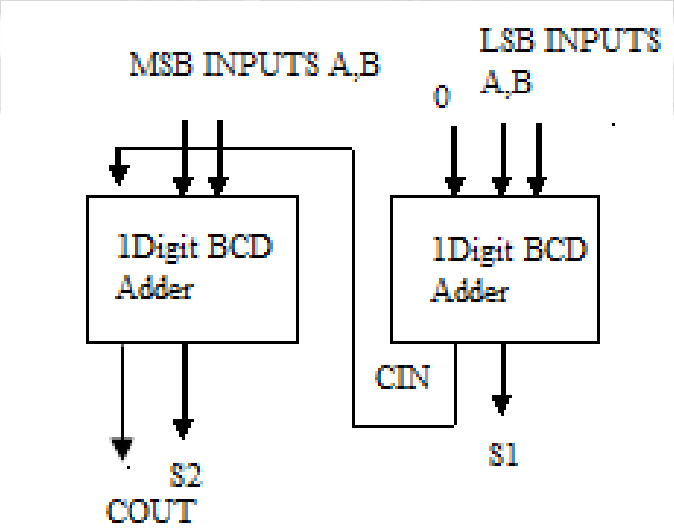


Fig 10: 2 DIGIT BCD ADDER

Simulation Results of Logic Structures:

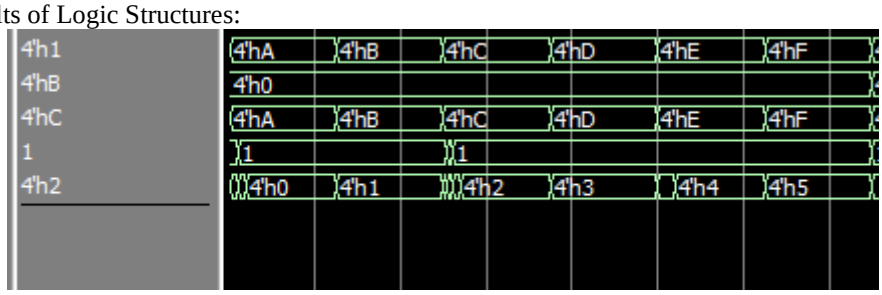


Fig: 11 Digit BCD ADDER

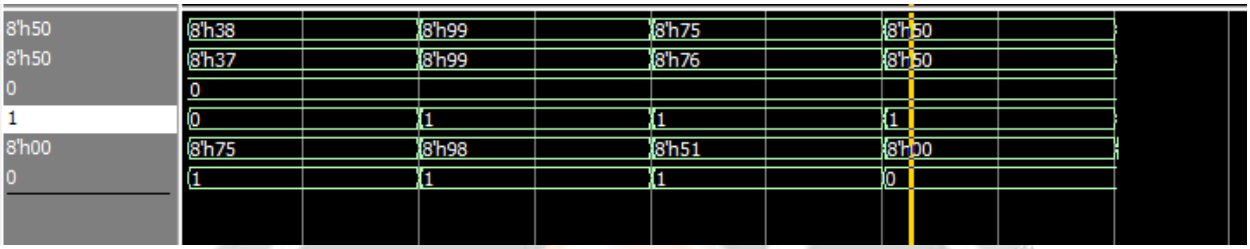


Fig: 12 Digit BCD ADDER

CONCLUSION

In this Paper we propose 2 Digit BCD Adder using Integrated Qubit Gates is designed. This circuit has less quantum cost than classical logic and reversible gates. The Functionality of above circuit is verified by using Modelsim 10.1 We can design m bit compact, fast adders for quantum applications in future.

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