INTERLEAVED BUCK CONVERTER USING MPPT ALGORITHM

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ABSTRACT

In this project proposes a simple and efficient interleaved buck converter (IBC) which was having low switching losses and improved step-down conversion ratio was proposed, IBC is suitable for photovoltaic battery charging application where the input voltage is high. It is similar to the conventional IBC, but in proposed IBC the two active switches are connected in series. The proposed IBC shows that the voltage stress across all the active switches is half of the input voltage before turn-on or after turnoff when the operating duty is below 50%.The capacitor charging and discharging depends upon the turn on and turn off operation of the switches and switching losses can be reduced considerably. This allows the proposed IBC to have higher efficiency and operate with higher switching frequency. By operating with the higher switching frequency, the proposed IBC has a higher step-down conversion ratio and a smaller output current ripple compared with a conventional IBC. The feasibility of the proposed topology is experimentally verified for a output current of a 20A max.

Keywords: Interleaved Buck Converter (IBC), Photovoltaic Battery, Higher Step-Down Conversion Ratio

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1. INTRODUCTION

In PV system power energy is most useful for the upcoming days. So this paper mainly concentrates on the PV battery storage applications. And also the interleaved operation of buck converter that was used to reduce the high current ripple content in the output current, high step down conversion ratio. MPPT algorithm is used to obtain the higher efficiency.

The key principle that drives the buck converter is the tendency to store electrical energy and delivers electrical energy based upon the construction and triggering pulses. In a buck converter the output voltage is always lower than the input voltage. The parallel operation of two buck converter is called interleaved buck converter that reduces the losses at the time of switch ON and OFF. Maximum power point is the operating point at which the power

dissipated in the resistive load is maximum, i.e., the maximum power extracted from the photovoltaic cell. The load remaining constant and fixed, varying the duty cycle of the converter, the effective load resistance appearing at the output of the solar array (or the input of the converter) is varied, thus changing the slope and shifting the operating point of the solar cell to its MPP. MPPT controllers with algorithms such as mountain-climb algorithm are used to track the maximum power output and maintain the duty cycle at that particular voltage corresponding to MPP. Here the voltage is kept nearly constant as the load requires rated voltage from the source. The perturb and observe algorithm is used to draw a maximum power from the PV systems.

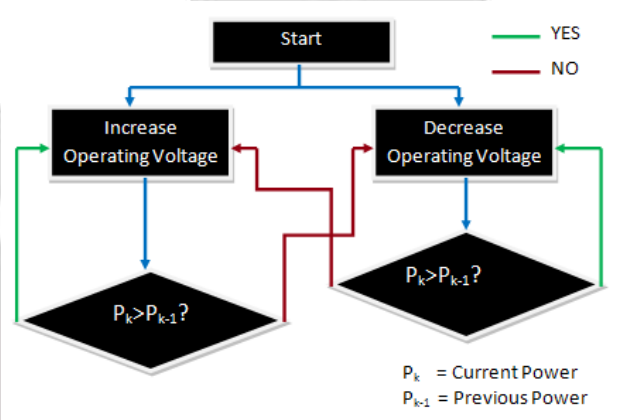

Fig 1: Perturb and Observe Algorithm

2. BLOCK DIAGRAM

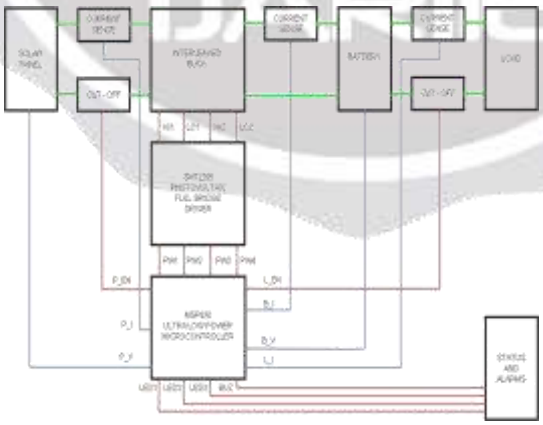

Fig 2: Interleaved buck converter using MPPT by PWM switching

In this proposed methodology mainly concentrates on the battery charging application and also maintain the life of the storage battery a long. This block diagram consists of interleaved buck converter, alarm circuit, battery for the storage purpose and the micro-

controller (MSP430F5132) that is used to control the pulse width time period of the power MOSFET through the driver circuit.

The input dc voltage to the interleaved buck converter is fed from the solar PV panel or array. In between the interleaved buck converter and the solar array there is current sense which one was used to measure the input current and the voltage to the interleaved buck converter. A interleaved buck converter produces the voltage less than the input voltage in it. Because it stores and delivers electrical energy based upon the switch ON an OFF time (pulse width) of the power MOSFET that in the interleaved buck converter by the way of driver circuit through microcontroller that has MPPT algorithm. This algorithm starts with measuring the PV power P at particular reference voltage as V. feedback loop which one was taken from the output side i.e, from the battery terminal that was compared with previous input current and voltage (reference voltage and current). If the present output power increased when compare with previous power so that the new power P is found at the higher voltage level. So this way p_{max} is obtained at the particular point that has the I_{max} and $V_{max.}$. All this control and mathematical calculation is done by the microcontroller that produces the error signal to the full bridge driver circuit which is used to drive and decides the pulse width time period of power MOSFET. In additionally driver consists of amplifier circuit that makes the amplified voltage (pulse width) suitable to drive the MOSFET above threshold voltage value. Only above the threshold voltage IBC turns ON condition i.e, the pulse width time period results increase in current. So the power is increased in such way to obtain maximum output from the interleaved buck converter that is stored in the battery. Battery provides supply to dc load.

3. SYSTEM DESIGN AND EFFICIENCY

The PMP7605 is developed around the MSP430F5132 controller IC. The design is targeted for small and medium power solar charger solutions. The present design is capable of operating with 12V/24V panels and 12V/24V batteries with up to 20A output current. However, it can be easily adapted to 48V systems by just changing the MOSFETs to 100V rated parts. Also, it is possible to increase the current to 40A by using TO-220 package version of the same MOSFETs used in the design. The design has an operating efficiency of above 97% at full load in a 24V system. For 12V systems the efficiency is above 96%. This efficiency figure includes the losses in battery reverse protection MOSFET and panel reverse flow protection MOSFET, which are part of the design. The high efficiency is the result of the low gate charge MOSFETs from TI used in the design, and the interleaved buck topology used. The interleaved buck topology reduces the component stresses by a great extent. Another feature is the relatively small sized components used, possible due to the high operating frequency. The design has built-in battery charge profiles for 12V and 24V Lead acid batteries. The circuit takes only under 10mA of standby current while operating from battery. There is also a provision to connect a load to the battery with overload and short circuit cut-off built in. The design presently uses ‘perturb and observe’ algorithm for MPP tracking.

4. HARDWARE CIRCUIT

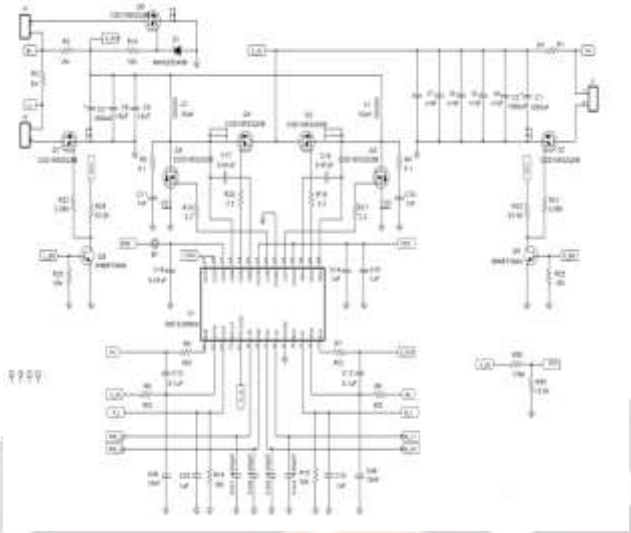

Fig 3: Hardware circuit

4.1 CIRCUIT EXPLANATION

In this circuit the combination of interleaved buck converter, driver circuit, microcontroller is connected. The interleaved buck converter consists of two single phase buck converter connected in parallel. The two PWM signal difference is 180 degree when each switch is controlled with the interleaving method. Because each inductor current magnitude is decreased according to one per phase, we can reduce the inductor size and inductance when the input current flows through two buck inductors. The input current ripple is decreased because the input current is the sum of each current is the sum of each current of inductor L1 and L2. With the required output from the controller the pulse is given to driver circuit and the ON and OFF operation is mode in the circuit as per the modes of the operation. As a main part, interleaved soft switching boost converter is explained below.

5. TEST DATA

5.1 12v SYSTEM PERFORMANCE

Table 1 show the 12v system performance, this system is used to charging the 12V battery storage. In this 12V system, the efficiency is above 96%.

Table 1: 12V System performance

Vi (V)	Ii (A)	Vo (V)	Io (A)	Pi (W)	Po (W)	Efficiency (%)
17.70	0.01	0.00	0.00	0.14	0.00	0.0
17.01	0.76	12.01	0.99	12.93	11.93	92.3
17.16	2.19	12.05	3.00	37.58	36.17	96.2
17.27	3.61	12.09	5.00	62.34	60.46	97.0

17.52	5.40	12.15	7.57	94.61	91.98	97.2
17.42	7.20	12.20	10.00	125.42	122.03	97.3
17.33	11.00	12.32	15.00	190.63	184.79	96.9
17.19	15.06	12.44	20.00	258.88	248.70	96.1

5.2 12V SYSTEM EFFICIENCY GRAPH

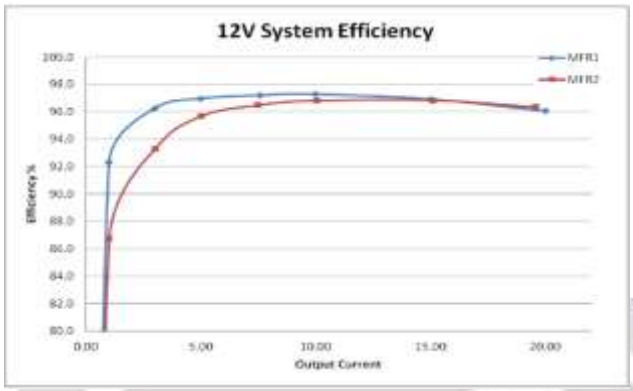

Fig 4: 12V Efficiency graph

6. OUTPUT WAVEFORMS

Switching Node Waveforms

12V System, 20A Load. Individual channel switch nodes show interleaved operation.

7. CONCLUSION

IBC is proposed in this project. The main advantage is that voltage stress across the switching is less. The cost is low, high step-down conversion ration when the input voltage is high. And higher current output with low ripple. Output power efficiency is above the 95% is achieved.

8. FERENCE

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