# Implementation Of 12V To 330V Boost Converter With Closed Loop Control Using Push Pull Topology

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**ABSTRACT**

*There is a growing need to reduce the size and weight of DC power supplies and at the same time improve power supply efficiency, be it in the areas of electronic power adapters or inverters. This paper presents a push pull topology of boost converter based on switched mode power supply. The converter utilizes an existing DC power supply capable of delivering 12V or a lead-acid battery of 12V as power input and transforms it to 330V dc. This kind of output voltage can be processed by inverter switches into an alternating AC signal. SG3525 pulse width modulator circuit controls the duty cycle of the MOSFET switches and implements closd loop control which reduces sensitivity of the system to parametric changes. The complete design is modeled using proteus software and the output verified practically.*

**Keyword**: *Push pull converter, pulse width modulator, inverter, SG3525, closed loop control*

## 1.0 INTRODUCTION

The push pull converter, a dc/dc transformer isolated converter, is a two forward converters derivative operating $180^{\circ}$ out of phase[9] [4] [6].

A push-pull converter operates as an interleaved forward converter and is ideal for higher power designs above 200W[6]. The push-pull converter has all the benefits of a forward converter while exhibiting lower input and output ripple currents compared to the forward, thus having smaller filter components. The push-pull converter can operate over the full duty cycle from zero to one.[5] [6]

Double-ended topologies, such as push-pull, half-bridge and full-bridge, allow higher efficiencies and greater power densities when compared with common single-ended topologies including flyback and forward converters[1][3].Therefore, double-ended topologies are increasingly popular in many applications, especially telecom and automotive.

## 2.0 PRINCIPLE OF OPERATION OF PUSH PULL CONVERTER

The basic topology of Push Pull converter is shown in figure1.The input DC voltage is switched through the center-tapped primary of the transformer by two switches, Q1 and Q2, during alternate half cycles. These switches create pulsating voltage at the transformer primary winding. The transformer used provides isolation between the input voltage source $V_{IN}$ and the output voltage $V_{OUT}$. The switches Q1 and Q2 are driven by the control circuit, such that both switches should create equal and opposite flux in the transformer core.

In the steady state of operation, when the switch Q1 is ON for the period of $T_{ON}$, the dot end of the windings become positive with respect to the non-dot end. The diode $D_5$ becomes reverse-biased and the diode $D_6$ becomes forward-biased. Thus, the diode $D_6$ provides the path to the output inductor current $I_L$ through the transformer secondary $N_{S2}$. As the input voltage $V_{IN}$ is applied to the transformer primary winding $N_{P1}$, a reflected primary voltage appears in the transformer secondary. difference of voltages between the transformer secondary and output voltage $V_{OUT}$ is applied to the inductor L in the forward direction.

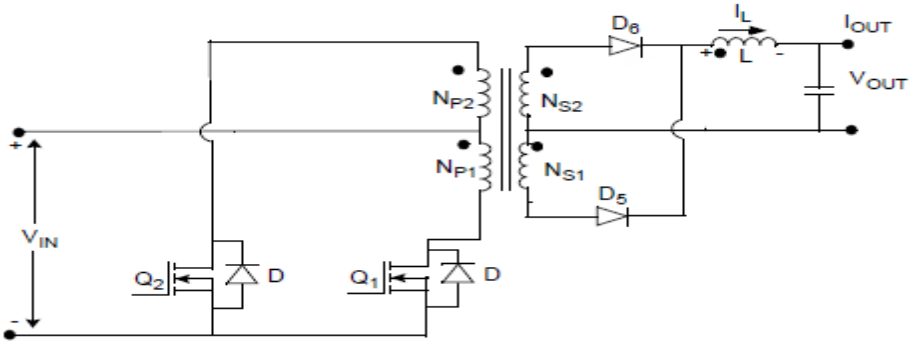


**Fig. 1**: Push Pull Converter Topology

The inductor current $I_L$ rises linearly from its initial to its peak value. During this TON period while the input voltage is applied across the transformer primary $N_{P1,}$ the value of the magnetic flux density in the core is changed from its initial value of $B_1$ to $B_2$, At the end of the $T_{ON}$ period, the switch $Q_1$ is turned OFF, and remains off for the rest of the switching period $T_S$. The switch $Q_2$ will be turned ON after half of the switching period $T_{S/2,}$ Thus, during the $T_{OFF}$ period, both of the switches ($Q_1$ and $Q_2$) are OFF. When switch $Q_1$ is turned OFF, the body diode of the switch provides the path for the leakage energy stored in the transformer primary, and the output rectifier diode $D_5$ becomes forward-biased. As the diode $D_5$ becomes forward-biased, it carries half of the inductor current through the transformer secondary $N_{S1,}$ and half of the inductor current is carried by the diode $D_6$ through the transformer secondary $N_{S2.}$ This results in equal and opposite voltages applied to the transformer secondaries, assuming both secondary windings $N_{S1}$ and $N_{S2}$ have an equal number of turns. Therefore, the net voltage applied across the secondary during the $T_{OFF}$ period is zero, which keeps the flux density in the transformer core constant to its final value B2. The output voltage $V_{OUT}$ is applied to the inductor L in the reverse direction when both switches are OFF. Thus, the inductor current $I_L$ decreases linearly from its initial value. Table 1 shows the push pull parameters and specifications

**Table 3**: Push Pull Converter Specifications

| **Parameter** | **value** |
|---|---|
| **Input voltage norminal** | 12V |
| **Input voltage Mininum** | 9V |
| **Input voltage maximum** | 14V |
| **Output voltage maximum** | 330V |
| **Output voltage minimum** | 283V |
| **Output power** | 100W |
| **Output current** | 1A |
| **Input current norminal** | 8A |
| **Switching frequency** | 50kHz |
| **Switch Duty Cycle** | 45% |

## 3.0 PUSH-PULL DESIGN CONSIDERATIONS

The converter is supplied by a low ESR capacitor C7 to lower the battery bus ripple current and the EMI of the converter input. The converter's MOSFETs Q5 and Q6 are controlled by SG3525 current mode controller.Because of the voltage source character of the converter, the rectifier has to be a current type, which is why smoothing chokes $L_1$ is used. Over voltage spikes across the rectifier diodes, due to the diodes reverse-recovery and transformer leakage, are clamped by RCD snubbers consisting of a $R_6$- $C_1$- $D_6$. $C_4$ Filters the output voltage. Figure 23 shows the circuit implementation

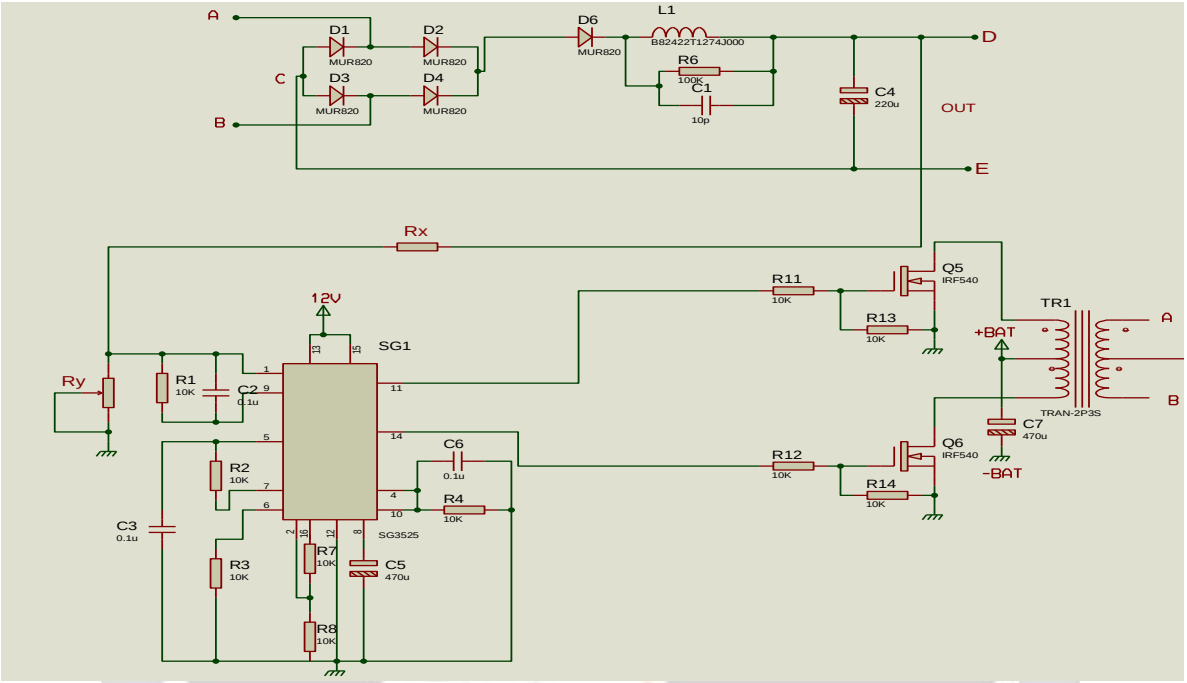


**Fig. 2:** Circuit Implementation of Push pull Converter Controlled By SG3525

## 3.1 PUSH PULL CONVERTER DESIGN PROCEDURE

### 3.1.1 Transformer

To come up with transformer design, the first task is to choose an appropriate transformer core. The core size can be selected Based on manufacturer power-handling-capability core tables. Subsequently, the maximum core flux density travel ΔB is determined from the core manufacturer data sheet, then the approximate number of turns can be calculated for both primary and secondary windings. Since the number of turns is usually an integer, the number is rounded and the real flux density travel is calculated. If ΔB is below a maximum limit with respect to the switching frequency (core material dependent), winding turns and the cross-sectional areas are calculated for all respective windings

For a 100W output power consideration, ETD44 core can be selected. The parameters specification is as follows:

Core factor $\Sigma = 0.589mm^{-1}$, Effective volume $V_e = 17800mm^3$

Effective lengthn $L_e = 103mm$, Effective area $A_e = 173mm^2$, Flux density travel = 400mT.

Using faradays law of electromagnetic induction, the amount of magnetic charge into the core is given by

$$V_i = \frac{d\psi}{dt} = N\frac{d\phi}{dt} = N.S\frac{dB}{dt} \quad (1)$$

Where

$V_i$ = induced voltage, $\psi$ =linkage flux in the core, N= number of turns, S= Core cross sectional area, B=flux density in the core,

Intergrating the induced voltage gives

$$\int V_i dt = N.S.\Delta B \quad (2)$$

Where $\Delta B$ is flux density travel. Since the induced voltage during the steady state operation of the converter is constant and equal to input voltage, the magnetic charge in the core is given by

$$\int V_i dt = V_{IN}.D_S.\mathrm{T} \quad (3)$$

Where $V_{IN}$ is input voltage norminal, $D_S$ is switching duty cycle, T is switching period

Therefore,
$\int V_i dt = 12\times 0.45 \times 2 \times 10^{-5} = 108\times 10^{-6}\mu V$
To calculate the number of primary turns, equation (2) is rearranged to give
$N_1 = \frac{\int V_i dt}{S.\Delta B} = \frac{108\times10^{-6}}{173\times10^{-6}\times0.4} \cong 2t$
For forward type converter, the turn ratio of primary to secondary winding is given by
$\frac{N_2}{N_1} = \frac{V_{out}}{V_{IN}\times D_s\, Max}$ (4)
where $D_s\, Max$ is the duty cycle defined at maximum value of 98%,
$V_{out}$ is the output voltage taken at the maximum value of 330V, $V_{IN}$ is the input voltage taken at a minimum value of 9V

Therefore
$\frac{N_2}{N_1} = \frac{330}{9\times0.98}$=37t
$N_2 = N_1 \times 37 = 2 \times 37 = 74t$

### 3.1.2 MOSFET Switch selection

The voltage rating of MOSFETs in the design of power converters is based on voltage spikes that can possibly occur during MOSFET switch-off. Of course it also depends on the drain current, switching frequency, the input voltage, load conditions, and transformer properties. For push-pull, a number of twice the input voltage is usually sufficient. IRF540 is a high speed switching N-channel MOSFET with $V_{DSS} = 100V$, $R_{DS(ON)} = 77m\Omega$, $I_D = 30A$. It is a choice in this design.

### 3.1.3 Rectifier diode selection

Rated diode voltage is given by the voltage waveform applied to the diode. As the rectifier is current-loaded there is no natural clamp for over voltage spikes at the instant of a diode reverse recovery. That is why a suitable snubber has to be implemented in order to cut-off the excess energy that could possibly overheat the diode chip by internal avalanche. An ultra fast diode STTH10LCD06 is used with current rating of 10A, reverse voltage of 600V, and 100ns reverse recovery time. This diode is good enough for 50kHz switching frequency.

### 3.1.4 Filter chokes

A basic design consideration when implementing a filter choke is to look at the rectified current ripple.
For an output current level in the range of 1A, the relative ripple $r_i$ can be considered in the range of 50 to 20%. Let $r_i$ equal 30% for nominal conditions. Then the filter choke inductance value is given by
$L = V_L.\frac{\Delta T}{\Delta i} = \left(V_{IN}.\frac{N_2}{N_1} - V_{OUT}\right) \times \frac{D_{SMax}.T}{r_i.I_{OUT}}$ (5)
where
$V_L$ = voltage across the choke during active cycle
$\Delta T$ =the time during active cycle
$\Delta i$ =current ripple
$V_{IN}$ =norminal input voltage
$\frac{N_2}{N_1}$ =transformer primary to secondary turn ratio
$V_{OUT}$ =norminal output voltage
$D_{SMax}$ =maximum switching duty cycle
$r_i$ =relative current ripple
$I_{OUT}$ =norminal output current
$L = \left(12 \times \frac{74}{2} - 325\right) \times \frac{0.98\times2\times10^{-5}}{0.3\times1}$ =7.7mH. Therefore a choke of 7.7mH inductance is wounded on a ferrite bead.

### 3.1.5 Push pull control

The control of the output voltage of the converter is made possible by implementing a PWM control scheme that switches the power MOSFETs ON and OFF at a desired frequency and changes the duty cycle of the control signal based on the preset conditions. SG3525 pulse width modulator control circuit is implemented to achieve PWM control.

### 3.1.6 Frequency setting

Frequency of operation of SG3525 can be set by first chosing the value of the timing capacity and resistor $C_T$ and $R_T$.
From the $C_T$ , $R_T$ and $R_D$ curve of SG3525, the recommended value for $C_T$ is (1nf-0.2µf), $R_T$ is (2K-150K), $R_D$ is (10Ω-47Ω) $C_{SS}$ is (1µf$-22\mu f$). The switching frequency is given by

$$F = \frac{1}{C_T(0.7R_T+3R_D)} \quad (6)$$

$C_T = 2nf$, $R_T = 14k\Omega$, $R_D = 10\Omega$. Therefore

$$F = \frac{1}{2\times10^{-9}(0.7\times14\times10^3+3\times10)} \cong 50kHz$$

### 3.1.8 Output voltage control

The internal voltage reference of SG3525 is
$V_{ref}$ =5.1V $\pm$1% on pin 16
$V_{ref}$ on pin 2 (non inverting terminal of the error amplifier) equals
$5.1V \times \frac{R8}{R8+R7} = 5.1\times\frac{10}{10+10}$ =2.55V, therefore $V_{ref}$ on pin 2 is 2.55V
This voltage needs to be compared with the voltage on the inverting terminal of the error amplifier. This is done by using a voltage divider to feedback the output voltage of the push-pull to pin 1 of SG3525. When voltage on the inverting pin (pin1) is greater than voltage on the non inverting pin (pin2), duty cycle is decreased, similarly, when voltage on the non inverting pin (pin2) is greater than voltage on the inverting pin (pin1), duty cycle is increased.
Therefore,

$$V_{ref} = V_{OUT}.\frac{R_Y}{R_Y+R_X} \quad (44)$$

$R_X = 10K\Omega$ , $V_{ref}$ =2.55V(voltage on pin1), $V_{OUT}$ =330V(Nornimal DC buck voltage at the converter output)

$$\Rightarrow \quad 2.55V = 330V \times \frac{R_Y}{R_Y+10k\Omega} \Rightarrow R_Y = 79\Omega$$

## 4.0 RESULTS AND DISCUSSION

The circuit was constructed and tested using digital storage oscilloscope and voltmeter to observe the gating signal as shown in figure 3 and output voltage of the converter as shown in figure 4.

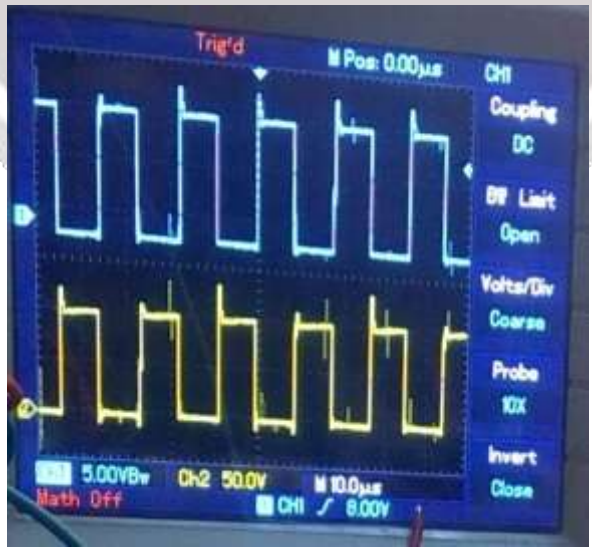


**Fig. 3:** Complementary Gating Signals Generated By Sg3525

The SG3525 produced a two complementary gating signals that switches the two MOSFET 180° out of phase.

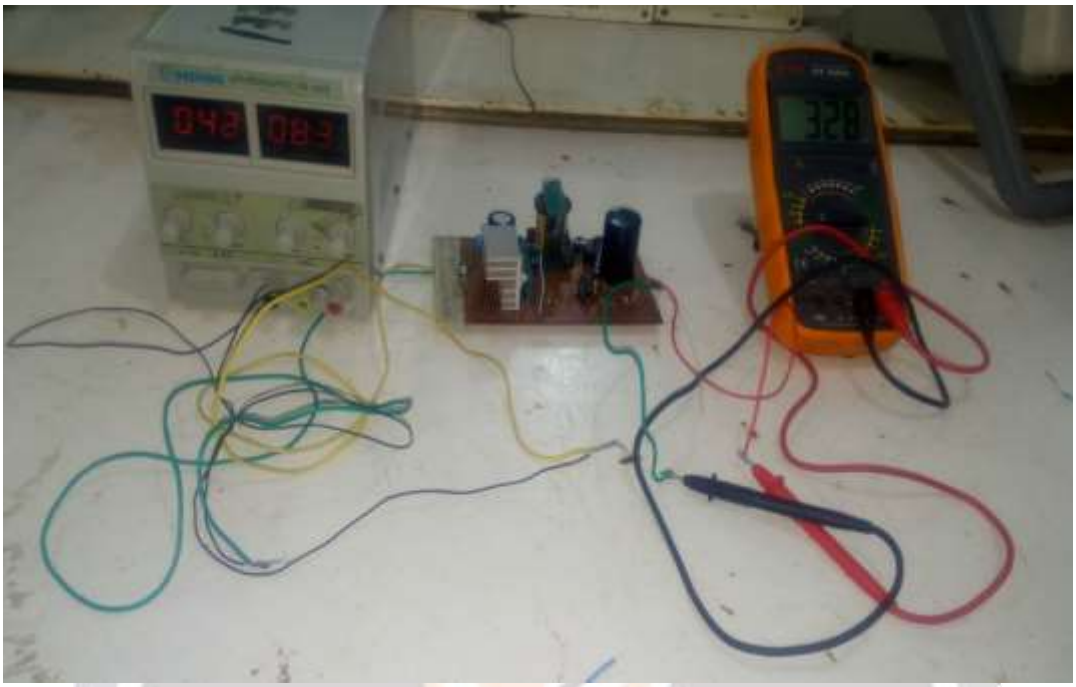


**Fig. 4:** Complete Circuit Prototype Showing DC Voltage Input And Output

The circuit however responded with the minimum input of 8.3Vdc when tested with variable DC voltage supply. The output voltage was seen to be 328V.

## 5.0 CONCLUSION

There are many topologies that can be used to achieve DC to DC voltage convertion. Push pull converter topology is used in this research due to its simplicity and the ability to scale out high throughput. From the results generated, it is possible to achieve higher voltage when the transformer turn ratio is increased.

## 6.0 REFERENCES

[1] A. Emadi, S. S. Williamson, and A. Khaligh, "Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems," IEEE Trans. Power Electron., vol. 21, no. 3, pp. 567–577, May. 2006.

[2] A. Khaligh and Z. Li, "Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art", IEEE Trans. on Vehicular Technology, vol. 59, no. 6, pp. 2806- 2814, Oct. 2009.

[3] Bob Bell (2006), "Half-bridge topology finds applications in high density power converters. Available at http://www.embedded.com/print/4012073, accessed on 09 May, 2017.

[4] Mousumbiswal, Sidharthsabyasach "A Study on Recent DC-DC Converters" International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 2, Issue 6 Nov 2012.

[5] PanXuewei A. , "naturally clamped zero current commuted soft-switching current –fed Push pull DC/DC converter:analysis, Design, Experimental Results", IEEE Trans.Power Electronics, 0885- 8993 2013.

[6] PanXuewei, Akshay K Rathore, "Current-fed Soft-Switching Push-pull Front-end Converter Based Bidirectional Inverter for Residential Photovoltaic Power System", 10.1109/TPEL.2014.2301495, IEEE Transactions on Power Electronics

[7] STMicroelectronics (2000). Regulating Pulse Width Modulators. SG3525A Data Sheet and Application note. Available at http://st.com/.../en/datasheet/sg3525.pdf, accessed on 15 June, 2017

[8] Swaminathan, B ‘‘A novel resonant transition push-pull dc - dc converter’’ Journal of the indian institute of science Vol 84, No 6 Nov-Dec 2004

[9] Thomas J. (ND). "Push Pull converter". Available at www.powerelectronicsconsultant.com/push-pull-converter.html, accessed on 25 June, 2017