Implementation of Optimized Low Power and Area Efficient MAC Unit for FIR Filter

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ABSTRACT

The Direct Form FIR filter is used for DSP application where the filter order is fixed. Generally this filter consumes more area and power. To overcome this problem Multiplier Control Signal Decision window (MCSD) schemes is incorporated into Direct Form FIR filter to dynamically change the filter order. MCSD structures consists of Control signal Generator (CG) and Amplitude Detection (AD) logic circuits. AD logic is used to revoke the right multiplication process and monitor the amplitudes of input samples. CG is used to control the filter operation through internal counter. Conventional reconfigurable FIR filter is designed using Vedic Multiplier that consumes more area and delay. In this paper, modified reconfigurable FIR filer is designed to further reduce the APT (Area, Power and Timing) product. The proposed Reconfigurable FIR filer, Vedic Multiplier is replaced by Russian Peasant Multiplication technique. Hence modified Reconfigurable FIR filter with Russian Peasant Multiplier consumes less area, delay and power than all compared methods

Keyword: *Reconfigurable FIR Filter, Multiplier Control Signal Decision Window (MCSD), Russian Peasant Multiplier.*

1. INTRODUCTION

The unstable growth in portable multimedia and mobile computing applications has enlarged the demand for low power Digital Signal Processing (DSP) systems and Wireless Communication. One of the most extensively used functions executed in DSP is Finite Impulse Response (FIR) filtering. In several applications, in order to attain high spectral suppression and noise reduction, FIR filters with moderately huge number of taps are essential. A lot of prior efforts for decreasing power consumption of FIR filter usually focus on the miniaturization of the filter coefficients whereas maintaining a fixed filter order . FIR filter structures are simplified to minimizing the number of additions/subtractions and add & shift operations. Though, one of the problems encountered is that one time the filter architecture is determined, the coefficients cannot be altered, and consequently, those are not appropriate to FIR filter with programmable coefficients. Fairly accurate signal processing systems are also used for the design of low power digital filters. In FIR filter order vigorously varies along with the stop band energy of the input signal. But the approach affects from slow filter-order adaptation time because of energy calculations in the feedback method.

Conventional methods in illustrate that sorting both the filter coefficients and data samples prior to the convolution operation have a desirable energy-quality feature of FIR filter. On the other hand, the overhead linked with the real-time sorting of incoming models is too huge. Reconfigurable FIR filter structural designs are previously projected for low power applications or to understand several frequency reactions using a particular filter. On behalf of low power structural designs, filter taps and variable input word-length different coefficient word lengths & dynamic reduced signal demonstration methods are used. In Multiplier Control Signal Decision window (MCSD) technique incorporated into reconfigurable FIR filter for low power or high speed applications. This approach is mainly used to dynamically change the filter order. But area and delay is more. In Pipelined booth multiplier is replaced to trade off the filter performance for dynamic power utilization. In booth multiplier is replaced by Vedic multiplier in reconfigurable FIR filter for low power and high speed process. In this paper, the Reconfigurable FIR filter is modified by novel Russian Peasant Multiplier, instead of Vedic Multiplier to optimize the area, delay and power utilization.

Chapter 2 deals with the basic development of FIR filter and existing method. Chapter 3 deals with the Design and Development of Reconfigurable FIR Filter and its architecture. Chapter 4 deals with the proposed

method and its advanced method and their Implementation. Chapter 5 deals with the result of proposed method and comparison with existing method. Chapter 6 deals with Conclusion and Future scope of our project work in details.

2. EXISTING METHOD

2.1 Conventional Vedic Multiplier

Vedic multiplier can be designed using different algorithm. The existing paper used Urdhva – Tiryakbhyam algorithm to design the Vedic multiplier. Urdhva – Tiryakbhyam is the common formula applicable to all cases of multiplication and also in the division of a huge number by another huge number. It means perpendicularly and diagonally. Conventional 16-bit Vedic Multiplier consists of four 8X8 Vedic Multiplier units and three 16 bit Ripple carry adders a. This Vedic Multiplier is incorporated into reconfigurable Finite Impulse Response (FIR) filter instead of regular multiplier. Vedic multiplier is used to perform the multiplication operation between input signal and coefficient. Conventional Vedic multiplier consumes less area and delay compared to regular multiplier. Further to reduce the area and delay Russian Peasant Multiplier is introduced. Controls signal Generator circuits are used to turn off the multiplier to reduce the switching activity.

3. PROPOSED SYSTEM

3.1 Reconfigurable FIR filter

Fig-1 shows architecture of Reconfigurable FIR filter. This structure consists of Amplitude Detection (AD), Control signal Generator, delay unit through OR gate, Multiplier unit and Adder unit. The amplitude of the input signal is monitored by AD and also removes the right multiplication process. As the absolute value of x(n) is slighter than the threshold , the output of AD is locate to logic 1. Amplitude Detection design is dependent on the input threshold, where the fan-in‘s of AND and OR gate are determined by a easy comparator circuit. In the reconfigurable filter, if we turn off the multiplier by allowing each of the input amplitude and the amplitude of input varies suddenly for every cycle, the multiplier will switch on and off continually, which shows considerable switching actions. Multiplier control signal decision window (MCSD) in dotted line of is used to explain the switching trouble. Using ctrl signal generator within MCSD, the number of input samples successively smaller than threshold are counted and multipliers are switched off only when consecutive input samples are lesser than threshold.

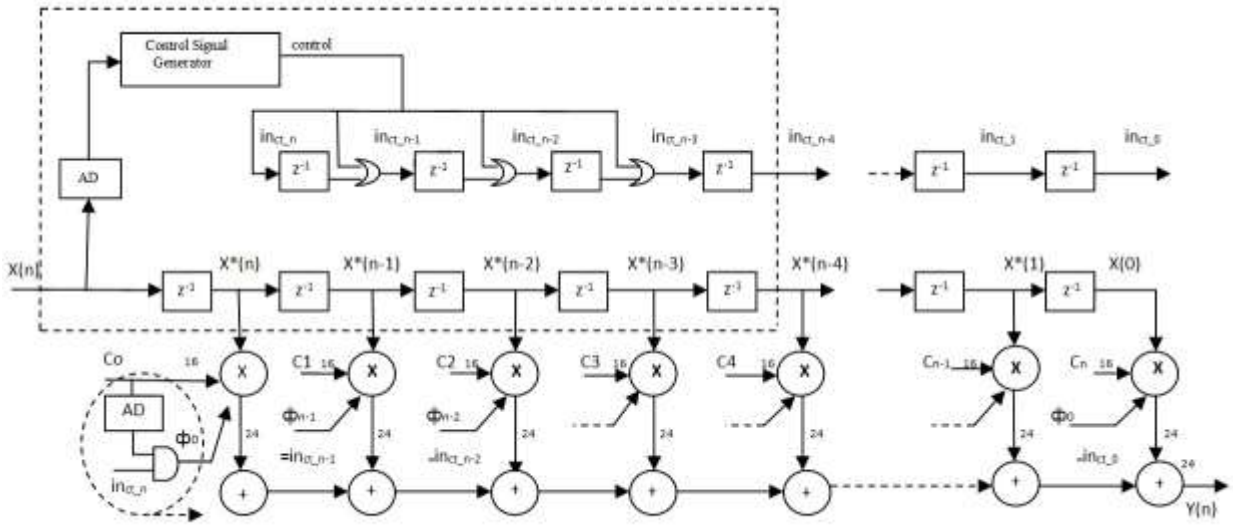

Fig-1: Reconfigurable FIR filter Architecture

When an input lesser than threshold comes in and AD output is located to logic 1, the counter counts lower to higher manner. As the counter reaches, the control signal in the figure modifies to logic 1, which specifies that successive small inputs are checked and the multipliers are prepared to switch off. One extra bit, in Fig-2 as dotted rectangle shape, is added and it is controlled by ctrl signal generator. Control signal generator is used to control the counter operation Multiplier is used to multiply the input signal and coefficient. Conventional Reconfigurable FIR filter is designed using Russian Peasant Multiplier. For a causal discrete-time FIR filter of order N, each value of the output sequence is a weighted sum of the most recent input values:

$$y[n] = C_0\, x[n] + C_1\, x[n-1] + C_2\, x[n-2] + \ldots + C_N\, x[n-N]$$
$$= \sum_{i=0}^{N} C_i\, x[n-i] \qquad (1)$$

where, x[n] is the input signal, y[n] is the output signal, N is the filter order, an N_{th}- order filter has (N+1) terms on the right-hand side and C_i is the value of the impulse response at the i_{th} instant for $0 \leq i \leq N$ of an N_{th} order FIR filter. If the filter is a direct form FIR filter then C_i is also a coefficient of the filter.

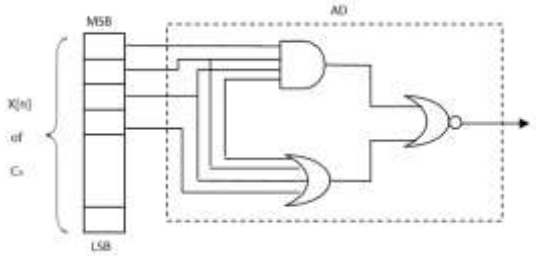

Fig-2: Block diagram of Amplitude Detector Logic Circuit

3.2 Russian Peasant Multiplier

The novel Russian Peasant Multiplier proposed earlier is slightly changed and modified. The modified Russian Peasant Multiplier is shown in Fig-3.

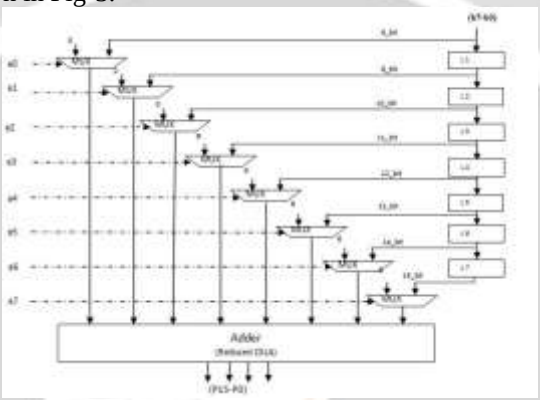

Fig-3: Architecture of Russian Peasant Multiplier

In conventional Russian Peasant Multiplier, two Shifters namely, left shifter and right shifter, 2:1 Multiplexers and adder units are used to perform the multiplication operation effectively. In this, Least Significant Bit (LSB) of Right Shifter is used for selection signal of corresponding multiplexers. This operation indicates passing multiplicand value to multiplexer in each stage. Therefore, in modified Russian Peasant Multiplier, the right shifter units are completely eliminated. This modified Russian Peasant Multiplier offers slight reduction in area and delay when compared to the normal Russian Peasant Multiplier.

3.3 CSLA using reduced CG block

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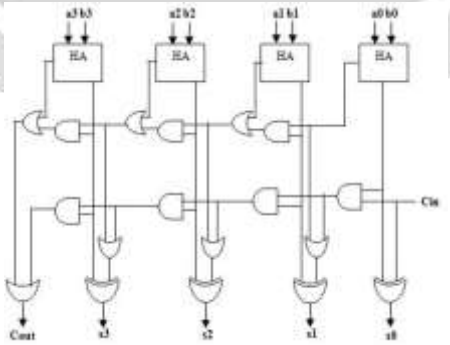

Fig-4: Architecture of Reduced CSLA

The modification is made on carry generation block of conventional CSLA. Because of two carry generation block conventional CSLA consumes more time to perform addition process. In order to reduce the time required to implement the carry generation block as well as addition process, CSLA using reduced CG block is

proposed. The CSLA using reduced CG block is shown in Fig-4. In Fig-4, only three AND gates and three OR gates used to generate the carry output where as in conventional CSLA, more number of AND gates and OR gates are used. When compared to conventional CSLA and CSLA using Sklansky Adder, the proposed CSLA using reduced CG block consumes less area and delay to perform addition process. This proposed CSLA using reduced CG block is further incorporated into Russian Peasant Multiplier for reducing area and delay for multiplication process.

4. DESIGN CONSIDERATIONS OF THE RECONFIGURABLE FIR FILTER

4.1 Design Consideration

In following discussions, as a metric of power savings, we use the power consumption ratio, which means the ratio of the reconfigurable filter power consumption to the conventional filter power. As a measure of filter performance degradation, we use Mean-Square Error (MSE) between the proposed reconfigurable filter output and original filter output. The most important factors that have a large effect on the proposed filter performance and power consumption are x_{th} and C_{th} . When x_{th} and C_{th} are set too large, it can give rise to large power savings with considerable distortion in the filter output. On the other hand, if x_{th} and C_{th} are too small, power savings become trivial. The other one to be considered is the length of MCSD.

The number of input samples whose m (x axis) consecutive input values are smaller than input threshold. The input signals used in the simulation are more than ten samples of sounds and speeches. If we choose a specific m value in the axis, the total number of canceled multiplications is the accumulated number of samples from the selected value to the right. Therefore, m if becomes larger, the number of input samples that make multipliers turned off decreases; then, power reduction becomes smaller and filter performance degradation becomes lower as well. The trade-off between the power saving ratio and the MSE for different m values in case of a 75-tap equi-ripple filter with x_{th} and C_{th} of a FIR ―tap‖ is simply a coefficient/delay pair. The number of IR taps is an indication of the amount of memory required to implement the filter.

4.2 Reconfigurable FIR Filter specification

Following are the specifications on the FIR filters implemented.

- Input sequence and coefficients are 16-bit data with fractional part of 15 bit. Hence, the data range is 16-bit.
- The outputs of the multiplier in the FIR filter are quantized into 16 bit and the final filter output is 24 bit.
- We use as an input threshold, x_{th}, and coefficient threshold, C_{th}. The values of MCSD window length, m, are differently assigned for the filters. The values of x_{th}, C_{th}, and can be controlled by users considering the performance degradation and power savings trade-off presented.

5. COMPARISON OF RESULTS

5.1 Using Table

The results of various multiplier used in our project is described in the following table (Table-1).

Table-1 Results of various multipliers

MULTIPLIER	AREA		DELAY	POWER
	LUT	SLICES		
VEDIC	725	394	47.848ns	0.372W
RUSSIAN PEASANT	686	376	39.533ns	0.274W

From the above table it is clear that the Area, Delay and Power are reduced respectively for each Multiplier. Vedic Multiplier consumed more Area, Delay and Power.

5.2 Using Graph

X-Axis denotes the values and Y-Axis denotes various Multipliers.

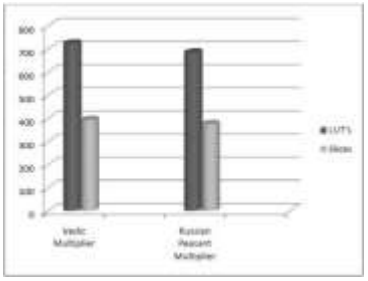

Fig-5: Areas of Multipliers

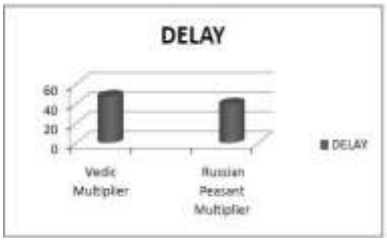

Fig-6: Delays of Multipliers

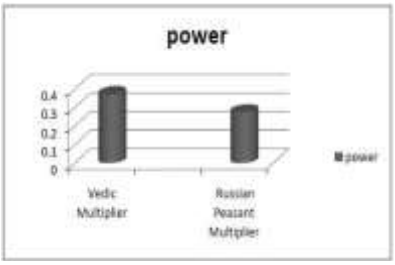

Fig-7: Power of Multiplier

Fig-5 represents the graph for Area of Vedic and Russian Peasant Multiplier. The number of LUT‘s and slices used is Vedic Multiplier is 725 and 394 respectively. The number of LUT‘s and slices used is Russian Peasant

Multiplier is 686 and 376 respectively. Fig-6 represents the graph for Delay of Vedic and Russian Peasant Multiplier. The delay of Vedic and Russian Peasant Multiplier is 47.848ns and 39.533ns respectively. Fig-7 represents the graph for Power of Vedic and Russian Peasant Multiplier. The power used by multipliers is 0.372W and 0.274W respectively. From the above graph, the various Multipliers and their respective Power, Delay and Area are plotted respectively

6. CONCLUSION

An area efficient and high speed Russian Peasant Multiplier is proposed. Russian Peasant multiplier consumes 18 slices, 8.315ns of delay and 0.098W power lesser when compared to conventional Vedic multiplier. The Russian Peasant multiplier has been incorporated in the reconfigurable FIR filter. This proposed reconfigurable FIR filter with Russian Peasant Multiplier is compared with the conventional reconfigurable FIR filter with Vedic Multiplier. The result shows that the proposed reconfigurable FIR filter with Russian Peasant multiplier offers better performance than the conventional reconfigurable FIR filter with Vedic multiplier. In future, the proposed FIR filter is applied in image processing application for sampling process.

7. REFERENCES

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